Using CAD Tools for Shortening the Design Cycle of High-Performance ΣΔM: A 16.4bit 9.6kHz 1.71mW ΣΔM in CMOS 0.7μm Technology

Fernando Medeiro, Belén Pérez-Verdú, José M. de la Rosa and Ángel Rodríguez-Vázquez

Instituto de Microelectrónica de Sevilla-Centro Nacional de Microelectrónica
Edificio CICA, C/Tarfia sn, 41012-Sevilla, SPAIN
Phone #34 5 4239923, FAX #34 5 4231832

Abstract

This paper uses a CAD methodology proposed by the authors to design a low-power 2nd-order ΣΔM. This modulator has been fabricated in a 0.7μm CMOS technology to be used as the front-end of an energy metering mixed-signal ASIC and features 16.4bit at a digital output rate of 9.6kHz with a power consumption of 1.71mW. It yields a value of the $\frac{\text{Power(W)}}{2^{\text{resolution(bit)}} \times \text{Output Rate(Hz)}}$ figure which is the smallest reported to now, thus demonstrating the possibility to design high-performance embeddable ΣΔMs using CAD methodologies.

I. INTRODUCTION

Because of their reduced analog content and high tolerance to hardware imperfections, ΣΔ modulators are well suited to design high-resolution conversion front-ends in mixed-signal ASICs. This is illustrated by the ample variety of their already demonstrated applications, which span from instrumentation to video [1][2][3][4][5][6][7] based on the clever usage of a wide catalogue of modulator architectures: from simple low-order single-bit single-loop architectures with high oversampling ratio (*M*) [8], to elaborate high-order multi-bit, single-loop or multi-stage modulators with low *M* [9][10][11][12][13][14].

Low-power consumption is one of the basic design targets for embeddable analog-to-digital converters. Because reducing the power may compromise the bandwidth, we may resort to the classical $\frac{\text{Power(W)}}{\text{Output Rate(Hz)}}$ figure-of-merit to classify different ADC ICs. However, by using this figure only converters with the same resolution can be compared among them. Recently, an alternative Figure-Of-Merit (FOM) has been proposed which combines power, speed and resolution, to provide a more global view of the universe of ADC ICs [15]. For better fitting to the features of ΣΔMs, the original formula in [15] has been slightly modified here as follows:

$$FOM = \frac{\text{Power(W)}}{2^{\text{resolution(bit)}} \times \text{Output Rate(Hz)}} \times 10^{12} \quad (1)$$

where *Output Rate* is the sampling frequency divided by *M* (usually called DOR). For a given circuit, (1) gives the energy needed per conversion measured in picojoules, and allow us to classify the different low-power ΣΔM ICs reported in literature. Obviously, this classification is neither an absolute ranking, nor attempts to serve as an indicative of the quality of the analog design behind each modulator. It is only useful for illustration purposes. Actually, this is in the very nature of [15] where this FOM is used to quantify the yearly advances on ADCs reported at the International Solid-State Circuits Conference (ISSCC).

During the last six years a number of ΣΔM ICs with FOM smaller than 10pJ have been reported – summarized in Table 1. We see that the smallest reported FOM is 2.1pJ – featured by a 4th-order ΣΔM in a BiCMOS technology [5]. For 2nd-order single-bit modulators, the smallest FOM corresponds to circuit in [16], which operates with only 1.5V supply to provide 12bit@6kHz using a 0.7μm CMOS technology. Larger resolutions in the audio range have been reported for this 2nd-order modulator at the price of larger power consumption and larger FOM values; namely, 16bit@50kHz@4.3pJ in 1μm CMOS technology with 5V supply voltage [17], and 15.3bit@6kHz@8.1pJ in 0.6μm CMOS technology with 1.8V supply voltage [18].

To design ΣΔM ICs for specifications at the state-of-the-art performance edges (i.e. with low values of the FOM) is a complicated and time-consuming task. Because at these performance edges

TABLE 1. Summary of reported ΣΔ Modulators with FOM < 10

	Resolution (bits)	DOR (kHz)	Power (mW)	Process / Supply	Architecture	FOM (pJ)
Yin and Sansen 94 [5]	15.8	1500	180	2μm BiCMOS / 5V	Cascade 2-1-1	2.1
Medeiro et al. 95 [25]	14.8	160	10	1.2μm CMOS / 5V	Cascade 2-2	2.2
Nys and Henderson 96 [28]	19	0.8	1.35*	2 μm CMOS / 5V	2nd-Order, 3bit	3.2
Rabii and Wooley 96 [11]	15	50	5.4	1.2 μm CMOS / 1.8V	Cascade 2-1	3.3
Yin et al. 93 [4]	15.7	320	65	1.2μm CMOS / 5V	Cascade 2-1	3.9
Peluso et al. 96 [16]	12	6	0.1	0.7μm CMOS / 1.5V	2nd-Order	4.1
Brandt et al. 91 [17]	16	50	13.8	1μm CMOS /5V	2nd-Order	4.3
Baird and Fiez 96 [7]	13.7	1000	58	1.2μm CMOS / 5V	4th-Order, 4bit	4.5
Brandt and Wooley,91 [6]	12	2100	41	1μm CMOS / 5V	Cascade 2-1, 3bit	4.8
Williams and Wooley 94 [14]	17	50	47	1μm CMOS /5V	Cascade 2-1	7.2
Dedic 94 [29]	14.7	200	40	1.2μm CMOS /5V	Cascade 2-2-2 (tri-level)	7.7

TABLE 1. Summary of reported ΣΔ Modulators with FOM < 10

	Resolution (bits)	DOR (kHz)	Power (mW)	Process / Supply	Architecture	FOM (pJ)
Grilo et al. 96 [18]	15.3	6	2	0.6 μm CMOS / 1.8V	2nd-Order	8.1

*. Although this ΣΔ converter includes digital filtering, the power computed here consumption corresponds only to the modulator.

the operation is limited by non-idealities other than quantization (thermal noise, incomplete settling, finite opamp-gain, opamp nonlinearities, mismatches, jitter, etc. [19]) a large wealth of knowledge is required to understand the impact of these non-idealities on the modulator performance [4][8][19][20][21]. In addition, intensive optimization is needed to map the high-level specifications of ΣΔMs into working ICs. These difficulties result in the necessity to complete large design cycles, thus compromising the timely marketing of mixed-signal ASICs with embedded ΣΔMs and, hence, their economic success. To alleviate this problem a number of CAD tools and methodologies have been proposed during the last few years [22][23][24][25][26][27]. Unfortunately, only a few of these methodologies have been demonstrated through real working state-of-the-art prototypes. This paper uses the methodology proposed by the authors in [25] to design a 2nd-order ΣΔM whose measurements featured 16.4bit@9.6kHz with a FOM of only 2pJ. This modulator has been fabricated in a 0.7μm CMOS technology to be used as the front-end of an energy metering mixed-signal ASIC requiring to accomplish these specifications for a maximum input of 1V and with minimum possible power consumption. Architecture selection, modulator sizing and cell sizing were supported by CAD tools and completed in only one week by one engineer, while the full-custom layout, which was done manually, took about three weeks.

II. A CAD METHODOLOGY FOR ΣΔM DESIGN

Fig.1 shows the flowgraph of operations involved in the design of ΣΔM ICs. It comprises three different synthesis levels: (a) Modulator level: architecture selection and modulator sizing; (b) Cell level: topology selection and cell sizing; and (c) Layout level: full-custom layout of the modulator. In addition, supervisory simulations should be performed between each couple of levels – usually behavioural simulation between the modulator and cell levels; electrical simulations between the cell and layout levels and electrical simulation of the complete modulator including the extracted layout parasitics in the end of the design cycle.

The CAD methodology presented by the authors in [25] uses a set of dedicated tools to support the most time consuming activities related to the design of switched-capacitor ΣΔM ICs, namely:

1. Modulator Architecture Selection: Depending on the modulator specifications, high-order and

or multibit modulators with small value of *M*, or simpler architectures with larger *M* can be selected to minimize the power dissipation. This is realized with the help of a tool called SDOPT.

2. Modulator Sizing: The same tool is used to automatically obtain specifications for the building blocks in accordance to the modulator specifications. This is done by combining detailed equations relating the circuit imperfections and the noise they introduce at the modulator output, and a statistical optimization algorithm based on simulated annealing.
3. Behavioural Simulation: An advanced sigma-delta simulator (ASIDES) is used to validate the modulator sizing. This program incorporates a large number of building blocks (integrators, comparators, multibit quantizers, D/A converters, etc.) that can be combined in a netlist to define arbitrary modulator topologies. Each block can be considered ideal or defined by a detailed behavioural model that contemplates many of the non-idealities due to the circuit imperfections. Some distinctive features of the tool are: inclusion of thermal noise for the integrators, slew-limited two-pole model for their transient response; non-linearity of capacitors; opamp DC-gain and multibit ADCs and DACs; Monte-Carlo simulations to take into account

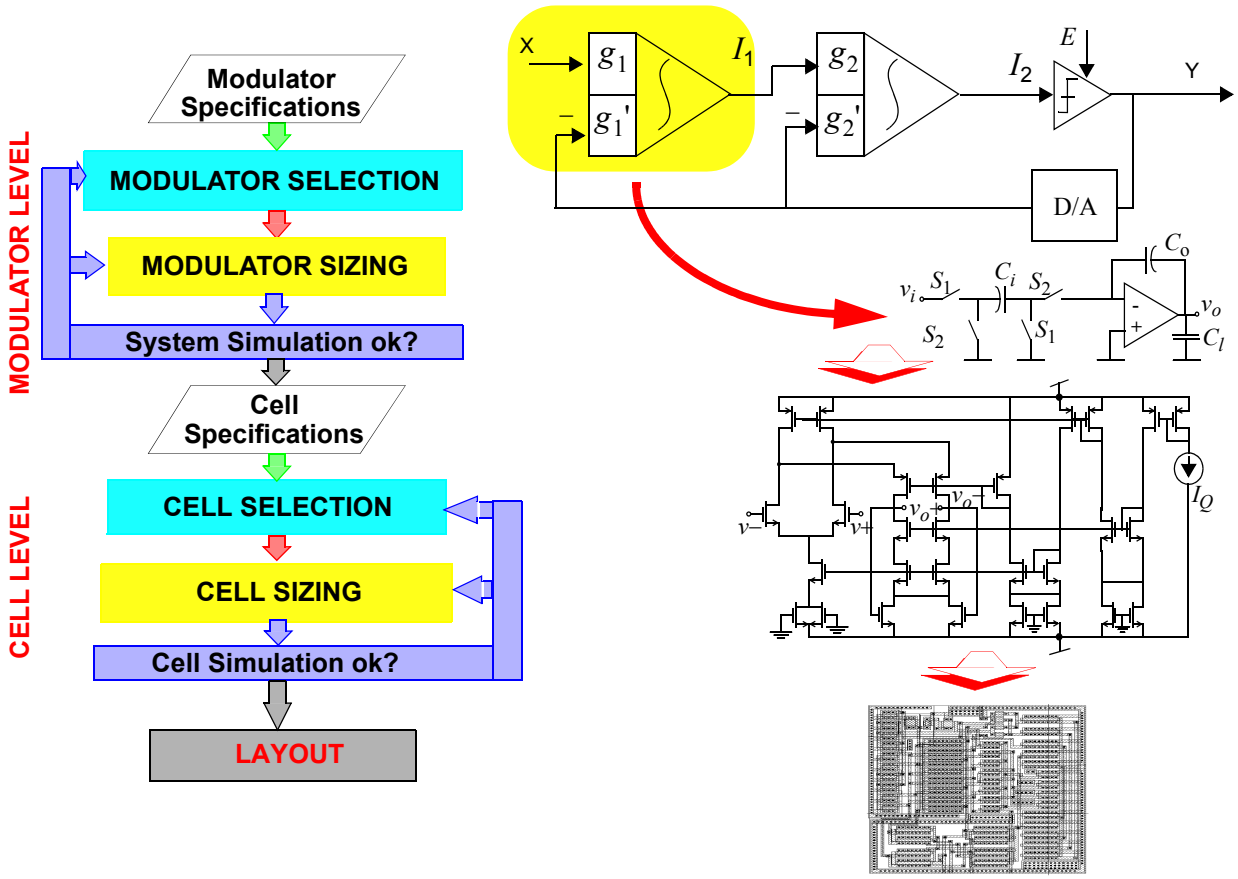

Fig. 1. Operation flow in ΣΔ modulator design.

the mismatch in capacitor ratios, etc.

4. Cell Sizing: A cell level optimizer (FRIDGE) enables the automatic sizing of the building blocks to fulfil their terminal specifications with minimum power dissipation and occupation area. This tool is based on electrical simulation and optimization (either statistical - a set of heuristic has been introduced to accelerate the convergence of simulated annealing algorithms, or a guided algorithm based on the Powell's Method).

In what follows we illustrate the use of this methodology and its related tools to achieve 16.4bit@9.6kHz using a switched-capacitor ΣΔM with the minimum possible value of the FOM, i.e. with the minimum possible power consumption. Such a design objective must be kept in mind at whatever level of the design flow. Particularly, a critical evaluation has to be performed regarding the trade-off between oversampling ratio and hardware complexity. Also, special effort has to be put in reducing the dynamic specifications of the amplifiers which often consume the 80% of the power.

III. ARCHITECTURE SELECTION.

At this level, some simplified equations are used to evaluate the power consumption of available single-bit modulator architectures. The possible benefit [28] of multi-bit quantization regarding

power consumption is difficult to quantify in a general case due to the diversity of the techniques used to attenuate the influence of the DAC non-linearity [7][10][28][30][31]. Thus, such architectures will not be considered in this study.

Let us assume that for whatever modulator the dominant error sources are quantization, thermal noise and incomplete settling noise. Other error sources like integrator leakage, capacitor mismatch and non-linearity, etc. are difficult to include in this simplified analysis and will be considered afterwards. For given resolution, b (bit), the dynamic range (DR) is evaluated as

$$DR = 3 \cdot 2^{2b-1} = \frac{V_r^2/2}{P_Q + P_{Th} + P_{St}} \tag{2}$$

where V_r represents the reference voltage (full-scale input) of the modulator; and P_Q, P_{Th}, and P_{St} are the in-band power of quantization, thermal and incomplete settling noise, respectively. Let us consider that P_{St} is controlled to be well below the other error sources. In such a case,

$$DR \cong \frac{V_r^2/2}{P_Q + P_{Th}} \tag{3}$$

The two noise powers in (3) can be approximated as functions of only three design parameters: modulator order L, oversampling ratio M, and integrator sampling capacitor C_i, as follows:

$$\begin{aligned} P_Q &\cong \frac{(2V_r)^2}{12}\frac{\pi^{2L}}{(2L+1)M^{2L+1}} \\ P_{Th} &\cong \frac{kT}{MC_i} \end{aligned} \tag{4}$$

where k is the Boltzman constant and T is the absolute temperature. Note that in (4) quantization noise has been supposed to be an additive white noise and that the contribution of the first integrator to the in-band thermal noise has been considered dominant as compared to that of other integrators in the modulator loop.

Using (3) and (4) it is possible to calculate a lower bound for the sampling capacitor for given DR, M, and L [1]. Once C_i is known, the equivalent load of the first integrator opamp is evaluated as

$$C_{eq} \cong C_i + C_p + C_l\left(1 + \frac{C_i + C_p}{C_o}\right) \tag{5}$$

1. An absolute lower bound must be imposed regarding layout requirements.

where an integrator like that of Fig.2 with single-stage opamp has been assumed. The opamp input and the integrator output parasitics, C_p and C_l, respectively, can be estimated as a fraction, ζ, of the sampling capacitor. The feedback capacitor, C_o, is also related to the sampling capacitor by the integrator gain. Assuming an integrator gain of 0.5, (5) is rewritten as

$$C_{eq} = (1+\zeta)C_i + \zeta C_i\left[1 + \frac{C_i(1+\zeta)}{2C_i}\right] = \left(1 + 2{,}5\zeta + \frac{\zeta^2}{2}\right)C_i \tag{6}$$

where C_p and C_l have been estimated as ζC_i.

To accomplish the previous assumption that $P_{St} \ll P_Q, P_{Th}$, the unity gain frequency of the opamp, given by $g_m/(2\pi C_{eq})$, should be large enough to render the settling error of the integrator negligible. A conservative choice is to make,

$$g_m/(2\pi C_{eq}) = 5f_S \tag{7}$$

where f_S represents the sampling frequency. This expression allows us to make an estimation of the transconductance needed in the opamps.

At this point, in order to estimate the power consumption, one more assumption has to be made regarding the topology of the opamp used for the integrators: Let be the opamp a folded-cascode OTA with the same current, I_B, flowing through the differential pair and the output branches. Assume also that the same current is used in the biasing stage. Thus, the total current spent by one opamp is $4I_B$. The current I_B depends on the required g_m as $I_B = g_m^2/(2\beta)$, where β is the transconductance parameter of the input transistors. Once the tail current of the opamps has been estimated, the static power can be calculated as

$$P_{WS} = 4I_B V_{supply} L \tag{8}$$

where V_{supply} is the supply voltage. Note that L identical opamps have been considered for simplicity.

On the other hand the dynamic power dissipated to commute a capacitor C_i between the reference voltages can be approximated by $P_w = (2V_r)^2 C_i f_S$. Using fully-differential circuitry there are

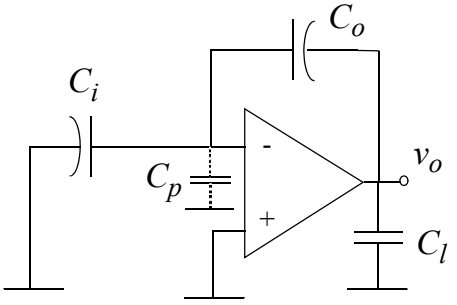

Fig. 2. SC integrator during the integration phase

6 commuting C_i per integrator (assuming $C_o = 2C_i$). Thus, the dynamic power of the analog part of a *L*Th-order modulator can be approximated by,

$$P_{WD,\,\text{analog}} = 6L(2V_r)^2 C_i f_S \tag{9}$$

In addition the dynamic power of the modulator digital part (quantizer, flip-flop and gates) has to be taken into account. However that power strongly depends on the number of quantizers in the modulator as well as the specific circuitry used to implement them. As a gross approximation we shall use the following expression:

$$P_{WD,\,\text{digital}} = 10N \cdot 5\text{mW}(1\text{ns}) f_S \tag{10}$$

where N denotes the number of quantizers (latch + flip-flop + small logic), each of them with 10 equivalent inverters commuting with a power peak of 5mW within 1ns. The value of N depends on the modulator architecture: It is one for single loop modulators and larger for cascade modulators. We will suppose a value $N = L/2$.

The above equations have been included into the modulator sizing tool, SDOPT, and used to estimated the FOM of several single-bit modulators architectures, from $L = 2$ to $L = 6$. Each architecture showed different suitability degrees for different regions of the resolution-bandwidth plane. We have found that for resolution around 17bit and above the lowest FOM corresponds to the 2nd-order modulator. This is because for those resolution levels the modulator output spectrum is thermal noise dominated. Thus, although the quantization noise can be reduced by using higher order modulators, the sampling capacitor cannot due to the thermal noise restriction, resulting in the same current per opamp. Fig.3 shows the estimated FOM as a function of the oversampling ratio to obtain 17bit@10kHz with several modulator architectures. The lowest FOM is featured by the 2nd-order modulator with oversampling ratio close to 300. According to these results, the 2nd-order single-loop ΣΔ modulator of Fig.4 with oversampling ratio equal to 256 was selected.

IV. SWITCHED-CAPACITOR IMPLEMENTATION

The modulator has been implemented using fully-differential switched-capacitor (SC) circuits.

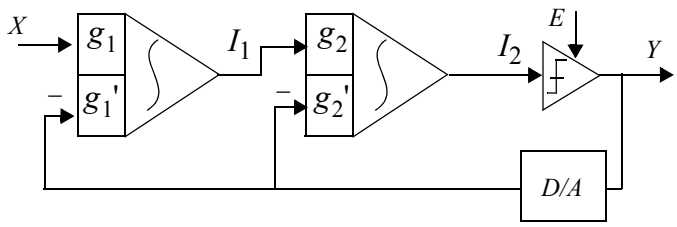

Fig. 4. Block diagram of the second-order modulator

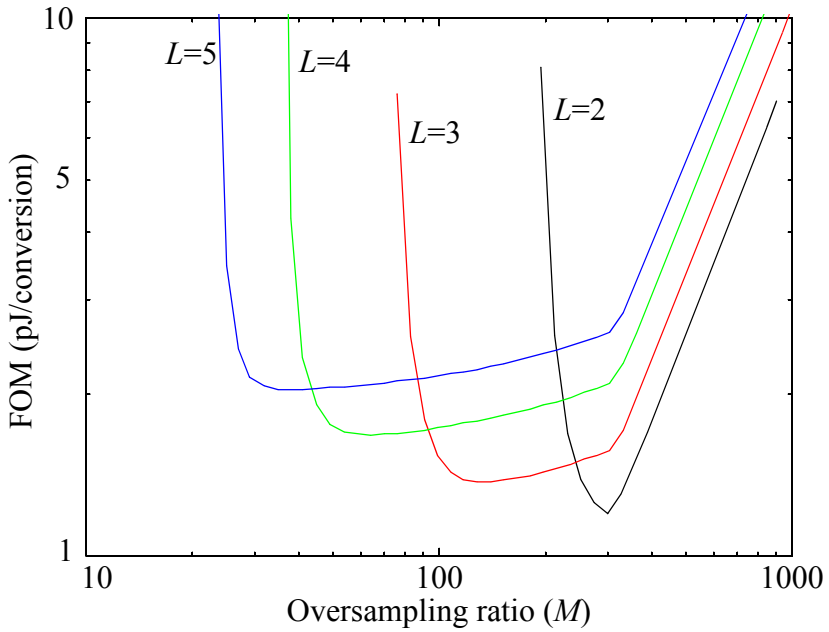

Fig. 3. Estimated FOM to obtain 17-bit resolution and 10-kHz DOR with several modulator architectures, as a function of the oversampling ratio.

Besides its robustness, this technique provides good suppression of common-mode interference. The integrator weights have been selected to minimize the required output-swing (OS) and speed of the two integrators. By using $g_1 = g_{1'} = g_2 = 0.25$ and $g_{2'} = 0.5$, the voltage swing at the integrator output is reduced so that the OS can be clipped at only the reference voltage, instead at twice the reference voltage as required using the classical choice $g_1 = g_{1'} = g_2 = g_{2'} = 0.5$. Fig.5 shows the SC fully-differential second-order ΣΔ modulator. Note that the opamp of the first integrator includes a chopper compensation technique to attenuate its offset and low-frequency noise. The second integrator has two branches to implement two different weights g_2 and $g_{2'}$. This is not necessary in the first integrator where the weights of the input and feed-back paths are the same.

Modulator timing consists of two non-overlapping phases and two delayed versions of them used to avoid signal-dependent feed-through errors. A chopper phase is also needed. Switches with large voltage swing, identified as "sc" in the schematic, are complementary to get maximum linearity. Each clock phase and its complementary will be routed together in the layout to minimize the substrate noise.

A. Modulator sizing

The specifications for the building blocks and other design parameters at the modulator level have been optimized using SDOPT to obtain the values shown in Table 2. This optimization is based on a set of equations relating the non-idealities of the building blocks to the power of noise and/or distortion that they introduce in the modulator base band [8][19][21][25]. For instance, the opamp

transconductance, g_m, is related to the in-band power of the incomplete settling error, P_{St}, as follows:

$$P_{St} = \frac{(2V_r)^2}{9M}\left(1+\frac{C_p}{C_i}\right)^2\left(\frac{C_i}{C_{eq}}\right)^2\left(1+\frac{C_l}{C_o}\right)^2 \exp\left(-\frac{g_m}{C_{eq}}\frac{1}{f_S}\right) \tag{11}$$

where V_r, C_p, C_i, C_o, C_l, C_{eq} and f_S were defined in Section III. Such equation was also used to estimate the constraint on the opamp unity gain frequency given in (7). Similar equations have been used to contemplate the effect of other circuit non-idealities.

The reference voltages has been set to ±1.5V (differential value) to have a margin respect to the maximum modulator input level which equals 1V. The power of noise and distortion contributions in the baseband are given in the end of the Table 2. Note that the incomplete settling noise is the dominant error source – the transconductance and output current of the opamp have been chosen as low as possible to minimize the power consumption. Other noise sources, including quantization, have approximately the same influence. The total inband noise power referred to the full-scale input leads to a dynamic range of 98.3dB which is large enough to ensure more than 16bit effective resolution.

Behavioural simulations have been performed using ASIDES to validate the modulator sizing. In these simulations each building block has an associated model containing the specifications obtained from SDOPT. Fig.6 shows the output spectrum of the modulator and its signal-to-(noise+distortion) ratio (SNDR) as a function of the input signal level. These results confirm the correctness of the specifications for the building blocks.

B. Operational amplifier design

Since the maximum output current and the DC-gain requirement are not very demanding, a sin-

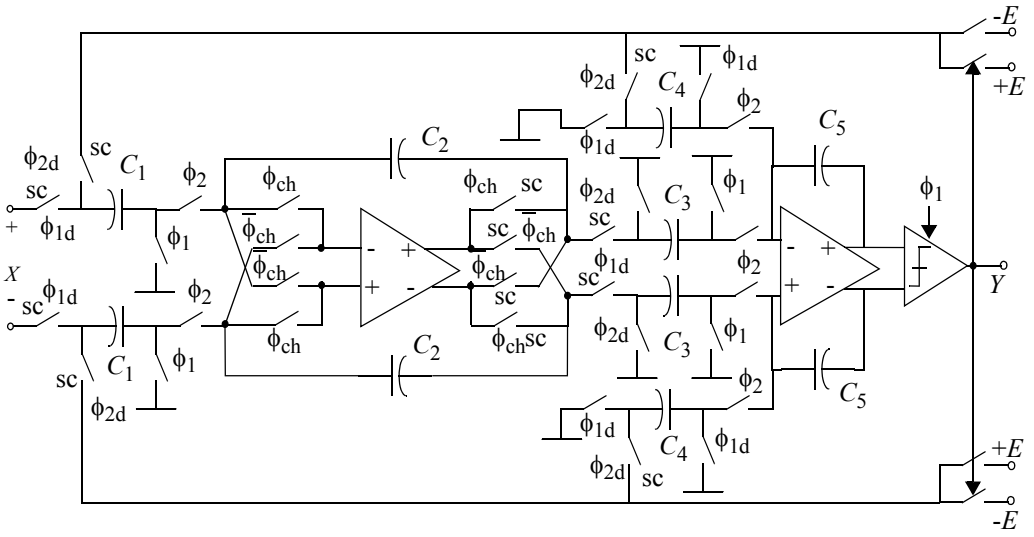

Fig. 5. Chopper-compensated SC fully-differential 2nd-order ΣΔ modulator

TABLE 2. Results of the modulator sizing

OPTIMIZED SPECS FOR:		16bit@9.6-kHz DOR@±1.5V
Modulator	Topology	2n-order
	Sampling frequency (MHz)	2.4576
	Oversampling ratio	256
	Reference voltages (V)	±1.5
Integrators	C_1, C_3 (pF)	1
	C_2 (pF)	4
	C_4 (pF)	0.5
	C_5 (pF)	2
	Capacitor non-linearity (p.p.m.)	≤ 50
	MOS switch-ON resistance (kΩ)	2.0
	Maximum clock jitter (ns)	≤ 2.0
Opamps	DC-gain (dB)	≥ 66.0
	DC-gain non-linearity (V^{-2})	≤ 20%
	gm (μA/V)	196
	Maximum output current (μA)	≥ 30
	Total output swing (V)	≥ 4.0
	Input noise density (nV/sqrt(Hz))	≤ 20.0
	Parasitic input capacitor (pF)	≤ 0.2
Comparators	Hysteresis (mV)	≤ 70
	Resolution time (ns)	≤ 50.0
RESOLUTION & NOISE POWER CONTRIBUTIONS		
Dynamic range:		98.3dB (16.04bit)
Quantization noise (dB)		-108.7
Thermal noise (dB)		-107.1
Incomplete settling noise (dB)		-99.3
Jitter noise (dB)		-118.1
Harmonic distortion (dB)		-107.0

gle-stage class-A amplifier is preferred. In particular, the fully-differential folded-cascode architecture of Fig.7 has been selected for the opamps that form the integrator core. A nmos-input topology is preferred to a pmos-input as long as flicker noise is not relevant (provided that chopper is activated) and white noise is. The opamp core if formed by transistors M_1 to M_{11} while the biasing stage com-

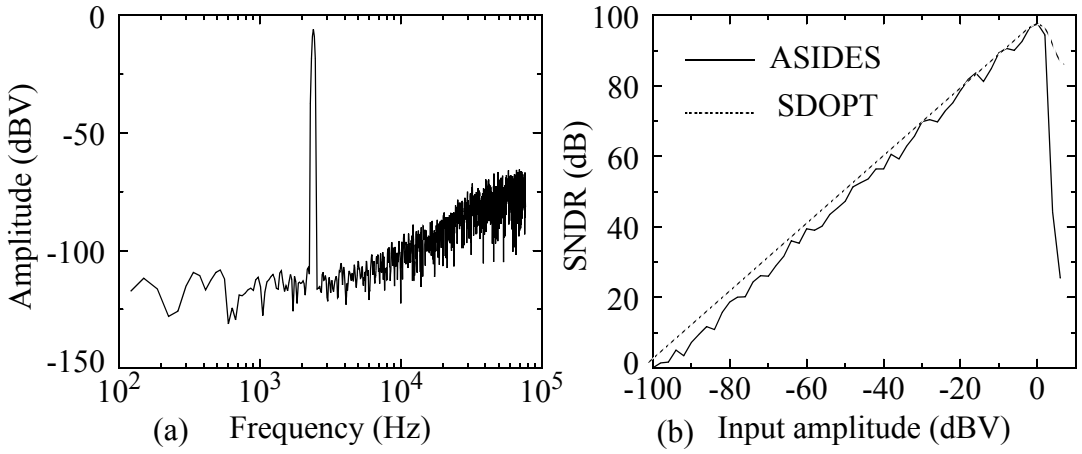

Fig. 6. Behavioral simulations: (a) Output spectrum for a 0.5-V@1.2kHz input. (b) SNDR as a function of the input level.

prises transistor M_{12} to M_{14}. A low-distortion current steering common-mode feedback net (CMFB) has been used (transistors M_{15} to M_{24}) [32]. Transistor M_{25} generates the bias voltage for the nmos-type current sources, while the pmos-type current sources are regulated by the CMFB net. This architecture has been automatically sized using FRIDGE to fulfil the specifications of Table 2 within a temperature range of [-25°, 85°] and for power supply range of [4.75V, 5.25V], which after 25min CPU time provided the sizes displayed in Table 3. *Ibias* was set to 30μA although it can be increased up to 45μA without degradation of the output swing. Table 4 summarizes the simulated performance. Terminal specifications correspond to the worst-case value obtained in the temperature and supply voltage operating range.

TABLE 3. Transistor sizes for the opamp (in microns)

Trans.	W/L	Trans.	W/L
$M_{1,2}$	70.5/2	M_{14}	2/4
$M_{3,4}$	15.8/2	M_{15}	15/2

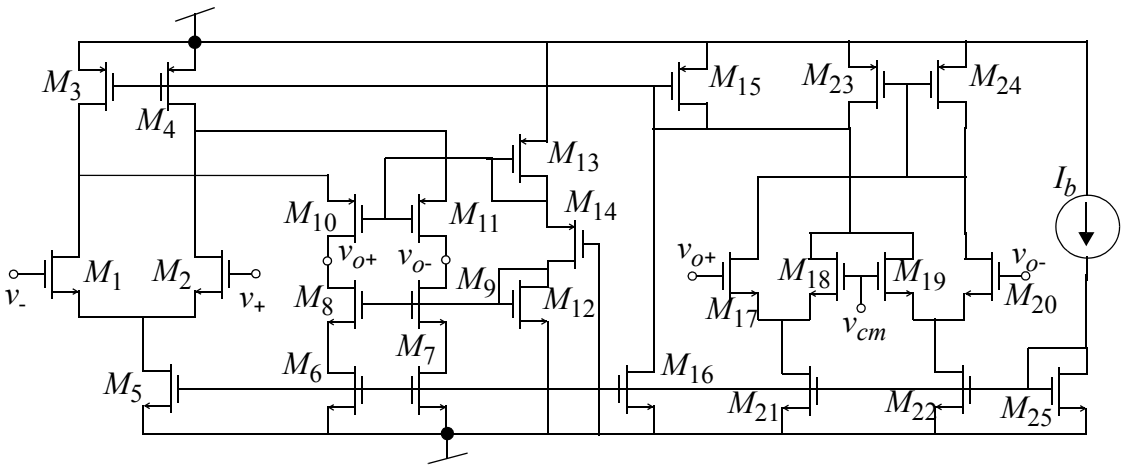

Fig. 7. Fully-differential folded-cascode opamp

TABLE 3. Transistor sizes for the opamp (in microns)

Trans.	W/L	Trans.	W/L
M_5	37.2/2	M_{16}	37.2/2
$M_{6,7}$	20.5/2	$M_{17,18}$	2/4.5
$M_{8,9}$	39.9/1.2	$M_{19,20}$	2/4.5
$M_{10,11}$	78.8/1.2	$M_{21,22}$	37.2/2
M_{12}	5/5	$M_{23,24}$	15/2
M_{13}	5/5	M_{25}	37.2/2

TABLE 4. Simulated performance of the folded-cascode opamp

Specs.	Worst case value	Unit.
DC-gain	85.1	
gm	196	μA/V
GB (1.2pF)	20.7	MHz
PM (1.2pF)	70	Degree
PSRR+ (1kHz)	192	dB
PSRR- (1kHz)	161	dB
CMRR (1kHz)	84	dB
White input noise	17	nV/√Hz
Total output swing	5	V
Maximum output current	30	μA
Supply current	127	μA

Fig.8 shows the layout of the opamp in a 0.7μm CMOS technology with a size of 140x114μm^2. In the layout all matched transistors were placed using common-centroide techniques. To protect against switching noise, properly biased guard rings were placed round the active devices.

C. Comparator design

Since no excessive resolution is needed (see Table 2) the regenerative latch of Fig.9(a) is selected for the core of the comparator. This is activated in phase ϕ_1 and a nor-gate SR flip-flop, Fig.9(b), is provided to hold the output data during the phase ϕ_2. The latch has been sized using FRIDGE to fulfil the specifications in Table 2. Sizes are given in Table 5. Note that it is possible to use small input transistors because the foreseen offset is not relevant -- it will be eliminated by the

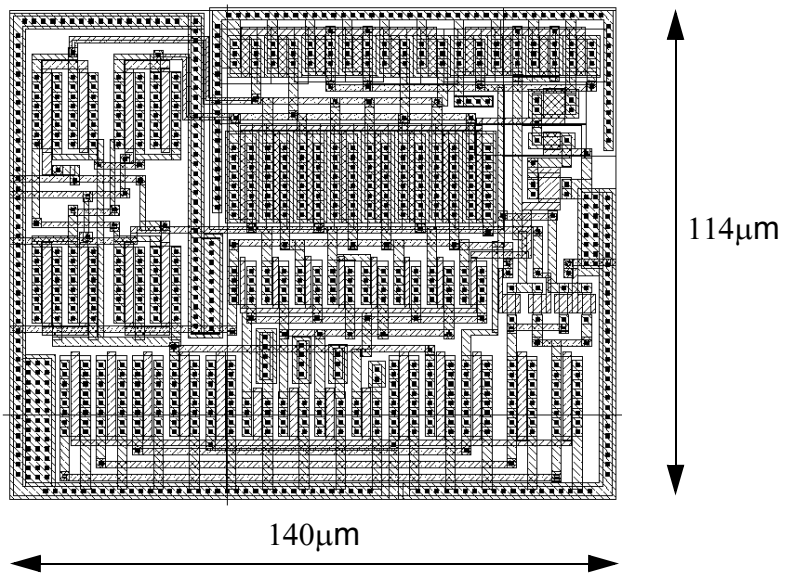

Fig. 8. Layout of the fully-differential folded-cascode opamp in 0.7μm CMOS technology

high DC-gain of the integrators in the loop. The simulation results corresponding to the worst case are shown in Table 6.

TABLE 5. Comparator sizes (in microns)

Trans.	W/L	Trans.	W/L
$M_{1,2}$	1.5/5	$M_{5,6}$	4/2
$M_{3,4}$	1.5/5	$M_{7\text{-}10}$	2.2/0.7
		$M_{11\text{-}14}$	2.2/0.7

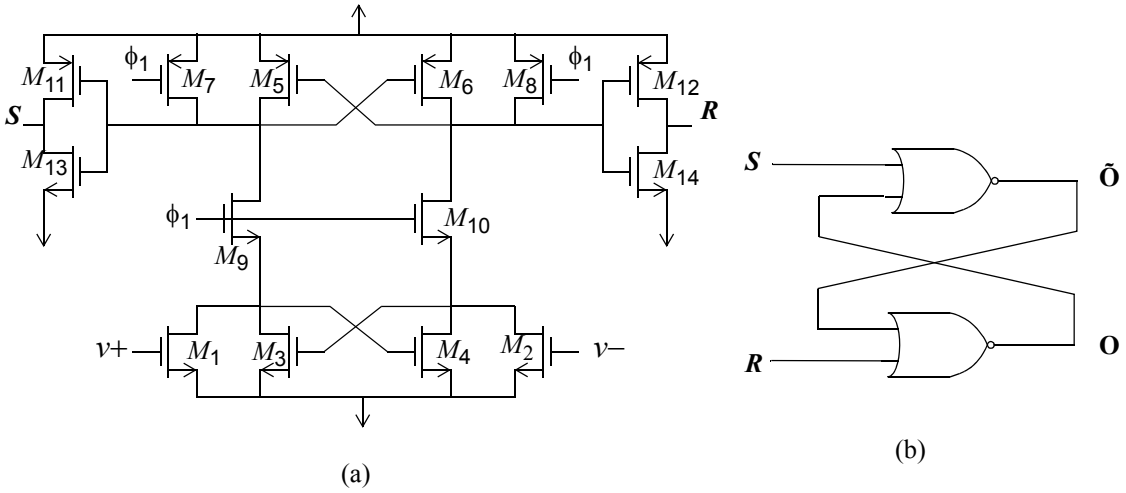

Fig. 9. Comparator. (a) Regenerative latch. (b) SR flip-flop

TABLE 6. Simulated performance of the comparator

Specs.	Worst case value	Unit.
Hysteresis	0	mV
Offset	-10	mV
Resolution time	9	ns

V. EXPERIMENTAL RESULTS

Two chips were fabricated for test purposes. One chip containing the modulator basic blocks, amplifier and comparator, and other containing the modulator and the clock generator with possibility to enable or disable the chopper operation. Results taken from both chips are given next.

A. Basic blocks

Table 7 summarizes the performance of the amplifier obtained by measuring eight samples. Static measurements show that the DC-gain is slightly lower than expected but is large enough to ensure maximum performance. Also a minor deviation is found in the average value of the transconductance. Other measurements agree with the simulation results.

TABLE 7. Summarized performance of the amplifier

	Measured	Units
DC-gain	80	dB
gm	210	μA/V
Max. output current	-31,29.2	μA
Total output swing	5	V
Offset	3.6	mV

Fig.10 shows the transfer curve of the latched comparator obtained for 2.5-MHz clock frequency. The offset and hysteresis varied from sample to sample. The average and worst case values obtained (eight samples) are shown in Table 8 together with the resolution time.

TABLE 8. Measured performance of the comparator

Specs.	Average	Worst case	Unit.
Hysteresis	28	34	mV
Offset	-27	-35	mV
TPHL	9.4	-	ns
TPLH	10	-	ns

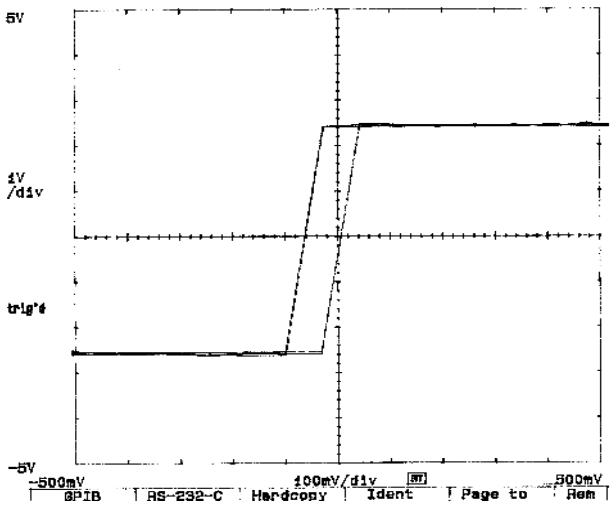

Fig. 10. Measured transfer curve of the latched comparator

B. Complete modulator

Fig.11 shows a microphotograph of the modulator chip in 0.7μm CMOS single-poly technology which presents an active area of 0.42mm^2 and consumes 1.71mW from a 5-V power supply. A two-layer board was fabricated to measure the performance of the modulator [33] with separated analog and digital ground planes, decoupling capacitors and signal filtering to attenuate the switching noise in the analog signal and biasing traces. The modulator was evaluated using a high-quality fully-differential programmable input signal source (THD < -100dB). A digital data acquisition system was used to generate the clock signal and to acquire the serial modulator output at the clock rate. Data were acquired automatically by controlling the test set-up with proprietary *C* routines and transferred to a

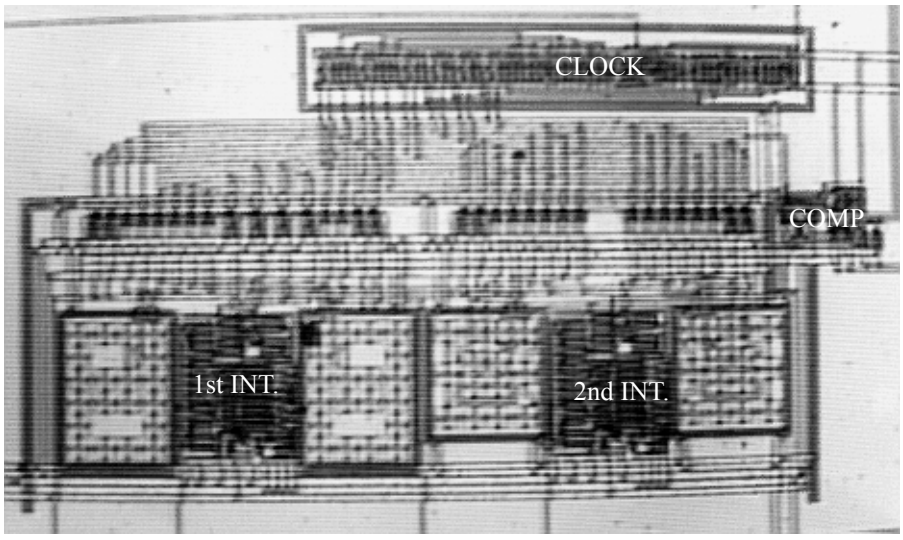

Fig. 11. Microphotograph of the second-order ΣΔ modulator. Clock phase generator is also shown.

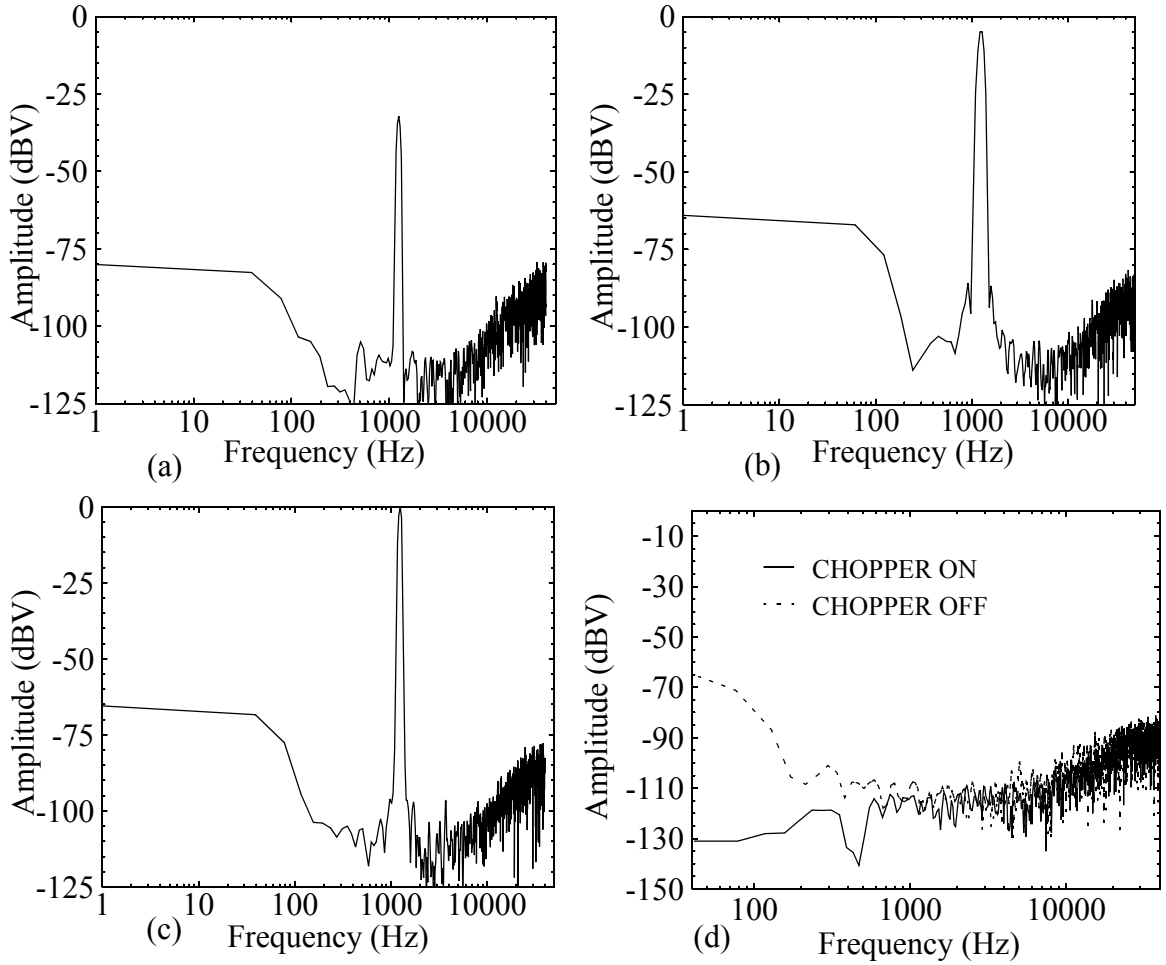

Fig. 12. Measured output spectrum of the modulator for (a) -32, (b) -2 and (c) 0-dBV amplitude and 1.25-kHz input tone. (d) Effect of the chopper compensation.

workstation to perform the decimation filtering using MATLAB. Fig.12(a), (b) and (c) show the modulator output spectrum with chopper not activated for different input amplitudes and 1.25-kHz frequency. Note that the noise floor in the base band is flat (around -115dBV) and no large noise patterns are observed. On the other hand, total harmonic distortion for 1-V amplitude is below -90dB. Fig.12(d) shows the output spectrum for no input with chopper enabled and disabled. Note that, when chopper is active, the offset is significantly reduced.

Measurements of the signal-to-noise ratio (SNR) and SNDR figures were obtained processing the modulator output bit stream with a digital filter implemented by software. Fig.13 shows both ratios for an input tone at 1.25kHz and oversampling ratios of 128 and 256 as a function of the input level. The dynamic range measured for $M = 256$ is over 100dB with a SNR-peak of 94.2dB corresponding to 1.2-V input and a SNDR-peak of 91.8dB for 0.8-V input. Respect to the case $M = 128$, the dynamic range is 92dB with SNR and SNDR peaks of 84.4dB for 1-V input.

Measurements of the dynamic range versus the oversampling ratio for given clock rate, see

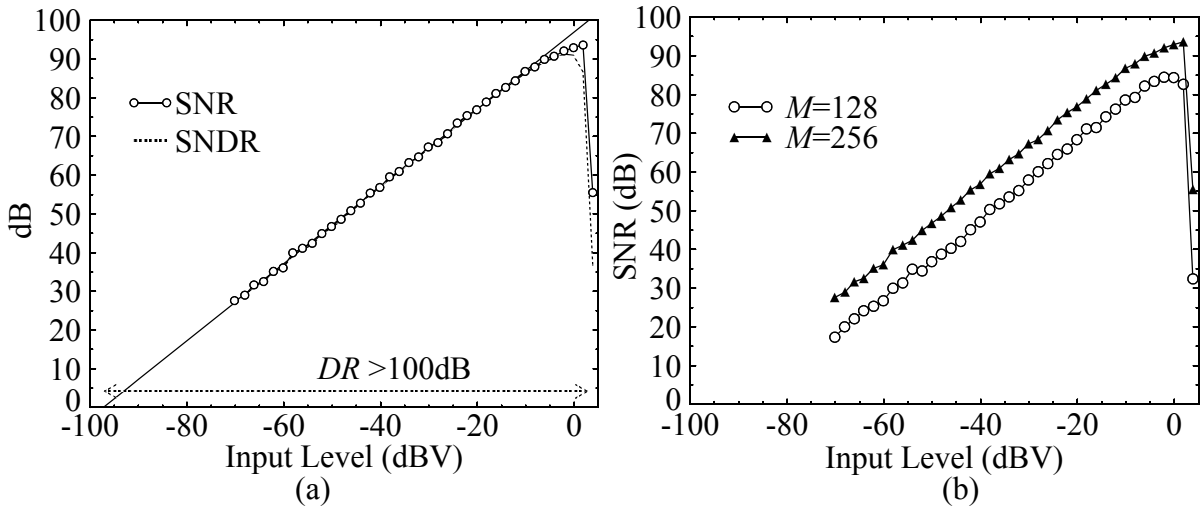

Fig. 13. Measured SNR and SNDR for an input tone of 1.25kHz and amplitude variable, (a) for M=256 and (b) for M=256 and M=128. In all cases the clock frequency was set to 2.56MHz.

Fig.14, show that for M = 256 the modulator is just on the limit between the quantization noise limited region (slope=15dB/octave) and the white noise limited region (3dB/octave) – a consequence of the dominance of the incomplete settling noise.

The modulator performance is summarized in Table 9 for three oversampling ratios M =128, 256 and 512. Note that, for the nominal value of M = 256, the FOM of the modulator is only 2pJ/conversion which is lower than those in Table 1. However the FOM increases for the two other values of M. This shows that the modulator has been optimized for the nominal oversampling ratio

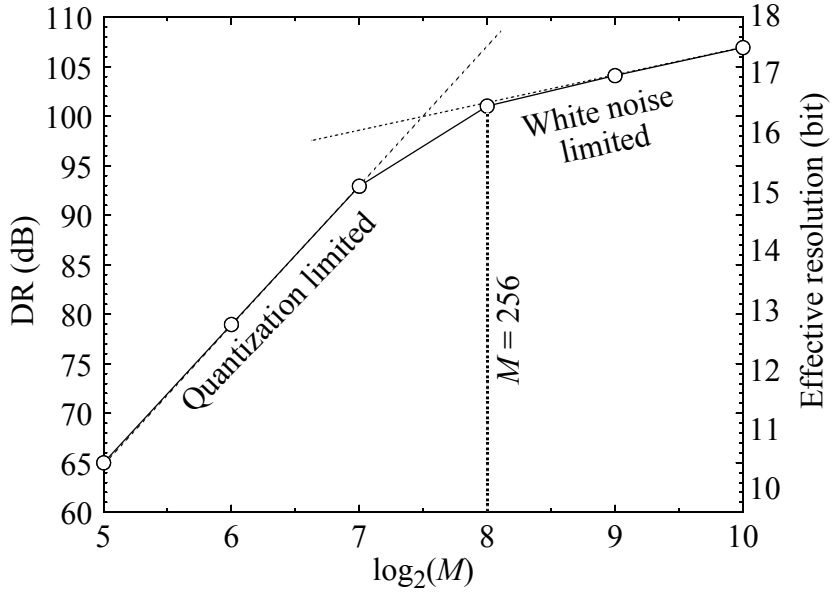

Fig. 14. Measured dynamic range versus oversampling ratio.

and, although it is possible to obtain better resolution with higher values of *M*, the FOM increases as well.

TABLE 9. Summarized performance of the modulator

	M = 128	*M* = 256	*M*=512	Units
Effective resolution	15	16.4	17.1	bit
DR	92	100.2	105	dB
SNR-peak	84.4	94.2	101	dB
SNDR-peak	84.3	92	99	dB
DOR	19.2	9.6	4.8	kHz
Max. input voltage (before overload)	1.25			V
Power (2.5MHz clock rate)	1.71			mW
Active area	0.42			mm^2
Minimum supply voltage	4			V
FOM	2.7	2.0	2.5	pJ/conversion

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