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Towards minimum achievable phase noise of relaxation oscillators

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ABSTRACT

A relaxation oscillator design is described, which has a phase noise rivaling ring oscillators, while also featuring linear frequency tuning. We show that the comparator in a relaxation-oscillator loop can be prevented from contributing to $1/f^2$ colored phase noise and degrading control linearity. The resulting oscillator is implemented in a power efficient way with a switched-capacitor circuit. The design results from a thorough analysis of the fundamental phase noise contributions. Simple expressions modeling the theoretical phase noise performance limit are presented, as well as a design strategy to approach this limit. To verify theoretical predictions, a relaxation oscillator is implemented in a baseline 65 nm CMOS process, occupying 200 μm × 150 μm. Its frequency tuning range is 1–12 MHz, and its phase noise is L(100kHz) = −109dBc/Hz at f_{osc} = 12MHz, while consuming 90 μW. A figure of merit of −161dBc/Hz is achieved, which is only 4 dB from the theoretical limit. Copyright © 2012 John Wiley & Sons, Ltd.

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KEY WORDS: oscillator; low noise; phase noise; figure of merit; FoM; jitter; relaxation oscillator; thermodynamics; linear frequency tuning; large frequency tuning range; power efficiency

1. INTRODUCTION

Oscillators are important circuits for on-chip frequency synthesis and digital clock generation. They can oscillate autonomously, but are also often locked to an external reference clock via a phase locked loop. LC oscillators are commonly used for phase noise critical high-frequency applications, which can live with a limited frequency tuning range (typically 5–20%). They take up an excessive area for lower frequencies, say below 1 GHz, where it becomes difficult to realize high-Q coils with sufficiently large inductance. RC oscillators on the other hand can be quite compact, even at lower frequencies. In addition, they feature a large tuning range. Both ring oscillators and relaxation oscillators are forms of RC oscillators [1]. Relaxation oscillators have an important advantage over ring oscillators: they not only feature a large, but also a *linear* tuning range. A linear control characteristic is often convenient, while being crucial for FM modulation and demodulation with low distortion [2].

Figure 1 shows a relaxation oscillator topology based on two resistors that alternately charge and discharge capacitor C_1. The capacitor voltage cycles between a high voltage V_H and a low voltage V_L controlled by a comparator with hysteresis. Such a resistor-based topology has a period time

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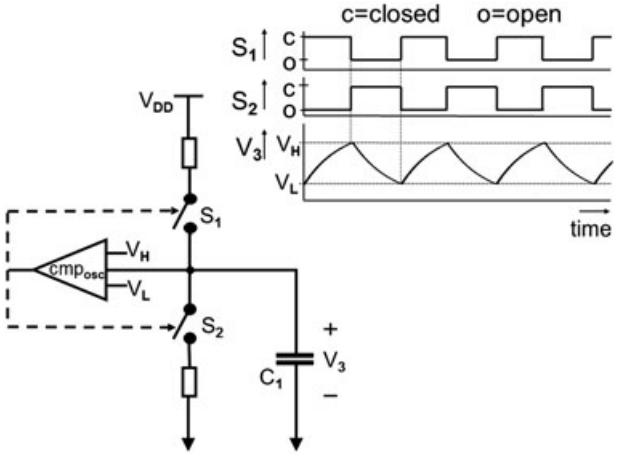

Figure 1. Basic relaxation oscillator topology based on resistive charging [1].

which linearly depends on resistance and capacitance. If resistors are replaced by current sources, a linearly current-controlled frequency can be realized.

A study by Navid *et al*. has shown that the phase noise performance of RC oscillators is fundamentally bound by thermodynamics to a level that is rather poor compared to that of typical LC oscillators [1]. Meeting a phase noise specification with an RC oscillator can thus easily result in high power consumption. To minimize power dissipation, RC oscillator designs that perform near to their theoretical limit are wanted, and this paper pursues this aim for a relaxation oscillator.

To characterize phase noise and jitter, the single-sided power spectral density L(f) is useful (see Appendix A for its exact definition and relation to jitter). Figure 2 shows L(f) for a typical relaxation oscillator, with three indicated regions. Two 'colored' regions, a $1/f^3$ region and a $1/f^2$ region, are caused by flicker and white noise that gets integrated in the oscillator [3]. Furthermore, white noise can be added directly without integration, e.g. white noise in an output buffer contributes a 'white noise floor'.

In a phase locked loop, $1/f^3$ noise can often be suppressed significantly by the loop gain, [4] and the $1/f^2$ noise of the oscillator is the most important timing jitter contribution together with the (usually white) noise of loop-components [4]. The value $L(f_{f-2})$ measured in the $1/f^2$ region is thus of crucial importance. To benchmark oscillator phase noise, the 'oscillator number' N_{osc} is useful [3] (see (21) in Appendix A). To quantify $1/f^2$ phase noise, taking into account the power consumption of the oscillator core P_{core}, the well-known figure of merit (FoM) of (22) is often used [5, 6] (see Figure 2 and appendix A).

In Figure 3, FoM values for RC oscillators are indicated, based on [1]. Practical ring oscillators can be close to the theoretical FoM limit of −165 dBc/Hz at 290 K. In contrast, relaxation oscillators have a

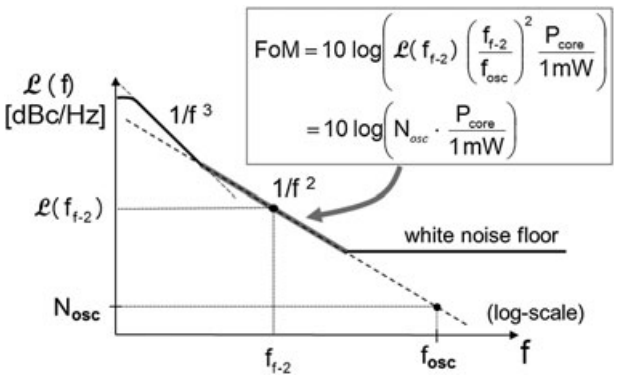

Figure 2. Phase noise plot with $1/f^3$, $1/f^2$ and white region and definitions of Nosc and FoM (see also Appendix A).

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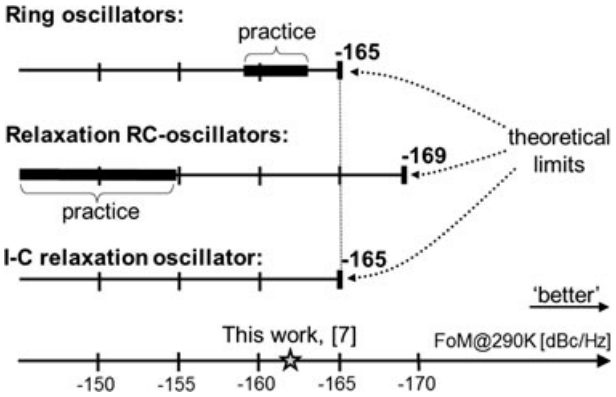

Figure 3. Overview of theoretical and practical achievable FoMs of various oscillators.

better theoretical FoM limit (−169 dBc/Hz), but worse practically achieved values [1,7]. This can be explained partly by the phase noise contribution of the loop-comparator (cmp_{osc} in Figure 1), which is present in a relaxation oscillator to switch been charging and discharging, but is not present in ring oscillators [1]. During the calculation of this theoretical limit in [1], only the noise of the charging and discharging process was modeled, while comparator noise was neglected. This loop-comparator noise contribution turns out to be significant, and this paper will show how it can be prevented to translate into phase noise. Doing so, we aim to close the phase noise gap between practical relaxation oscillators and ring oscillators. The oscillator circuit and phase noise measurements were earlier reported in [7], but this paper provides a theoretical foundation, discusses a practical design strategy and reports some additional comparisons of measurements with simulation results.

The contents of this paper are organized as follows. In Section 2, we show how comparator noise can be prevented from contributing $1/f^2$ phase noise. We analyze the remaining fundamental $1/f^2$ colored phase noise contributions in a relaxation oscillator, i.e. the white noise of the charging and the discharging mechanism, and develop simple though precise phase noise expressions. Based on these expressions, we devise a design strategy to maximize the phase noise performance. In Section 3, we will describe a new switched-capacitor relaxation oscillator topology [2] based on the developed insight and show that the simple phase noise expressions still hold for this topology. We then describe a transistor implementation in Section 4 and explain how it can be designed to perform near to the theoretical FoM limit. In Section 5, we discuss measurement results, while Section 6 draws conclusions.

2. TOWARDS THE THEORETICAL LIMIT OF PHASE NOISE

We will now discuss a technique which can prevent the noise of the oscillator loop-comparator from contributing $1/f^2$ phase noise, so that its power consumption can be reduced. We will abandon the general relaxation oscillator topology of Figure 1 based on resistors and use the topology given in Figure 4, based on current sources instead (I-C relaxation oscillator). This topology shows a linear tuning range if the current sources are controlled linearly.

2.1. Eliminating the comparator noise

In the relaxation oscillator topology of Figure 4, the charging mechanism is implemented by current source I_1 that charges capacitor C_1 continuously. As a result, the capacitor voltage V_3 increases linearly in time and when it crosses V_M, an active edge is produced at V_{OUT}. When the capacitor voltage subsequently crosses V_H, the discharging mechanism is activated which discharges the capacitor by a fixed amount of charge. The discharging mechanism can be implemented by a 'one-shot' (mono-stable circuit) that produces a pulse with fixed time-width in response to a trigger, in

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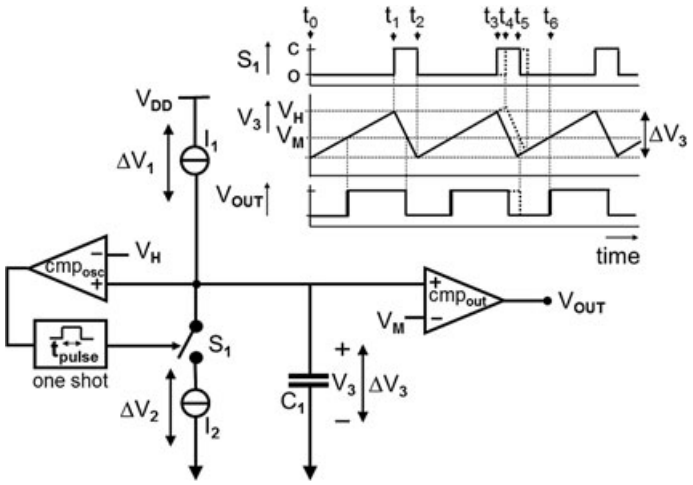

Figure 4. Current source-based relaxation oscillator with rising output edges insensitive to noise and delay of comparator cmp_{osc}.

combination with an ideal current source I_2, which is also fixed. Assuming first a situation in which the comparator cmp_{osc} is noiseless, this discharging takes place in the interval $[t_1, t_2]$ in Figure 4.

Now, suppose the comparator cmp_{osc} is noisy, i.e. the discharge pulse does not start at the nominal time t_3, but at a somewhat shifted instant t_4 as shown in Figure 4. Although the discharge ramp voltage is shifted, the rising edge of V_{OUT} still crosses V_M at the right time t_6. Thus, the *active edge* is *unaffected and so is the phase noise associated with the rising edge of* V_{OUT}. Of course, the falling edge is shifted (from t_4 to t_5), changing the duty cycle of V_{OUT}. This is acceptable in many applications that only use the rising edge. If a reliable 50% duty is needed, this can be realized adding a divider triggered on rising oscillator edges while doubling the oscillator frequency. Of course, cmp_{out} also adds noise, but this is white noise which is not integrated to $1/f^2$ noise (to be discussed later).

In periodic steady state (PSS), the charge flowing into the capacitor during a period of oscillation (T_{osc}) is equal to the charge flowing out of the capacitor during the same period, i.e. $Q_{in} = I_1 T_{osc} = Q_{out} = I_2 T_{pulse}$ or $f_{osc} = I_1 / Q_{out}$. By choosing Q_{out} *fixed*, the oscillation frequency is a linear function of I_1 and independent of the delay and noise of cmp_{osc}.

Summarizing, if the discharge packet Q_{out} can be fixed, this technique effectively eliminates the noise contribution of the comparator. More precisely, it prevents the noise of the comparator cmp_{osc} to translate into $1/f^2$ *colored* phase noise, i.e. prevents it to get integrated into the period of oscillation. This technique with one-shot resembles the anti-jitter circuit technique [8], albeit for another application (reject jitter of an incoming clock signal by the use of a frequency locked loop).

Taking a skeptic view, one might note that we shifted the problem of the noisy comparator to the one-shot that needs an accurate on-time to keep Q_{out} fixed. We will show in Section 3, though, that we can apply this technique without the need for this one-shot.

Before doing so, we will first calculate the theoretical phase noise performance limit for the circuit in Figure 4, which uses current sources instead of resistors and will also devise a FoM-enhancement circuit design strategy.

2.2. *Noise current fed to a capacitor*

The noise calculations that will follow all relate to the case where a noise current is fed to a C with parallel 'leakage resistor' for some time, which will be analyzed first.

In Figure 5a, we see the RC circuit, which is assumed to be noiseless and initially fully discharged ('reset'). The white noise current i_n is modeled by parameter $R_{n,I}$ (see Figure 5a; note this is an *equivalent noise resistance*, not an impedance like R; only in specific cases it will be equal to R). Current i_n is fed to the RC network during switch conduction time t_{sw}. The resulting variance of the noise voltage across the capacitor can be written as [2]:

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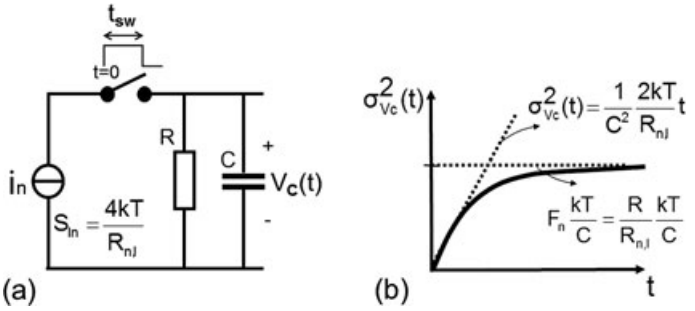

Figure 5. a) Equivalent circuit for noise calculations; b) Variance of the capacitor voltage noise.

$$\sigma^2_{Vc}(t) = F_n \frac{kT}{C}\left(1 - e^{\frac{-2t}{RC}}\right) \qquad \begin{cases} t << RC \\ \quad \approx \quad F_n \dfrac{kT}{C}\dfrac{2t}{RC} = \dfrac{1}{C^2}\dfrac{2kT}{R_{n,I}} \\ t << RC \\ \quad \approx \quad F_n \dfrac{kT}{C} = \dfrac{R}{R_{n,I}}\dfrac{kT}{C} \end{cases} \qquad 0 \le t \le t_{sw} \qquad (1)$$

$$F_n = \frac{R}{R_{n,I}}$$

where k is the Boltzmann constant, T is the absolute temperature and F_n is a dimensionless 'excess noise factor', equal to the ratio of the resistance R and the equivalent noise resistance $R_{n,I}$, i.e. $F_n = R / R_{n,I}$. If the noise current is caused by the same resistance with which it is filtered (e.g. in Figure 1), the noise excess factor will be unity.

Figure 5b contains a plot of (1), in which we see that it takes some time before the variance of the capacitor voltage reaches its steady-state value. Only after sufficient time, and if $F_n = 1$, the well-known value kT/C arises. Intuitively, this steady-state results because, for a given time interval, the current source on average adds the same amount of noise charge to the capacitor as the resistor removes (charging and discharging noise contributions are then in equilibrium).

2.3. Minimum period jitter of the oscillator

We will now calculate the minimum period jitter of the relaxation oscillator of Figure 4. In this calculation, we presume that the noise sources can be considered small signal and that the oscillator has reached a PSS. As motivated in the introduction, we only consider noise sources that cause $1/f^2$ colored phase noise. The period jitter is calculated by accumulating the charge noise contributions to the main capacitor over a nominal oscillation period and converting the resulting voltage variance to time variance via the slew rate [9]. For a rising edge which produces an output edge, we find:

$$\sigma_j^2 = \frac{\sigma^2_{V_{C1,tot}}}{\left(\frac{dV_{C1}}{dt}\right)\Big|_{V_{C1}=V_m}} = \frac{\sigma^2_{V_{C1,tot}}}{\left(\frac{I_1}{C_1}\right)} = \frac{\sigma^2_{Q_{C1,tot}}}{I_1^2} \qquad (2)$$

The *minimum* period jitter of the oscillator will now be derived applying this to the topology in Figure 4, where the jitter contributions of interest are the white noise sources of the charging current source I_1, the discharging current source I_2, the comparator cmp_{osc} and the one-shot.[§] The first two contributions are functionally required for timing and will fundamentally limit phase noise. We will show later that the latter two contribution can be eliminated. Evaluating (1) for I_1 and I_2 noise contributions to V_{C1} gives:

[§]Comparator/buffer cmp_{out} is 'outside the loop', and its noise is not integrated by the oscillator itself, i.e. does not contribute $1/f^2$ phase noise.

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$$\sigma^2_{V_{C1,I1}} \geq \frac{1}{C_1^2}\frac{2kT}{R_{n,I1}}T_{osc}$$
$$\sigma^2_{V_{C1,I2}} \geq \frac{1}{C_1^2}\frac{2kT}{R_{n,I2}}T_{pulse} \quad (3)$$

where $R_{n,I1}$ and $R_{n,I2}$ are the equivalent noise resistances of current source I_1 and I_2, respectively (see also Appendix B). Note that the charging current source I_1 contributes noise during the entire oscillation period T_{osc}, while the discharging current source I_2 contributes only during T_{pulse}. Note also that the upper approximation in (1) becomes exact for a relaxation oscillator containing an *ideal* current integrator, i.e. for $R \to \infty$ [2]. As the contributions in (5) are uncorrelated, the total accumulated voltage noise variance can be written as:

$$\sigma^2_{V_{C1,tot}} \geq \sigma^2_{V_{C1,I1}} + \sigma^2_{V_{C1,I2}} \geq \frac{1}{C_1^2}\left(\frac{2kT}{R_{n,I1}}T_{osc} + \frac{2kT}{R_{n,I2}}T_{pulse}\right) \quad (4)$$

In Appendix B, we show that for constant current I, reducing noise in a current source requires more voltage headroom ΔV. Moreover, we show that practical MOS-current sources are noisier than a linear resistance, i.e. $R_{n,I} < \Delta V / I$, so that the latter equation should be used for deriving a (best case) theoretical FoM limit. Doing so, using (4) and $Q = C \cdot V$, the total accumulated charge noise variance in $[C^2]$ becomes:

$$\sigma^2_{Q_{C1,tot}} = C_1^2\sigma^2_{V_{C1,tot}} \geq 2kT\left(\overbrace{I_1 T_{osc}}^{=Q_{in}}\frac{1}{\Delta V_1} + \overbrace{I_2 T_{pulse}}^{=Q_{out}}\frac{1}{\Delta V_2}\right) \quad (5)$$

where ΔV_1 and ΔV_2 are the voltage headroom 'reserved' to realize current source 1 and 2 (see Figure 4).

As PSS oscillation implies $Q_{in} = Q_{out}$, the accumulated charge variance (5) can be written as:

$$\sigma^2_{Q_{C1,tot}} \geq 2kTI_1 T_{osc}\frac{\Delta V_1 + \Delta V_2}{\Delta V_1 \Delta V_2} \quad (6)$$

Introducing an 'effective reserved voltage headroom' ΔV_{eff}:

$$\Delta V_{eff} = \frac{\Delta V_1 \Delta V_2}{\Delta V_1 + \Delta V_2} \quad (7)$$

and combining (2), (6) and (7), the relative period jitter variance can be written as:

$$\frac{\sigma_J^2}{{T_{osc}}^2} = \frac{\sigma^2_{Q_{C1,tot}}}{(I_1 T_{osc})^2} \geq \frac{2kTf_{osc}}{\Delta V_{eff} I_1} \quad (8)$$

We see here that the period jitter due to noise from current sources, expressed as a fraction of the period time, is fundamentally limited by oscillation frequency, the value of the current and the effective voltage headroom available to realize the current sources. Clearly, high ΔV_{eff} is good for jitter and $1/f^2$ phase noise, maximizing headroom is crucial.

2.4. Minimum FoM

We can now also calculate the minimum FoM of the relaxation oscillator of Figure 4. In [3], it has been shown that:

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$$\frac{\sigma_J^2}{T_{osc}^2} = N_{osc} f_{osc} \tag{9}$$

where σ_J/T_{osc} is the relative period jitter exclusively caused by the white noise sources that translate into $1/f^2$ phase noise and where N_{osc} is the oscillator number, obtained from extrapolation of the $1/f^2$ phase noise to f_{osc} as indicated in Figure 2. Substituting (9) in (8), we get:

$$N_{osc} = \sigma_J^2 f_{osc} \geq \frac{2kT}{\Delta V_{eff} I_1} \tag{10}$$

Using (10), the FoM in Figure 2 on linear scale becomes:

$$FoM = \sigma_J^2 f_{osc} \frac{P_{core}}{1mW} \geq \frac{2kT}{\Delta V_{eff} I_1} \frac{P_{core}}{1mW} \tag{11}$$

Unlike the oscillator number, the FoM is typically bound by thermodynamics. Thus, one can define a minimum FoM: FoM_{min}. As $P_{core} = V_{DD}\, I_{core}$, it can be written as:

$$FoM_{min} = \min(FoM) = \min\left(\frac{2kT}{1mW} \frac{V_{DD}}{\Delta V_{eff}} \frac{I_{core}}{I_1}\right) \tag{12}$$

As I_{core} includes I_1 by definition, the optimal case occurs for $I_{core} = I_1$. Given (7), we conclude that ΔV_{eff} is maximized when $\Delta V_1 = \Delta V_2 = V_{DD}/2$. As a result, the minimum FoM of the topology in Figure 4 can be written as:

$$FoM_{min} = 8 \frac{kT}{1mW} \quad [Hz^{-1}] \tag{13}$$

This corresponds to -165 dBc/Hz, the minimum value for I-C relaxation oscillators indicated in Figure 3. Taking the ratio of this minimum FoM and the actually achieved FoM results in the *oscillator design efficiency* [10]:

$$ODE = \frac{FoM_{min}}{FoM} \tag{14}$$

This oscillator design efficiency quantifies the quality of the oscillator design regarding its $1/f^2$ phase noise performance.[¶] This design efficiency can be written as:

$$ODE = \frac{FoM_{min}}{FoM} = \frac{1}{4} \frac{VDD}{\Delta V_{eff}} \frac{I_{core}}{I_1} \tag{15}$$

Both (12) and (15) are optimized if ΔV_{eff} is maximized. From the topology in Figure 4, we can observe that $V_{DD} = \Delta V_1 + \Delta V_2 + \Delta V_3$, in which ΔV_3 is the allowed voltage swing across the capacitor.[**] This leads to the counterintuitive conclusion that the *1/f² phase noise* performance FoM

[¶]In [1], the inverse of the oscillator design efficiency is called the 'wastefulness factor'. Note also that lower FoM is better.

[**]Note the difference between V_3 and ΔV_3 in Fig. 4: V_3 is the actual voltage across capacitor C_1 and ΔV_3 is the assigned voltage swing across capacitor C_1 (a design choice; $\Delta V_3 = \max(V_3) - \min(V_3)$).

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and ODE of the topology in Figure 4 is optimized if there is *no voltage swing* across the capacitor. For most types of oscillators, the oscillation amplitude is important for the $1/f^2$ phase noise performance, for instance in LC oscillators [11]. However, for this specific type of relaxation oscillator that contains an ideal current integrator, the oscillation (voltage) amplitude is unimportant for the $1/f^2$ phase noise performance. Inspecting (8) indicates why: it is the *ratio* of the *stochastic* and the *deterministic charge* contribution to the capacitor that matters. Capacitor size determines oscillation amplitude and the voltage headroom available for the current sources but *does not affect this charge ratio*. As N_{osc} and FoM are proportional to this charge ratio, while f_{osc} is cancelled combining (8) and (9), voltage swing nor capacitor size affects $1/f^2$ phase noise FoM and ODE.

However, there is more than $1/f^2$ phase noise. While in a phase locked loop, $1/f^3$ noise can often be suppressed to an insignificant level [4], this is not true for the wideband white noise floor. For a given oscillation frequency and waveform, a decrease in amplitude means a decrease in slew rate, degrading the phase noise floor caused by the *voltage-sensing* output comparator/buffer cmp_{out}. Once again, note that this 'output comparator/buffer' is *not* in the oscillator loop; hence, its decisions are not memorized and integrated to $1/f^2$ phase noise (white noise causes white phase noise floor). Minimizing the white noise floor means maximizing the slew rate across the capacitor, i.e. maximizing the swing ΔV_3 in Figure 4, which compromises the voltage headroom for current sources I_1 and I_2. We conclude that this particular circuit does not allow for simultaneous optimization of the $1/f^2$ and white phase noise. However, we will see in Section 3 that a change in topology does help.

2.5. Theoretical FoM limit equal to ring oscillator limit

The previous calculations show that the relaxation oscillator topology of Figure 4 has a theoretical FoM limit (13) which is in decibel equal to -165 dBc/Hz@290 K. This phase noise performance limit is 4 dB higher than that of the topology of Figure 1 [1]. To get an intuitive feel for this difference, note that the topology of Figure 4 acts as an *ideal* current integrator, whereas the topology of Figure 1 acts as a *leaky* current integrator, which 'forgets' part of the charge noise during operation. Interestingly, the phase noise performance limit of the circuit in Figure 4 is equal to that of ring oscillators [1].

2.6. Design strategy to approach the theoretical FoM limit

Based on the insight developed above, the following design strategy to optimize overall phase noise performance of a relaxation oscillator is proposed:

1. *Maximize both* $\Delta V_{eff}/V_{DD}$ *and* ΔV_3, i.e. maximize the voltage headroom reserved for the charging and discharging currents on the one hand (for $1/f^2$ noise), and the voltage swing across the capacitor on the other (for white noise). Choose a circuit topology that allows for independent optimization, or, if a trade-off exists, balance noise contributions.
2. *Maximize* I_1/I_{core} so that current is mainly spent for the fundamentally required charging function. *Remove* the avoidable phase *noise contribution of the loop-comparator* cmp_{osc}, which relaxes its bias current requirements. Moreover, as comparator delay now no longer affects the period of oscillation, this will *also improve frequency tuning linearity*, as in the sawtooth oscillator proposed in [2, 12, 13].

3. SWITCHED-CAPACITOR RELAXATION OSCILLATOR

We will now develop the switched-capacitor relaxation oscillator topology [7] step-by-step on the basis of the above design strategy. Afterwards we will show that expression (8) and this design strategy also hold for this new relaxation oscillator topology.

3.1. Step-by-step development

As a first step, take the topology of Figure 4 and replace the grounded capacitor by a charge-sensing amplifier (CSA), i.e. a charge-to-voltage converter as shown in Figure 6. The OTA in this CSA

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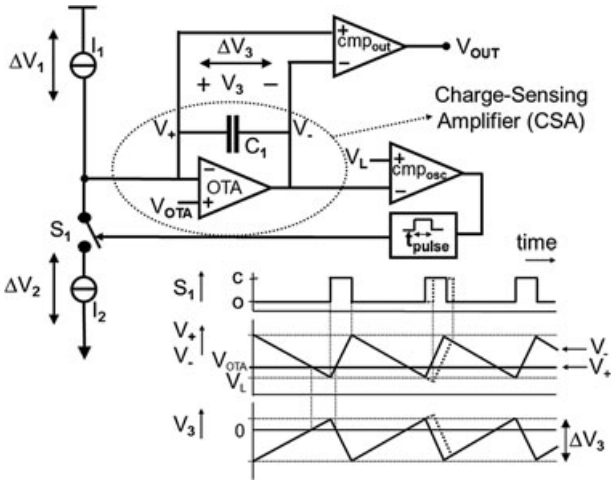

Figure 6. A grounded capacitor is replaced by a charge-to-voltage converter, so that ΔVeff = ΔV1 ΔV2 / (ΔV1 + ΔV2) and ΔV3 can be maximized simultaneously.

turns capacitor node V_+ into a virtual ground node biased to V_{OTA}. This means that $\Delta V_1 = V_{DD} - V_{OTA}$ and $\Delta V_2 = V_{OTA}$. Using (7), the maximum of $\Delta V_{eff}/V_{DD}$ is *1/4* and is reached by choosing $V_{OTA} = V_{DD}/2$. The charging current source I_1 is still charging the capacitor, but now via the OTA. As a result, the voltage at node V_- decreases linearly and when it crosses V_L, comparator cmp_{osc} issues a discharge signal. This signal activates the discharging mechanism which discharges the capacitor by a *fixed* amount of charge, again via the OTA. The allowed voltage swing across the capacitor can now be maximized as well, i.e. $\Delta V_3 \approx V_{DD}$. Note furthermore that the output comparator/buffer cmp_{out} does not need an additional reference voltage now (which can be noisy) as the capacitor voltage can be sensed differentially. This intermediate topology allows maximizing $\Delta V_{eff}/V_{DD}$ and ΔV_3 simultaneously (goal 1 in Section 2.6).

As a second step, observe that the combination of current I_2 and one-shot time t_2 effectively removes a charge packet I_2t_2 from capacitor C_1. Realizing an accurate one-shot time is a challenge especially with low jitter. However, the discharge charge packet can also be implemented by a (switched-) capacitor in combination with the OTA, as shown in Figure 7.

The operation of this discharging mechanism is as follows. At the beginning of the oscillation period, capacitor C_2 is discharged to ground. When comparator cmp_{osc} issues signal X (discharge C_1), capacitor C_2 is connected to node V_+ (virtual ground node of the OTA) and is charged from 0 to V_{OTA} by current source I_1 together with the OTA. During this action, capacitor C_1 is discharged

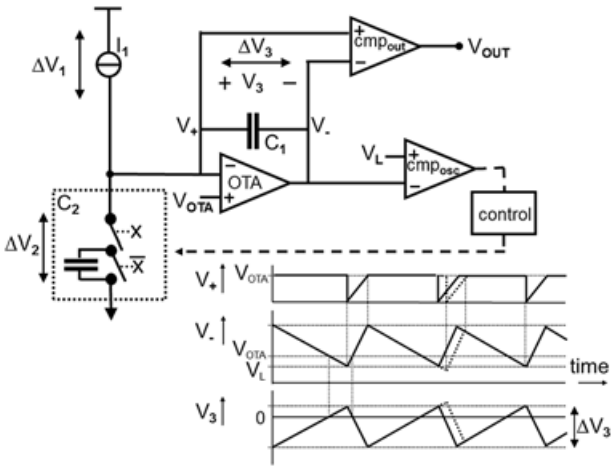

Figure 7. Alternative discharging mechanism by a switched capacitor, which does not require an accurate one-shot time (current-limited OTA assumed for constant slopes).

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by *a fixed* charge packet of C_2V_{OTA}. Still, as for Figure 4, the noise of comparator cmp_{osc} does not matter (see Figure 7).

Although the switched-capacitor topology does not contain a one-shot, it does contain an additional OTA (which can be noisy as well). In Section 4, we will show that part of the noise of this OTA is prevented to translate into colored $1/f^2$ phase noise by the settling/filtering of capacitor C_2. In Appendix C, it is shown that the minimal phase noise contribution of this switched-capacitor discharging mechanism is equal to that of the original discharging mechanism so that expression (8) and the design strategy of Section 2.6 still applies. Voltage ΔV_2 can now be interpreted as the allowed voltage swing across capacitor C_2. Note that for the topology of Figure 7 still $\Delta V_1 = V_{DD} - V_{OTA}$, $\Delta V_2 = V_{OTA}$ and $\Delta V_3 \approx V_{DD}$ holds, just like for Figure 6.

A final improvement step is to reverse the switched-capacitor instead of discharging it to ground, see Figure 8. When comparator cmp_{osc} issues a discharge signal, a divide-by-two is toggled (toggle control block) and capacitor C_2 is reversed. C_2 is now charged from $-V_{OTA}$ to $+V_{OTA}$ by current source I_1 and the OTA and capacitor C_1 is discharged by a fixed discharge packet of $2C_2V_{OTA}$ (doubled compared to Figure 7). This means that $\Delta V_1 = V_{DD} - V_{OTA}$, $\Delta V_2 = 2V_{OTA}$ and $\Delta V_3 \approx V_{DD}$, i.e. this final topology allows for doubling ΔV_2 and hence $\Delta V_{eff} / V_{DD}$ *without increasing current consumption* (C_1-discharge time defines the required current, to maintain voltage waveforms of Figure 7, C_2 needs to be halved for Figure 8).

In Section 4, we will show how a switched-capacitor relaxation oscillator can be implemented without much overhead, but first we coarsely estimate performance.

3.2. *Comparison of typical phase noise performance*

To get some feeling for the practical achievable phase noise performance, consider Figure 4 and assume V_{DD} is equally divided over charging, discharging and signal swing, i.e. $\Delta V_1 = \Delta V_2 = \Delta V_3 = V_{DD}/3$, so $\Delta V_{eff} / V_{DD} = 1/6$. The current consumption is at least $I_{core} = I_1$, which *does not* include the current consumption of the one-shot.

For the topology of Figure 8, as $\Delta V_1 = V_{DD} - V_{OTA}$ and $\Delta V_2 = 2V_{OTA}$, the maximum of ΔV_{eff} occurs for $V_{OTA} = (\sqrt{2} - 1)V_{DD}$. A close choice for the OTA reference voltage, which is still nearly optimal and gives easy comparison numbers is $V_{OTA} = V_{DD}/3$. A practical OTA circuit would furthermore limit the swing across capacitor C_1, e.g. to $\Delta V_3 = 2V_{DD}/3$. This would mean $\Delta V_1 = \Delta V_2 = \Delta V_3 = 2V_{DD}/3$, so $\Delta V_{eff} / V_{DD} = 1/3$. If the OTA is class-A and is able to discharge C_1 in the same time it is charged, an OTA bias current equal to I_1 is required, i.e. the total core current consumption is at least $I_{core} = 2I_1$. Note that this *does* include all the dominant sources of current consumption, in contrast to the one-shot case in Figure 4.

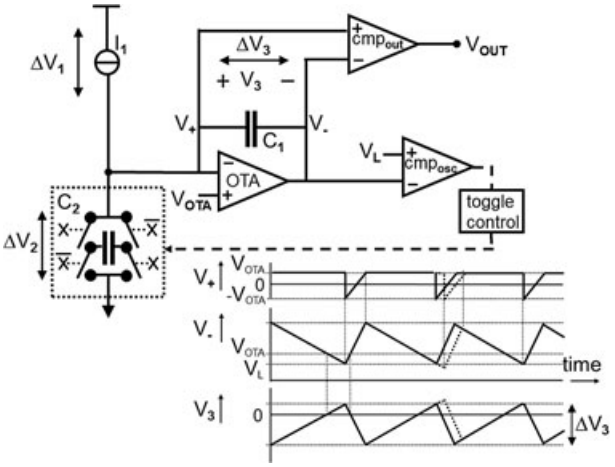

Figure 8. Switched-capacitor oscillator in which C2 is reversed (flipped) to increase ΔVeff (OTA is current limited).

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Comparing the above predicted phase noise of the two circuits, neglecting the one-shot contribution, we find an equal FoM = −163 dBc/Hz at 290 K, which is indeed close to the theoretical best value of −165 dBc/Hz (Figure 3). However, to make the phase noise contribution of the one-shot in the topology of Figure 4 insignificant, its current consumption will be significant, seriously degrading FoM. This in contrast to the calculation for Figure 8 in which we already accounted for OTA-current. From a FoM perspective, the situation is now somewhat similar to ring oscillators, where the 'inverter' transistors not only implement the charging and discharging function, but also the toggling between the two states. Thus, there is no additional noise for this 'comparator' function as for the circuit in Figure 8.

4. TRANSISTOR IMPLEMENTATION

To demonstrate in practice that we can come close to the theoretical minimum FoM of −165 dBc/Hz for I-C relaxation oscillators (13), we will now design a transistor circuit implementation. Figure 9 shows a transistor implementation of the switched-capacitor relaxation oscillator topology of Figure 8. Component values are equal to the case described in Section 3.2, i.e. $\Delta V_1 = \Delta V_2 = \Delta V_3 = 2V_{DD}/3$, meaning $\Delta V_{eff} = V_{DD}/3$. The frequency control linearity and output resistance of current source I_1 should both be high, and it is therefore implemented by a long PMOST that is heavily resistively degenerated. The voltage across the resistor is approximately $V_{R1} = V_{DD}/2$, and the drain-source voltage is $\Delta V_1 - V_{R1} = V_{DD}/6$. This thick gate-oxide PMOST allows for both setting $V_{DSsat} = V_{DD}/6$ and $V_{TUNE} = V_{DD}$ at the maximum oscillation frequency. The noise performance of this current source approaches that of a linear resistance. To tune the oscillation frequency, we change V_{TUNE}, i.e. we implement a voltage-controlled oscillator. However, reducing V_{TUNE} significantly deteriorates the noise performance as we use less ΔV ('throw away' available headroom). Noise performance could be maintained by splitting current source I_1 into many small current sources, all biased at $V_{TUNE} = V_{DD}$, selecting them digitally (digitally controlled oscillator).

To reduce power consumption during charging, the NMOST in the OTA implementation is biased exclusively by current source I_1 through C_1 such that $V_{GS} = V_{OTA} = \Delta V_2/2 = V_{DD}/3$. Only when V_- crosses $V_L = V_{DD}/6$ and comparator cmp_{osc} issues a C_1-discharge signal, current source I_2 in the OTA, implemented by a PMOST, is on for activation time $T_{act} < T_{osc}$. It supplies a *fixed* discharging current $I_2 = I_1 T_{osc}/T_{act}$. As T_{act} is independent of frequency and is not very critical, it was implemented by a fixed RC delay. Note that this RC delay does not have to be accurate as opposed to the pulse width of the one-shot. To allow $\Delta V_3 = 2V_{DD}/3$, both the NMOST and PMOST (realizing I_2) in the OTA are biased near weak inversion. Such a basic implementation of the CSA

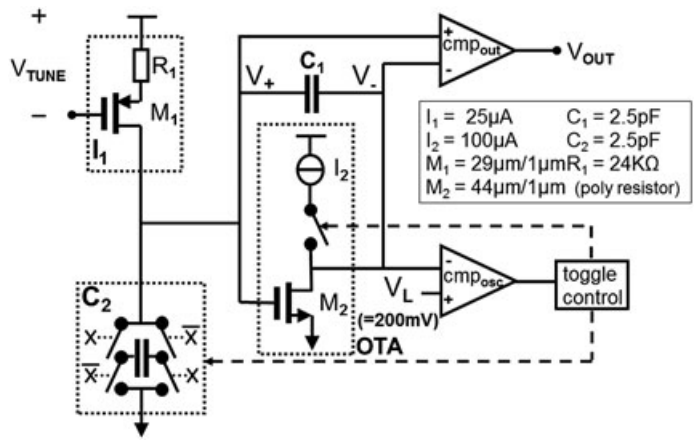

Figure 9. Implementation of the switched-capacitor relaxation oscillator.

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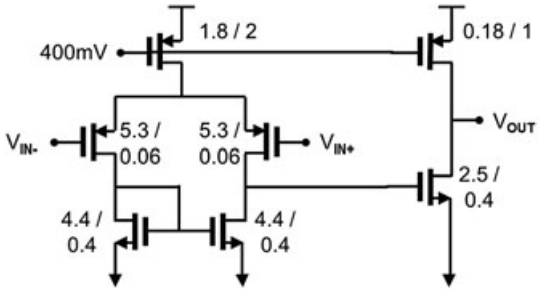

Figure 10. Transistor implementation of the oscillator comparator (cmp_{osc}).

has some attractive characteristics: it only consumes I_1, it results in a low excess noise factor and it has a low closed-loop input impedance ($1/g_{m2}$). This input impedance should be low such that the voltage on capacitor C_2 is allowed to settle accurately between the moment that current source I_2 is deactivated and the moment that capacitor C_2 is reversed again ($C_2/g_{m2} << T_{osc,min} - T_{act}$).

The non-linearity of the OTA, i.e. the non-linearity of the gate-source voltage of transistor M_2 versus I_1 in Figure 9, can largely compensate the non-linearity of the V_{TUNE}-I_1 relation (assuming square-law devices, they are inverse functions[‡]). Put differently, their effect on oscillation frequency is opposite: $Q_{in} = I_1(V_{TUNE})T_{osc} = Q_{out} = 2C_2V_{GS2}(I_1)$.

As mentioned briefly in Section 3, part of the noise of the OTA is prevented to translate into colored phase noise, namely the noise of I_2 contributed during discharging. To understand why, first note that T_{act}, the activation time of current source I_2, is chosen small enough to allow the voltage on capacitor C_2 to fully settle to $V_{GS2}(I_1)$ during the rest of the oscillation period T_{osc}-T_{act}. During this settling, the noise charge contribution on C_1 originating from discharge current I_2 has enough time to leak away (via the closed-loop input impedance). By the time capacitor C_2 is reversed again, its contribution to the $1/f^2$ colored phase noise can be negligible. This means that only the noise of the NMOST in the OTA implementation contributes to $1/f^2$ colored phase noise as further detailed in Appendix C.

We will now calculate the process technology and application-specific dimensioning. The available 65 nm CMOS process sets $V_{DD} = 1.2$ V. As we aim to demonstrate low phase noise at high power efficiency, we aim for a low-frequency application in which the required power is set by noise requirements, and not by speed requirements. The target application that we used as a proof-of-concept application (a digital audio application) sets $f_{osc,max} = 12.5\,MHz$ and $N_{osc} = -151\,dBc/Hz$ at 290 K, which is equivalent to about $100\,ppm$ relative period jitter. According to (10), this results in $I_1 = 2\,kT/(\Delta V_{eff}\ N_{osc}) = 25\,\mu A$. PSS furthermore implicates $Q_{in} = I_1\ T_{osc} = Q_{out} = C_2\Delta V_2$, meaning $C_2 = I_1/(f_{osc}\Delta V_2) = 2.5\,pF$. We choose $T_{act} = 1/(4\,f_{osc,max}) = 20\,ns$ to allow sufficient time for the settling of capacitor C_2, even at the maximum oscillation frequency. This results in $I_2 = I_1T_{osc}/T_{act} = 100\,\mu A$. Finally, we set ΔV_3 by choosing $C_1 = (\Delta V_2/\Delta V_3)C_2 = 2.5\,pF$.

The oscillator comparator and its reference are designed to consume about 10 μA and 5 μA, respectively. Figure 10 shows the transistor implementation of the oscillator loop-comparator (cmp_{osc} in Figure 9). The output comparator/buffer is designed to drive 50 Ω phase noise measurement equipment and therefore consumes about 2.5 mA, but this could be reduced to 10 μA if we would drive an on-chip inverter chain. The circuitry to switch I_2 and reverse C_2 reliably consumes about 5 μA. As a result, $I_{core} = 70\,\mu A = 2.8I_1$. According to (11), the FoM is expected to be −161.7 dBc/Hz at 290 K. In terms of the oscillator design efficiency in (14), this means ODE = −4 dB, i.e. this implementation of the topology of Figure 8 shows a $1/f^2$ phase noise performance that is only 4 dB from its theoretical limit. Further simulation results will now be presented in Section 5 as well as measurement results.

5. IC IMPLEMENTATION AND MEASUREMENTS

We will now discuss measurements that demonstrate correct functional operation of the oscillator and a noise performance close to the theoretical prediction. Figure 11 shows the baseline 65 nm LP CMOS

[‡]Only during chip measurements we realized this linearization exists but we did not design for it.

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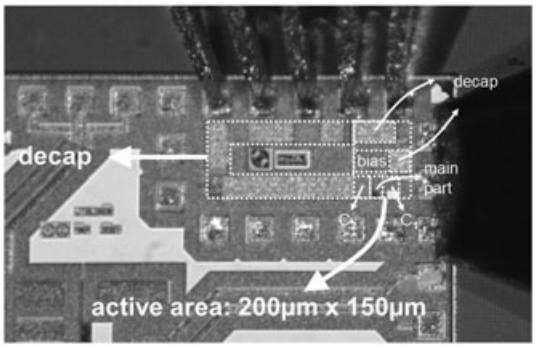

Figure 11. Die micrograph of baseline 65 nm LP CMOS design.

implementation of the switched-capacitor relaxation oscillator of Figure 9. The circuit is measured using a battery supply and probes. Figure 12 and Figure 13 show the simulated and measured waveforms, respectively.

These waveforms differ somewhat, and detailed analysis shows this is because current source I_2 is active for somewhat less than $T_{osc}I_1/I_2$. This can be easily corrected in a re-design and hardly affects the phase noise performance.

Figure 14 shows that the frequency tuning range is both large and linear: 1–11 MHz. Measured frequencies are slightly lower than simulated.

In Figure 15, the simulated phase noise is plotted, at the maximum frequency $f_{osc} = 11.2$ MHz for $V_{DD} = 1.2$ V. In the center of the $1/f^2$ region, we find L(100 kHz) = −109 dBc/Hz at 60.5 µA@1.2 V. Substitution in (22) renders a FoM of −161.4 dBc/Hz at 290 K, which is very close to the −161.7 dBc/Hz predicted in Section 2.5. The simulated $1/f^3$ corner frequency is about 10 kHz.

Figure 16 provides a detailed summary of the contributors to the simulated phase noise. At 100 KHz, nearly all the $1/f^2$ phase noise is indeed caused by the charging and discharging mechanisms, and only a few % by the loop-comparator. Explorative simulations have shown that the jitter produced by the same comparator, when applied in the traditional oscillator of Figure 1 without the 'trick' of Figure 4, would add more $1/f^2$ phase noise than all other noise sources together. The fact that the loop-comparator has high noise is still evident from its high contribution to the white-noise phase noise floor at 1 MHz (last column in Figure 16; 66.37% contribution).

Figure 17 shows the measured output spectrum at 12 MHz measured with a 1.28 V battery. Using the data a 100 kHz offset frequency, the FoM is −161 dBc/Hz, which fits well to both theory and simulation results mentioned in the previous paragraph. Figure 18 shows how this FoM varies over

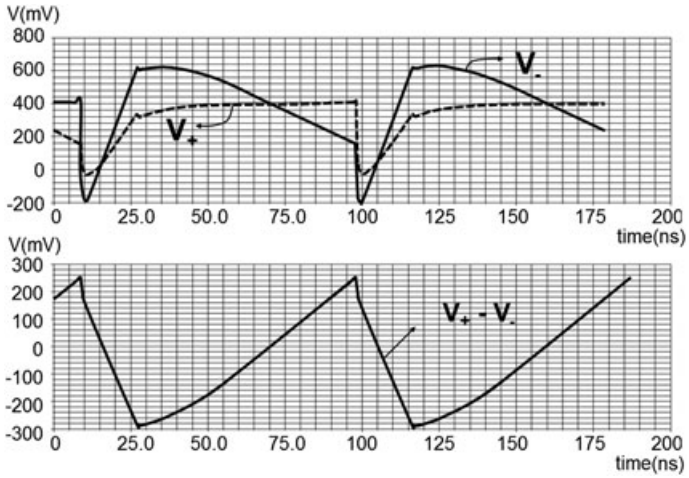

Figure 12. Simulated waveforms for the oscillator in Figure 9.

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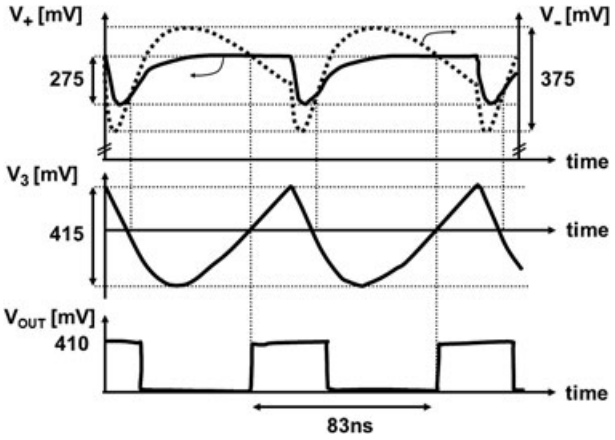

Figure 13. Measured waveforms for the oscillator in Figure 9.

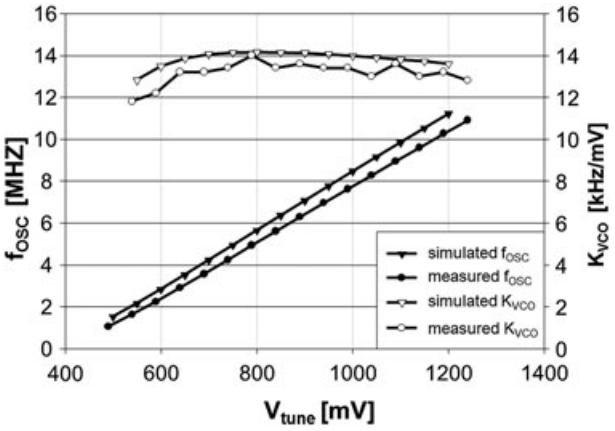

Figure 14. Simulated and measured frequency tuning range and frequency tuning gain (R&S FSP spectrum analyzer).

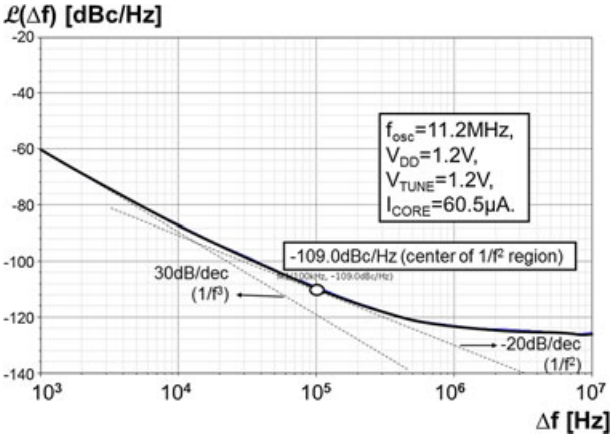

Figure 15. Simulated phase noise spectrum with $1/f^2$ and $1/f^3$ asymptotes.

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	contributor	£(1K) (%)	£(10K) (%)	£(100K) (%)	£(1M) (%)
charge	R1 - flicker	0.74	0.38	0.06	~ 0
	R1 - thermal	4.12	20.61	33.92	9.03
	M1 - flicker	43.76	22.42	3.60	0.10
	M1 - thermal	0.57	2.85	4.69	1.24
discharge	M2 - flicker	39.14	20.07	3.26	0.11
	M2 - thermal	4.08	20.37	33.30	9.03
	switches C2 - thermal	1.72	8.55	13.96	3.88
cmp_{osc}	cmp_{osc} - flicker	4.28	2.22	0.74	1.35
	cmp_{osc} - thermal	0.30	1.53	5.03	66.37
	bias cmp_{osc} - thermal	0.05	0.19	0.67	7.03
	rest	1.29	0.81	0.77	1.86
	total	**100**	**100**	**100**	**100**
		(1/f3 region)	*(transition)*	*(1/f2 region)*	*(white floor)*

Figure 16. Simulated phase noise summary.

the tuning range. The FoM deteriorates for lower oscillation frequencies as expected, as discussed in the first paragraph of Section IV. Ten samples have been measured, and all have similar FoMs. This FoM is only 4 dB from the theoretical limit of this topology and to date still is the best reported one as shown in Figure 19 (although more recent designs are quite close). It is also similar to that of state-of-the-art ring oscillators [1] (see also Figure 3).

6. CONCLUSIONS

We have shown that the comparator in a relaxation-oscillator loop can be prevented from contributing to $1/f^2$ colored phase noise and degrading control linearity. We described a relaxation oscillator topology that does this in a power-efficient way, leaving only the white noise of the charging and the discharging mechanism to contribute significantly to $1/f^2$ phase noise. We derived simple though precise expressions that predict the theoretical phase noise performance limit of these relaxation oscillators and proposed a design strategy to approach this limit.

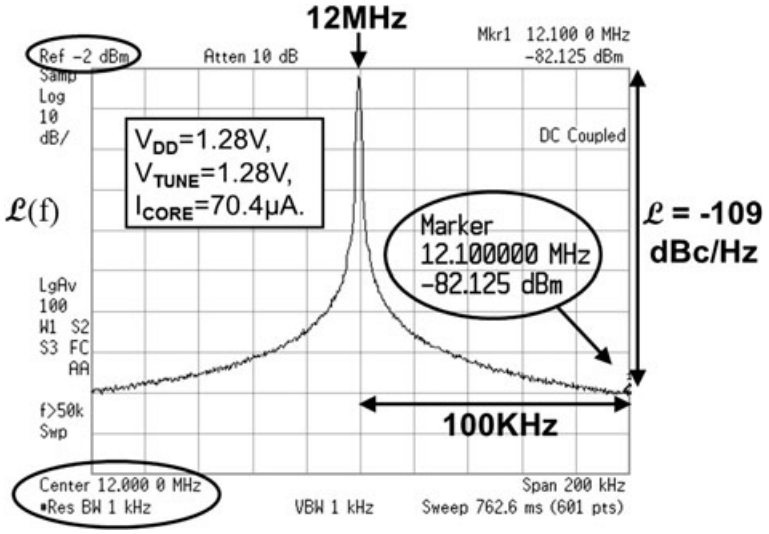

Figure 17. Measured output spectrum (Agilent E4440A).

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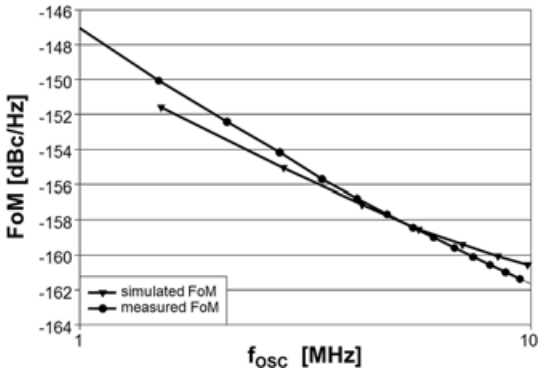

Figure 18. Simulated and measured phase noise FoM (evaluated in the 1/f2 region) versus oscillation frequency.

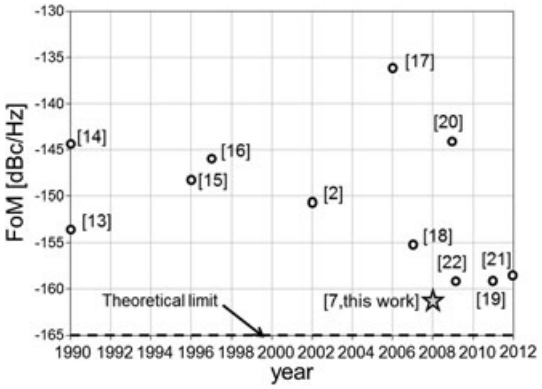

Figure 19. Phase noise FoM of previous relaxation oscillator designs.

A 65 nm CMOS implementation shows a large and linear frequency tuning range of 1–11 MHz. The phase noise FoM is −161 dBc/Hz at room temperature, only 4 dB from the theoretical limit of this topology. This FoM is similar to that of state-of-the-art ring oscillators, but this relaxation oscillator also features a linear control characteristic.

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7. APPENDICES

APPENDIX A
Jitter and phase noise metrics

Timing uncertainty or frequency instability can be described in different ways and can be related to each other under certain condition that we will summarize briefly here. Suppose we compare an ideal zero-jitter clock with a practical jittery one, where timing deviations compared to the ideal clock are denoted Δt. Three common jitter metrics are now: *absolute* jitter σ_A, *period* jitter σ_J and *adjacent*

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period jitter $\sigma_{\Delta J}$ [23]. These refer to the standard deviation of these zeroth, first and second-order differences, respectively:

$$\sigma_A \sqrt{E\left[(\Delta t)^2\right]} \tag{16}$$

$$\sigma_J = \sqrt{E\left[(\Delta t_N - \Delta t_{N-1})^2\right]} \tag{17}$$

$$\sigma_{\Delta J} = \sqrt{E\left[((\Delta t_{N-1}) - (\Delta t_{N-1} - \Delta t_{N-2}))^2\right]} \tag{18}$$

where index N identifies the N-th timing deviation, i.e. the N-th threshold-crossing. Period jitter is sometimes also called cycle jitter and adjacent period jitter also cycle-to-cycle jitter. Although these jitter metrics are very useful in the time domain, they do not provide much information regarding the spectral distribution or single-sideband phase noise $S_\phi(f)$. As measuring the amplitude power spectral density $S_X(f)$ is often easier, the single-sideband metric L(f) is commonly used, which can be related to $S_X(f)$, power of the carrier P_s and phase noise as:

$$L(f) = \frac{S_x(f_c + f)}{P_s} \approx \frac{S_\Phi(f)}{2} \tag{19}$$

where the approximation holds for $f_{crL} << f << f_c$ [5], in which f_{crL} is the linewidth of the oscillator and f_c the oscillation frequency. As motivated in the introduction, the $1/f^2$ noise often dominates, in which case [5]:

$$\frac{\sigma_J^2}{T_{osc}^2} = N_{osc} f_{osc} \tag{20}$$

where T_{osc} is the period of oscillation and σ_J / T_{osc} is the relative period jitter *exclusively caused by the white noise sources* that translate into $1/f^2$ phase noise, and where N_{osc} *is the oscillator number* [5]:

$$N_{osc} = L(f_{f\text{-}2}) \left(\frac{f_{f\text{-}2}}{f_{osc}}\right)^2 \tag{21}$$

where f_{f-2} is equal to a frequency offset somewhere in the $1/f^2$ region (see Figure 2) and f_{osc} is the oscillation frequency. The oscillator number can be thought of as an extrapolation of the $1/f^2$ region at an offset frequency equal to the oscillation frequency, see Figure 2. The oscillator number specifies the $1/f^2$ phase noise behavior and provides an indication of how difficult it is to achieve, by normalizing for offset and oscillation frequency. It can also be shown that the oscillator number is equal to the phase diffusion coefficient associated with white noise, i.e. c_w in [5].

Normalizing the oscillator number to the power consumption of the oscillator core P_{core} (excluding auxiliary output buffers) renders the well-known FoM [5, 6]:

$$FoM = L(f_{f\text{-}2}) \left(\frac{f_{f\text{-}2}}{f_{osc}}\right)^2 \frac{P_{core}}{1mW} = N_{osc} \frac{P_{core}}{1mW} \tag{22}$$

This FoM quantifies the oscillator's $1/f^2$ phase noise performance, taking into account power consumption. We will use this for benchmarking the oscillators. The ratio of the performance of a given oscillator topology (*FoM*) and the target phase noise specification (N_{osc}) gives an indication of the necessary power consumption (P_{core}).

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APPENDIX B
Noise behavior of practical CMOS current sources

Relaxation oscillators require a charge current which also produces noise. In this section, we model the noise performance of a resistor and MOS transistor (MOST)-based current source and relate it to the bias current I and voltage headroom ΔV. We will show that for a fixed bias current, lowering noise requires more voltage headroom ΔV and that the resistor achieves the best noise performance.

For a simple resistor R with only thermal noise, the equivalent noise resistance $R_n = R$, which is also equal to $R_n = \Delta V / I$. The equivalent current noise of this resistance is:

$$\sigma^2_{I,Rn} = \frac{4kT}{R_n}\Delta f = \frac{4kT \cdot I}{\Delta V}\Delta f \tag{23}$$

For a MOST in strong inversion with a square-law characteristic, the noise current variance can be written in the following form [24]:

$$\sigma^2_{I,thermal} = 4kT\gamma \cdot g_m \Delta f = 4kT\gamma \frac{2I_D}{V_{GT}}\Delta f \geq 2\gamma \frac{4kT \cdot I}{\Delta V}\Delta f \tag{24}$$

With γ=2/3 for a long channel transistor, while practical sub-micron transistor typically shows a γ in the range of 1–1.5. To minimize noise current variance, we want a low g_m, which implies high V_{GT} and high headroom ΔV, if the current is fixed. The minimum voltage headroom to be reserved to keep a MOST in saturation is $\Delta V \geq V_{GT}$. Comparing (23) to (24), we conclude that the noise performance of such a current source implementation is at least 2γ times worse than (23). Furthermore, note that both (23) and (24) are proportional to $I/\Delta V$, i.e. for a fixed bias current, lowering noise requires more voltage headroom.

For a MOST in weak inversion, a few times kT/q is needed as voltage headroom and the noise due to shot noise is:

$$\sigma^2_{I,Shot} = 2qI\Delta f = 4kT\frac{qI}{2kT}\Delta f \tag{25}$$

This noise performance is only better than (23) if $\Delta V < 2\,kT/q$, but for such a low ΔV the MOST in weak inversion does work as current source. Note furthermore that this conclusion also holds for a current source consisting of a BJT. If more voltage headroom that 2 kT/q is available, it is a good idea to resistively degenerate the above transistor implementations of a current source.[§§] The noise performance of such a current source implementation would still ultimately be limited by the degeneration resistance though and will not be lower than (23). Thus, we conclude that (23) renders the best case noise, i.e. if we want to lower noise for a current source with current I, we need to 'reserve more voltage headroom ΔV'. As (23) renders the best case noise, it constitutes a good basis for deriving fundamental limits in phase noise of current-source based oscillators.

APPENDIX C
Switched-capacitor relaxation oscillators

We will now show the validity of the derived phase noise expressions for the switched-capacitor relaxation oscillator topology of Figure 7. As the charging mechanism is still implemented by current source I_I, the noise variance of the charging mechanism is still given by the upper part of (1). Hence, we only have to show that the minimal phase noise contribution of the switched-capacitor discharging

[§§]Note that this also increases output resistance and lowers 1/f noise of the current source, as resistors show much lower 1/f noise than MOSFETs.

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mechanism in Figure 7 is equal to that of the original discharging mechanism, i.e. current source I_2 in Figure 4. This is done, by applying (1) of Section 2 three times.

At the beginning of an oscillation period, the switched-capacitor C_2 is reset to ground via a resistive switch which is on for sufficient time to result in the steady-state voltage variance kT/C. Thus, $F_n = 1$ ($R_{n,I} = R$), and (1) converted to charge variance becomes kTC_2. After connecting C_2 to node V_+ and allowing the capacitor voltage sufficient time to settle to V_{OTA}, the additional charge noise variance due to the charging current noise becomes F_nkTC_2, in which the excess noise factor F_n depends on the specific implementation of the OTA. If we implement the OTA as shown in Figure 10, with a single transistor M_2, it can be considered as a noise current source as in the model of Figure 5. Treating it as other current sources, we again take $F_n = 1$ as the best case for the derivation of the fundamental FoM limit. Assuming the noise contributions are uncorrelated, the lower limit of total charge noise variance becomes two times kTC_2 plus the contribution of the charging mechanism:

$$\begin{aligned}\sigma^2_{Q_{C1,tot}} &\geq \frac{2kT}{R_{n,I1}} T_{osc} + 2kTC_2 = 2kT\left(\overbrace{I_1 T_{osc}}^{=Q_{in}} \frac{1}{\Delta V_1} + \frac{Q_{out}}{\Delta V_2} \right) \\ &= 2kTI_1 T_{osc} \frac{\Delta V_1 + \Delta V_2}{\Delta V_1 \Delta V_2}\end{aligned} \tag{26}$$

Where we again use the condition that $Q_{in} = Q_{out}$ for steady-state oscillation. This result is equal to (6), and we can then apply the theory of Section 2 also for this switched-capacitor relaxation oscillator. ΔV_1 and ΔV_2 now have the more general meaning of the voltage headroom reserved for the charging and discharging mechanism, respectively. Showing the validity of the used phase noise expressions for the switched-capacitor relaxation oscillator topology of Figure 8 is similar and results in (26) as well.

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