

## Anticipation of digital patterns

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### SUMMARY

A memristive device is a novel passive device, which is essentially a resistor with memory. This device can be utilized for novel technical applications like neuromorphic computation. In this paper, we focus on anticipation – a capability of a system to decide how to react in an environment by predicting future states. Especially, we have designed an elementary memristive circuit for the anticipation of digital patterns, where this circuit is based on the capability of an amoeba to anticipate periodically occurring unipolar pulses. The resulting circuit has been verified by digital simulations and has been realized in hardware as well. For the practical realization, we have used an Ag-doped  $\text{TiO}_{2-x}$ -based memristive device, which has been fabricated in planar capacitor structures on a silicon wafer. The functionality of the circuit is shown by simulations and measurements. Finally, the anticipation of information is demonstrated by using images, where the robustness of this anticipatory circuit against noise and faulty intermediate information is visualized. Copyright © 2016 John Wiley & Sons, Ltd.

KEY WORDS: memristive devices, anticipation, amoeba learning, neuromorphic computation, artificial intelligence

### 1. INTRODUCTION

Even unicellular organisms like amoebas exhibit astonishing behavioral capabilities. For example, initially motivated by foraging, the amoeba *Physarum polycephalum* is able to solve mazes and in particular geometrical puzzles [1, 2]. In an experiment, Saigusa et al. demonstrated anticipation in amoeboid organisms, which were exposed to periodic environmental events [3]. Herein, the organism learned a periodic shock event pattern and anticipated a further subsequent event, although the event was experimentally not applied. Anticipation is not restricted to cellular organisms and is understood as a very general concept in nature [4]. The various aspects of anticipation have been debated in numerous research fields as for example, natural sciences, social sciences, and engineering [4, 5]. A well-accepted definition of the term "anticipation" was given by Rosen and reads: *An anticipatory system*

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is a system containing a predictive model of itself and/or of its environment, which allows it to change at an instant in accord with the model's predictions pertaining to a later instant. Anticipation is not restricted to living species. Under the framework of bio-inspired engineering, anticipation is considered as an interesting approach, e.g. for cell-based robot controller or multi-agent robotics [6, 7]. The above-mentioned amoeba experiment by [3] was later modeled by [8] based on an electric resonance circuit comprising a memristive device. The model exhibited electronically essential features of the biological experiment. In 2012 anticipation, as inspired by the amoeba experiment, was realized experimentally [11]. In this work we present a compact memristive circuit for the anticipation of digital patterns, which extends the amoeba learning circuit [8] to an anticipatory system for bipolar signals. After a quantization procedure, this anticipatory system can be used for the anticipation of information represented by general bit patterns. This allows for a variety of possible applications, especially from the field of bio-inspired engineering.

## 2. The anticipation system

### 2.1. Anticipation circuit for analogue patterns

Anticipation events, as it has been observed in unicellular organisms like amoebas [3], was mimicked by a memristive resonance circuit [8] as shown in Fig. 1.

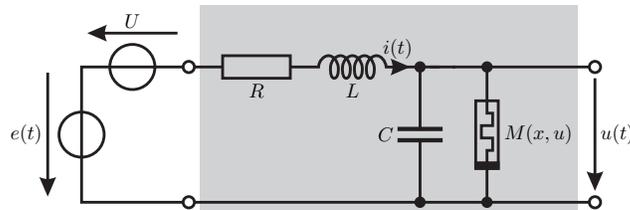


Figure 1. Anticipation two-port driven by two voltage sources, cf. [11].

The circuit comprises a series interconnection of two voltage sources, which supply an anticipation two-port (grey-shaded) with the signal  $e(t) + U$ . Here,  $e(t)$  is an information-bearing input voltage and  $U$  is a positive voltage offset. The anticipation two-port is a damped oscillator, including a resistance, a capacitance, an inductance, and comprises especially a memristive device [9, 10]:

$$u = M(x, u) i, \quad \frac{dx}{dt} = f(x, u). \quad (1)$$

The structural parameter  $x$  represents the memory behavior of the memristive device, and is itself a suited function of the applied voltage  $u$ . Independent of the specific function  $f$  the memristive device is due to its non-negative memristance  $M$  a passive one-port [9]. Due to the fact that only passive one-ports are port-wise interconnected via a Kirchhoff network, the anticipation two-port is itself passive.

Most of the memristive devices are based on ionic transport mechanisms [12] and are consisting of the layer sequence metal-insulator-metal. The memristive behavior is based on an ionic drift inside the insulator layer under the applied electrical field. In those devices,  $f$  is physically related to an ionic drift model [13]. To be more specific, here we have used an Ag/TiO<sub>2-x</sub>/Al memristive cell, where the device resistance varies according to the Ag drift/diffusion process. This switches the device resistance at the positive threshold voltage  $U_{\text{on}}$  from a high ohmic state  $M_{\text{off}}$  to a low ohmic state  $M_{\text{on}}$  and vice versa at the negative threshold voltage  $U_{\text{off}}$ , i. e. the memristance varies between the low and high ohmic state,

$$M_{\text{on}} \leq M(x, u) \leq M_{\text{off}}, \quad (2)$$

where  $x$  changes accordingly to the differential equation in (1). Below the threshold voltage  $U_{\text{on}}$  and above the threshold voltage  $U_{\text{off}}$  the memristive device behaves as a constant resistor.

For an electronic implementation of anticipation the circuit must process specific (periodic) input patterns by precisely adjusting the memristive device resistance and simultaneously leaving the resonant frequency unaffected [11]. This is an implicit task because the memristive device, in turn, must be adapted to the circuit oscillations evoked by the input pattern. An analytical description of the memristive anticipation two-port is hindered by the recursive dependency of the memristance  $M(x, u)$  from the state variable  $x$  and the voltage  $u$ , cf. [11]. Nevertheless, under the restriction of a constant memristance  $M$ , it is possible to get a general insight into the anticipation two-port functionality. Whereas in [11] one can find a steady-state analysis of the anticipation circuit, we will here investigate the transient behavior by analyzing the pulse response of the system, which is important for the anticipatory functionality of the system. To this end, we start with the system matrix and transfer function of the circuit,

$$\mathbf{A} = \begin{bmatrix} -R/L & -1/L \\ 1/C & -1/MC \end{bmatrix} \quad \text{and} \quad H(p) = \frac{\omega_0^2}{[p - \lambda][p - \lambda^*]}, \quad (3)$$

respectively [11]. Here,  $p$  is the complex frequency variable,  $\omega_0 = \frac{1}{\sqrt{LC}}$  is the resonance frequency of the ideal  $LC$ -circuit. The eigenvalues of this real damped oscillatory system are complex conjugate pairs  $\lambda_1 = \lambda_2^* = \lambda = -\gamma + j\omega_r$ , where

$$\gamma = \frac{\omega_0}{2} \left[ r + \frac{1}{m} \right], \quad \omega_r^2 = \omega_0^2 \left[ \frac{r}{m} + 1 \right] - \gamma^2, \quad \text{with } r = \frac{R}{Z}, \quad m = \frac{M}{Z} \quad \text{and } Z = \sqrt{\frac{L}{C}}. \quad (4)$$

As can be taken from the real and imaginary part, the memristance  $M$  affects the damping and the resonance frequency. Especially, these effects are minimal, when the memristive device is in a high ohmic state since  $r/m = R/M$  is much smaller than one. In this case the anticipation two-port is able to anticipate pulse trains matched to the resonance frequency

$$e(t) = -e_0 \sum_{\mu} q(t - t_{\mu}), \quad \text{with } q(t) = \begin{cases} 1 & \text{for } 0 \leq t \leq \frac{T_r}{2} \\ 0 & \text{otherwise} \end{cases}. \quad (5)$$

For a fixed memristance the response of the circuit to this pulse train reads:

$$u(t) = -e_0 \sum_{\mu} \text{Re} \left\{ \frac{2\omega_0^2}{[\lambda + R/L]^2 - \omega_0^2} \frac{\lambda + R/L}{\lambda} \left[ 1 - e^{-\lambda \frac{T_r}{2}} \right] e^{\lambda[t - t_{\mu}]} \right\}. \quad (6)$$

A detailed examination of this response shows that the pulses must have negative amplitude  $-e_0$  and ideally they should equally spaced by the resonant period  $T_r$ , with  $\omega_r T_r = 2\pi$ . Pulses at these instants lead to a constructive oscillating behavior where the output voltage  $u(t)$  has a high amplitude, which in turn indicates anticipation.

## 2.2. Anticipation circuit for digital patterns

The anticipation two-port is only able to anticipate pulses with negative amplitude, i. e. the anticipation is limited to unipolar signals. The aim of this section is to extend the circuit to bipolarity. For this purpose, the bits 0 and 1 are mapped to  $-e_0$  and  $+e_0$ , respectively:

$$e(t) = e_0 \sum_{\mu} x_{\mu} q(t - t_{\mu}), \quad \text{with} \quad x_{\mu} = \begin{cases} -1 & \text{for } b_{\mu} = 0 \\ +1 & \text{for } b_{\mu} = 1 \end{cases}, \quad (7)$$

where  $b_{\mu}$  denotes the bit associated with the instance  $t_{\mu}$ . In particular, a digital anticipator should allow for anticipating the bits by generating a tristate output signal, which indicates whether bit 1, bit 0 or nothing has been anticipated.

In order to anticipate positive pulse trains, one can modify the electrical circuit of Fig. 1 by interconnecting an ideal transformer with turns ratio  $1 : -1$  between the information bearing input voltage source  $e(t)$  and the rest of the circuit. Because of the sign inversion with respect to the voltages of the primary and secondary side of the transformer, this modification leads to an anticipator of positive pulses. Next, we can get rid of the ideal transformer by transforming the complete circuit on the secondary side. This solely results in a sign inversion of the constant voltage source  $U$  and an interchanged orientation of the memristive device.

A combination of both anticipation circuits leads to an electrical circuit layout as sketched in Fig. 2, where the left and right part anticipates positive and negative pulse trains, respectively. For this circuit, a negative pulse train will be anticipated by the right anticipator and yields an oscillating voltage  $u_0(t)$ . In contrast to this, a positive pulse train will be anticipated by the left anticipator, which results in an oscillating voltage  $u_1(t)$ . Hence, the circuit layout depicted in Fig. 2 is able to anticipate bipolar signals and will be called bit anticipator in the sequel.

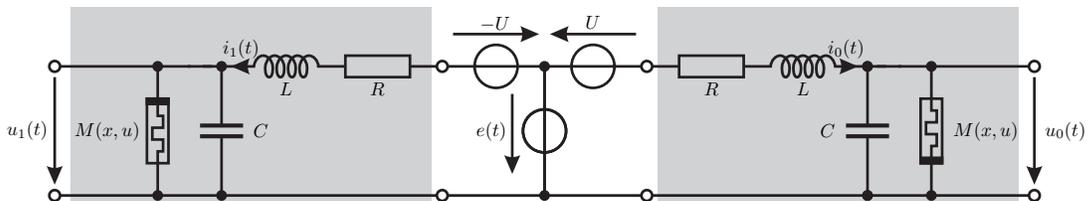


Figure 2. Bit anticipator circuit.

It remains to define the different logical states of the digital anticipator, which are tabulated in Fig. 3: The bit anticipator anticipates nothing if neither the left nor the right anticipator anticipates. It anticipates a 0 respectively a 1 if only the associated output voltage is oscillating. The situation is critical if both anticipators have an oscillating output signal because anticipating a bit 1 and a bit 0 simultaneously is obviously an error. This error can be treated in many ways. For instance, we can decide that the circuit ignores this case or both anticipators are reset to their initial states.

1 \ 0	nothing anticipated	anticipated
nothing anticipated	nothing anticipated	0 anticipated
anticipated	1 anticipated	error

Figure 3. Logical states for the anticipation of digital pattern.

### 3. Hardware design

In the following section, the technical realization of the bit anticipator is presented. In Sec. 3.1 fabrication issues and the resistive switching behavior of the used memristive devices are discussed, while Sec. 3.2 deals with the hardware design of the bit anticipator.

#### 3.1. Memristive Device

The key components of the anticipation circuit are memristive devices, which we have externally connected to the circuit board. The used memristive devices consist of the layer sequence Ag/TiO<sub>2-x</sub>/Al and are fabricated as planar capacitor structures on a Si-wafer with 400 nm of thermally oxidized SiO<sub>2</sub> by employing a standard optical lithography process. In detail, Ag is deposited by thermal evaporation. In a one-step lithography 50 μm × 50 μm contact windows are defined, followed by reactive ion sputtering of 10 nm TiO<sub>2-x</sub> and 5 nm Al. For the wiring 140 nm Al is deposited by thermal evaporation on top, while the device fabrication is completed by a subsequent lift-off in acetone.

The fabricated devices belong to the class of electrochemical metallization cells (ECM) for which the change in resistance is due to the formation and dissolution of electrically conducting paths in a transition metal oxide [12, 14]. On a macroscopic scale, the mechanism of resistive switching is typically illustrated as follows: Metal atoms from the active electrode are oxidized and drift/diffuse through the transition oxide layer towards the opposite electrode.

Here, they can be reduced and start clustering. Step by step conductive filaments are growing and binary bipolar resistive switching characteristics are obtained. In Fig. 4 two typical current-voltage characteristics (i-u-curves) for two individual Ag/TiO<sub>2-x</sub>/Al devices are shown where the connections to the external voltage source are interchanged in order to reach the requirements defined by (7). For this measurements, an Agilent E5260 source measurement unit was employed by sweeping the applied voltage and measuring the device current, simultaneously. Moreover, a current compliance of 100 μA has been set in order to avoid an electrical break down of the memristive cell. In particular, resistive switching from the initial high resistance state  $M_{\text{off}}$  to the low resistance state  $M_{\text{on}}$  is observed if a positive voltage is applied to the active Ag-electrode, cf. Fig. 4. For the back transition from the  $M_{\text{on}}$ -state to the  $M_{\text{off}}$ -state a negative voltage is required at the Ag-electrode. While  $M_{\text{off}}$  of the fabricated devices is in the range of several GΩ,  $M_{\text{on}}$  is approximately 10 kΩ. However, we would like to mention that the  $M_{\text{on}}$  can be varied by appropriate settings of the employed current compliance.

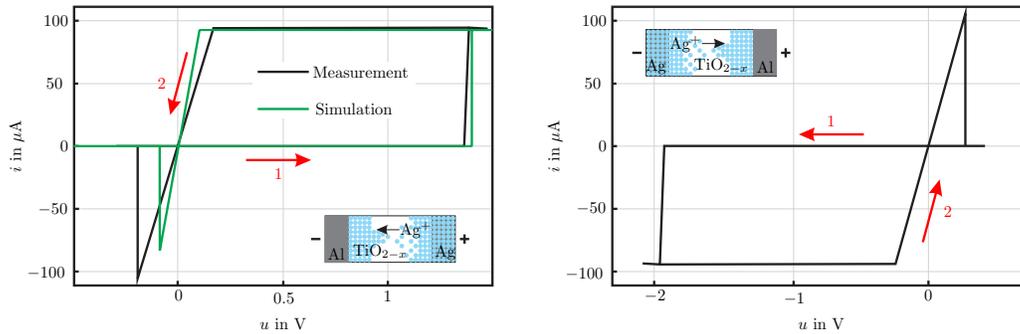


Figure 4. Typical current-voltage characteristics ( $i$ - $u$ -curves) of Ag-doped  $\text{TiO}_{2-x}$ -based memristive cells for different electrical connections. While in (left) negative and positive voltages are, respectively, applied through the left and right electrode, in (right) the device polarity is reversed. For the measurement a compliance current of  $100 \mu\text{A}$  has been used. Insets: Schematic of the layer sequence of the Al/ $\text{TiO}_{2-x}$ /Ag device indicating the electrical connection. For a comparison, the simulated curve of the memristive model used in simulations is also shown in the left figure (green).

In general, an important characteristic of ECM cells is that they feature threshold voltages  $U_{\text{on}}$  and  $U_{\text{off}}$  for the resistance set and reset process, respectively. Depending on the voltage source polarity the investigated memristive cells in Fig. 4 have different threshold voltages:  $U_{\text{on}} = 1.4 \text{ V}$ ,  $U_{\text{off}} = -0.2 \text{ V}$  (left) and  $U_{\text{on}} = -1.9 \text{ V}$ ,  $U_{\text{off}} = 0.2 \text{ V}$  (right). It is worth mentioning that the used class of memristive devices feature an inherent stochastic nature in which the threshold voltages reflect the local atomistic Ag drift/diffusion processes [14, 15]. Thus, such a device stochastically influences the transient dynamic of the bit anticipator circuit. This has to be taken into account for a technical realization.

### 3.2. Circuit Implementation

The bit anticipation circuit of Fig. 2 was technical realized on a printed circuit board using the memristive cells of Fig. 4 and a comparator-electronic to digitize the anticipated output signals  $u_0$  and  $u_1$ , see Fig. 5. Due to technical reasons, there are slight differences between the realized and idealized circuit mentioned before. The required values for the used passive circuit elements has been taken from [11].

## 4. Results

### 4.1. Simulations

For a verification of the functionality of this anticipation circuit, we have used LTSpice. The fast switching behavior of real ECM cells has been incorporated by the voltage-controlled memristor model from [8]. Based on the insights of [8], we have adapted the memristor model to be closer to the real device functionality, as depicted in Fig. 4 (left). Therefore, we have

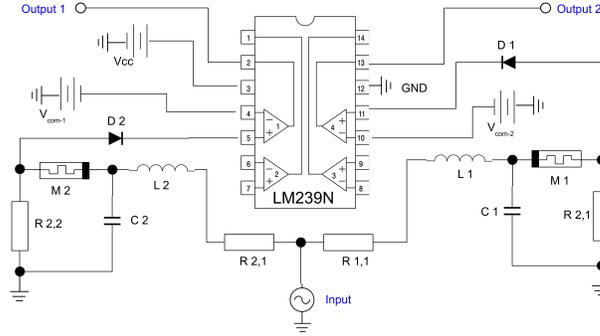


Figure 5. Circuit layout of the bit anticipation circuit of Fig. 2. For the implementation on a printed circuit board the following values of the passive circuit elements have been used:  $R_{1,1} = R_{1,2} = 100 \Omega$ ,  $L = 100 \text{ mH}$ ,  $C = 150 \text{ nF}$ ,  $R_{2,1} = R_{2,2} = 10 \text{ k}\Omega$ , and  $\omega_0 = 8.16 \text{ rad/s}$ . In addition, a comparator electronic (LM239N) digitizes the anticipated logical states. The comparator threshold voltages are set to  $V_{\text{com}} = V_{\text{com-1}} = V_{\text{com-2}} = -100 \text{ mV}$ .

utilized asymmetric thresholds for positive  $U_{\text{on}}$  and negative  $U_{\text{off}}$  applied voltages with

$$f(M, u) = g(u) [\sigma(u) \sigma(M - M_{\text{on}}) + \sigma(-u) \sigma(M_{\text{off}} - M)], \quad (8)$$

with  $g(u) = \beta [\sigma(u - U_{\text{on}}) [U_{\text{on}} - u] + \sigma(U_{\text{off}} - u) [U_{\text{off}} - u]]$ ,

where  $\sigma(u)$  is the unit-step function.

The simulation results are shown in Fig. 6: After a certain sequence of learning process, the electrical circuit is indeed capable of anticipating a bit value of 0 for negative pulses and a bit value of 1 for positive pulses. In order to digitize the analogue output voltage a threshold voltage of  $U_{d_0} = -U_d = -3.8 \text{ V}$  and  $U_{d_1} = U_d$  was chosen for a bit value of 0 and 1, respectively. Under the conditions that have been mentioned in the context of (5) the simulation result shows, that for negative pulses the amplitude of the oscillating voltage  $u_0(t)$  and for positive pulses the amplitude of the oscillating voltage  $u_1(t)$  grows up. After the learning process, one pulse is sufficient to yield an oscillating voltage with high amplitude at the associated output terminal. Therefore the anticipation circuit enables bit anticipation.

#### 4.2. Measurements

The measured signals of the electrical implemented bit anticipation circuit are depicted in Fig. 7. The bipolar voltage trains, which were applied to the circuit to anticipate digital patterns, are shown in Fig. 7(a,d). Both voltage trains contain three learning voltage pulses in series at the resonance frequency of the circuit followed by a set of two separated voltage pulses. The second set of voltage pulses represents an incomplete bit pattern with only two pulses, which were used to demonstrate the pattern completion ability of the anticipation circuit.

At each single voltage input pulse the voltage across the memristive device increases, where at a certain point the voltage across the memristive device is large enough that the corresponding device changes its resistance state from  $M_{\text{off}}$  to  $M_{\text{on}}$ . For the electronic circuit the amplitudes  $e_0$  and  $e_1$  of the bipolar input signals have been chosen to  $e_0 = -1.9 \text{ V}$  and  $e_1 = 2.1 \text{ V}$ , respectively. Those amplitude values ensure that the voltage oscillation at the

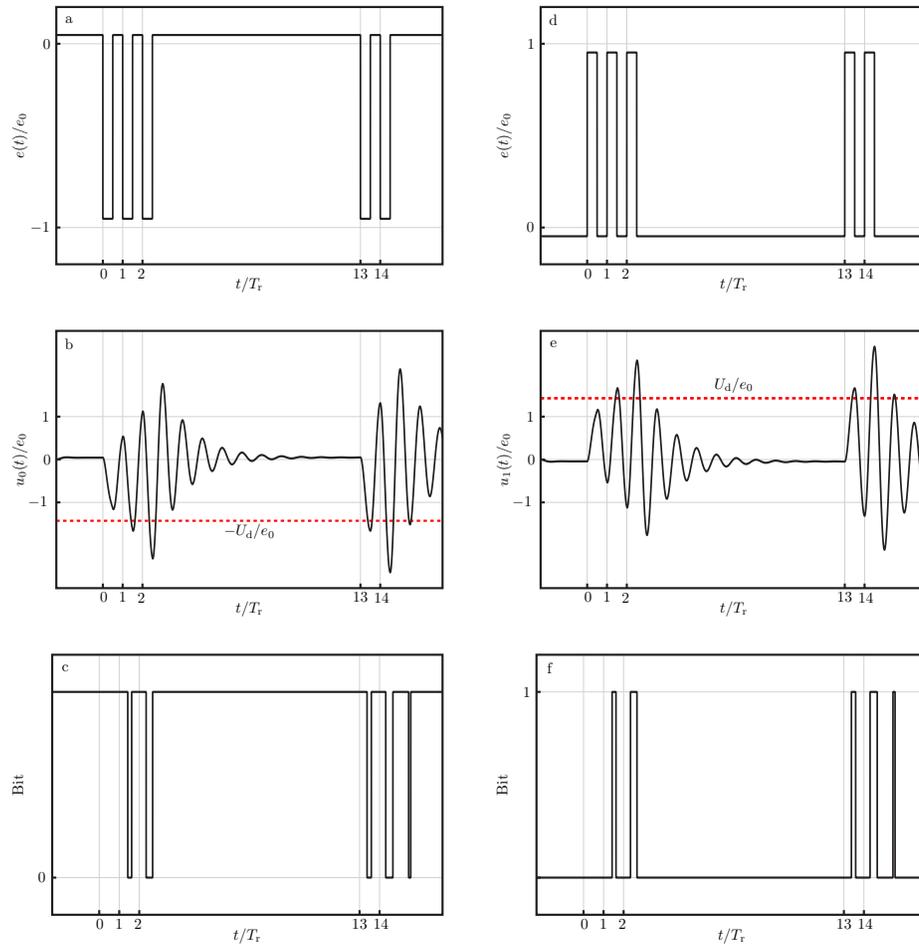


Figure 6. Simulation results of the bit anticipation circuit, where the parameters  $e_0 = 2.1$  V,  $U_d = 3.8$  V,  $R = 100$   $\Omega$ ,  $C = 150$  nF,  $L = 100$  mH,  $\beta = 10^{16}$ ,  $U_{on} = 1.4$  V,  $U_{off} = -0.1$  V,  $M_{on} = 1$  k $\Omega$  and  $M_{off} = 0.5$  G $\Omega$  have been used. Negative (a) and positive (d) voltage pulses were used for anticipating a bit 0 and 1, respectively. Depending on the excitation signal there are oscillating output voltages  $u_0(t)$  for bit 0 and  $u_1(t)$  for bit 1 (b, e). A bit 0 is anticipated for negative excitation pulses (c), whereas a bit 1 is anticipated for positive excitation pulses (f).

third input voltage pulse is large enough to overcome the set voltage  $U_{on}$  of the memristive device. Therewith, the particular memristive device switches its resistance state and the given bit pattern is anticipated. The voltages  $u_0$  and  $u_1$  across the resistances  $R_{2,1}$  and  $R_{2,2}$  are shown in Fig. 7(b,e). In the beginning the memristances  $M_1$  and  $M_2$  are much higher as the series resistances  $R_{2,1}$  and  $R_{2,2}$ . Consequently, most of the input voltage drops across the particular memristive device, such that  $u_0$  and  $u_1$  remains nearly unaffected. The voltage  $u_0$  or  $u_1$  alters significantly if the corresponding bit is anticipated. After the learning intervals, the incomplete pattern of only two input pulses results in an oscillation of  $u_0$  or  $u_1$ , in which

a negative input pulse yields an oscillating voltage  $u_0$ , while a positive input pulse results in an oscillation of  $u_1$ , cf. Fig. 7(b,e). Finally, these signals are digitized using the comparator electronics, see Fig. 7(c,f). We like to remark that the threshold voltage in the experimental realization have been chosen with respect to the voltage dividers  $R_{2,1}$  and  $M_1$  or  $R_{2,2}$  and  $M_2$ . In contrast to the simulation model, the voltage used for the comparator electronics differs therefore only from zero, if the respective memristive device is in the low ohmic state. Hence, a smaller voltage (labelled by  $V_{\text{com}}/e_0$  in Fig. 7) has been used compared to the simulation, cf. Fig. 6. To summarize, the circuit enables a kind of pattern completion, where after the learning phase an incomplete pattern, which consists of only two voltage pulses, results in an output pattern consisting of three individual voltage pulses.

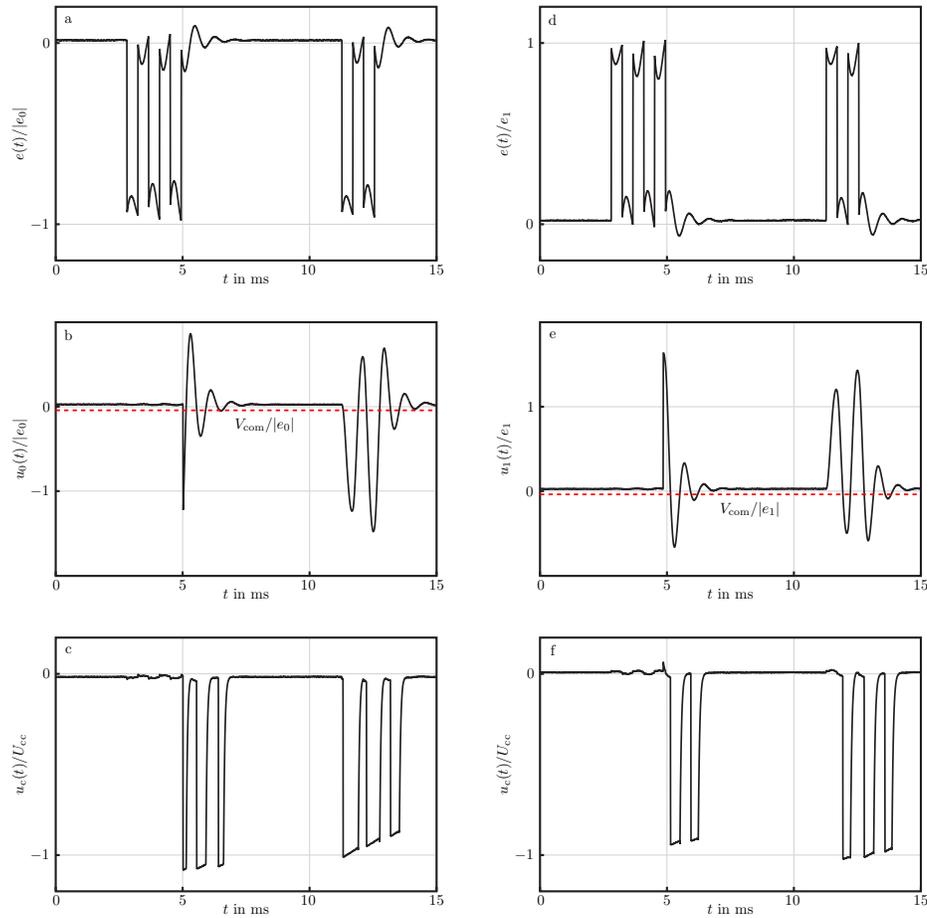


Figure 7. Measured signal sequences of the bit anticipation circuit in accordance to Fig. 6: Input voltage pulse sequence for the anticipation of a bit 0 (a), the corresponding oscillating output signal (b) and the anticipated logical states (d). In (d,e,f) the signals for the anticipation of a bit 1 are shown. Here,  $U_{\text{cc}}$  denotes the comparator output voltage amplitude and  $V_{\text{com}}$  is the comparator threshold voltage ((b, e) red-dashed).

*Demonstration of a software bit-array anticipator*

So far the bit anticipator is understood as a basic element and has been discussed in an abstract way. Now, we will focus on the anticipation of information, where any information can be represented by a set of bits, which in turn can be anticipated by an array of bit anticipators. For the sake of clarity, we used a grayscale image of digits with  $5 \times 9$  pixels as input information. Black and white pixels are associated with the bits 0 and 1, respectively. Gray values in between have to be quantized in order to decide if this value belongs to a white or black pixel. In order to visualize an analog information change under certain conditions, we refrain from this quantization.

At first, we train the anticipation array by the images in accordance to the excitation used in Fig. 6. As expected, after the first three input training images the output image fades out over time, but the image is successfully anticipated after the last two excitations. Hence, anticipation can be regarded as to regenerate information.

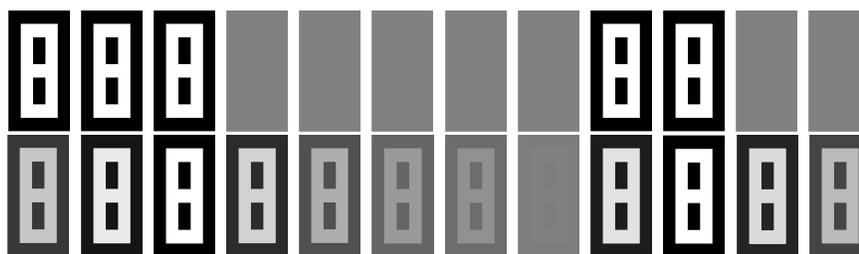


Figure 8. Anticipation of images: Input sequence (top) and output sequence (bottom).

Secondly, we examine the anticipation under noisy conditions. From Fig. 9 it can be taken that this anticipatory system inherently reduces the noise and the anticipation is still working. Of course, this depends on the noise level. In the case of a higher noise level, further simulations have shown that this can be compensated by increasing the number of training images.

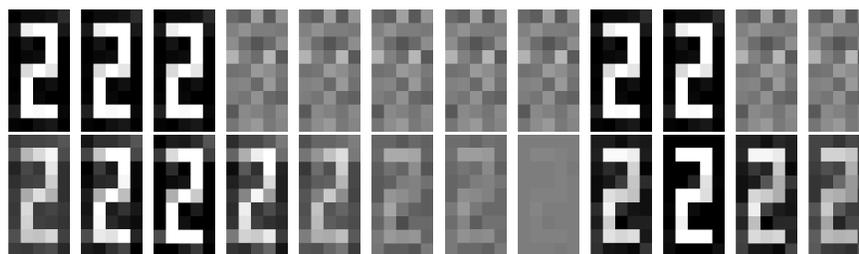


Figure 9. Anticipation of noisy images: Input sequence (top) and output sequence (bottom).

At last, we inspect the anticipation, when the input sequence is disturbed by an intermediate failure image, see Fig. 10. From the output sequence, it can be verified that the failure image is treated like in the noisy case before. When it comes to the second excitation with the two

correct images the influence of the failure image can be neglected, i. e. this anticipatory system has filtered out the faulty information.

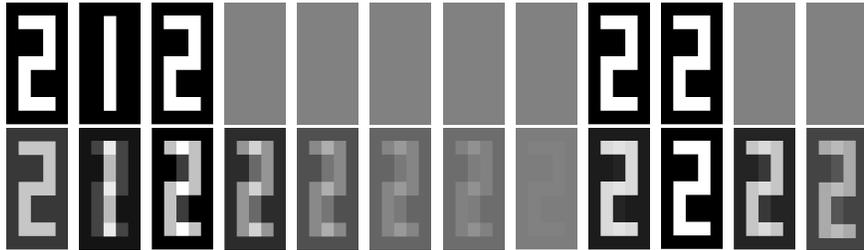


Figure 10. Anticipation of images disturbed by a failure image: Input sequence (top) and output sequence (bottom).

## 5. Conclusions

Anticipation is a general concept in nature and even observed in unicellular creature such as amoebas. In this work, a bio-inspired memristive circuit is presented which enables information anticipation. It is based on a memristive resonator circuit, which mimics the anticipation capability of an amoeba but is limited to anticipate unipolar pulses. Moreover, this circuit has been extended to anticipate bipolar pulses representing an information bit with the values 0 or 1. This extension allows for the anticipation of a single bit, which is the basic unit of information in digital computing. An anticipation of bit vectors can be realized by replicating this circuit pursuant to the length of the bit vector. Hence, any information represented by such a bit vector – which occurs in periodical events – can be anticipated. In particular, this functionality could be interesting in robotics. For instance, if this bit vector contains information about location, velocity vectors, and so on, a robot could predict a future location and act according to this prediction. To sum up, our work can be considered as a path towards implementing the biological phenomenon of anticipation in technical systems by using a memristive circuitry, which is capable of pattern completion even under noisy signal conditions or false input information.

## Acknowledgement

We acknowledge support by: German Science Foundation (DFG) - Research Group FOR 2093 'Memristive Bauelemente für neuronale Systeme'.

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