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Preface

Our capability to integrate ever larger number of transistors is surprising even to the most ardent believers of scaling. At 2005 International Solid State Conference, Intel announced a processor with 1.7 billion transistors. This trend is likely to continue at least for a decade. However, there are a number of issues that must be dealt with if this integration trend is to continue. In this context, thermal and power management of ultra large scale integration (ULSI) is one of the major concerns.

Thermal issues are a bi-product of scaling and quest for speed. This issue came to the forefront as we scale the technology in nano-metric regime. However, it is not limited to high speed circuits alone. Today, even moderate speed ULSI must worry about containing the junction temperature under limits. The junction temperature affects large number of important device parameters, and an unabated increase in the junction temperature may have disastrous implications on performance, and long term reliability of integrated circuits. Moreover, manufacturing and operational costs such as expensive cooling solutions may increase significantly, if rising junction temperatures are not contained.

Recently, a great deal of attention has been paid to thermal issues and there are international conferences dedicated to thermal issues in electronics. However, lack of books in this area is impeding the awareness of the subject to engineers and managers who are suddenly confronted with these issues. This book makes an attempt to provide a comprehensive overview of the power and thermal management of integrated circuits.

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Arman Vassighi and Manoj Sachdev

Foreword

Semiconductor industry has benefited from several decades of growth following the Moore's law. Today's high-performance Integrated Circuits (ICs) have more than one billion transistors. Scaling of CMOS technology has enabled this increase in transistor count, and scaling continues in spite of emerging barriers in process technology development, design and test. Today, the 65nm CMOS technology node is moving from development to high volume manufacturing while research and development continues on future technology nodes.

This growth comes with multiple challenges. Design of ICs in these scaled technologies faces formidable limitations. It is becoming increasingly difficult to sustain supply and threshold voltage scaling in order to provide the required performance increase, limit energy consumption, control power dissipation, and maintain the reliability. These requirements pose several difficulties across a range of disciplines spanning process technology, manufacturing, circuits, testing, systems, and architecture. One of these critical challenges is the thermal and power management of high speed ICs which has been subject of extensive research over past several years. Moreover, reliability screening and burn-in at elevated voltage and temperature further exacerbate this problem. Furthermore, researchers have looked into finding ways to cool ICs efficiently by accounting for the cooling cost in total system power. It may be possible to use efficient cooling to improve performance, leakage, and reliability of ICs, and thus continue on the path of scaling.

This book is very timely to address these challenges and to capture key learning concepts. This book discusses thermal design barriers and the proverbial power wall that IC and system designers are facing today. We have followed authors' work, interacted with them, and we highly recommend this book to students, engineers, professionals and people that are pursuing advanced designs and are facing some of these challenges.

Vivek De