Lecture Notes in Computer Science

Edited by G. Goos and J. Hartmanis

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Heinrich J. Stüttgen

A Hierarchical Associative Processing System

Springer-Verlag
Berlin Heidelberg New York Tokyo

Author

Heinrich J. Stüttgen
Universität Dortmund, Fachbereich Informatik
Postfach 500 500, D-4600 Dortmund 50

CR Subject Classifications (1985): B.3.2, C.1.2, D.4.2, D.4.3, H.2.6

ISBN 3-540-15652-6 Springer-Verlag Berlin Heidelberg New York Tokyo
ISBN 0-387-15652-6 Springer-Verlag New York Heidelberg Berlin Tokyo

Printing and binding: Beltz Offsetdruck, Hemsbach/Bergstr.
2145/3140-543210

Acknowledgement

I would like to thank Professor Dr. Lutz Richter for his guidance in carrying out this research. Thanks are also due to Dr. Alfons Steinhoff and Dipl.-Inform. Michael Goedicke as well as numerous other people for their valuable comments and suggestions on various aspects of this project. Further I am indebted to Elke Schickentanz, Wolfgang Deiters Frank Paszota, and Burkhard Peuschel for their assistance in preparing the manuscript. Last not least, I thank my wife Evelyn for the improvements of my writing style and for her continuous encouragement during the course of this work.

Abstract

The concept of associative or content addressable memories (CAMs) has been around for over 25 years. They are generally considered an attractive but at the same time very expensive type of memory. Therefore any CAM organization has been tailored to and restricted to a specific application. In this book we describe the design of a two level associative memory hierarchy which is aimed at a broad spectrum of applications. The design is based on state of the art technology and configurable to a wide range of cost/performance requirements.

After a short review of the logical aspects of memories we survey and classify existing designs and implementations of the associative concept, with regard to programming languages and hardware organizations.

The actual design is top-down structured and consists of four levels.

The first level is the programming language PASCAL/A, which is an extension of standard PASCAL by a few powerful constructs providing associative data structures and processing. The second level is an intermediate language; suitable for direct interpretation on an associative processor. Third we describe the architecture of a two-level hardware associative memory. The first level is a processing ensemble built of single chip processors with on-chip memory. The second level is a cellular logic organization based on modified movable head disks. Fourth we suggest a memory hierarchy management scheme that employs staging and which is data structure and program semantic oriented. Finally we point out some open questions and make some suggestions for future research in the area.

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