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Power-Aware Computer Systems

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Preface

Welcome to the proceedings of the Power-Aware Computer Systems (PACS 2002) workshop held in conjunction with the 8th International Symposium on High Performance Computer Architecture (HPCA-8). Improvements in computer system performance have been accompanied by an alarming increase in power and energy dissipation, leading to higher cost and lower reliability in all computer systems market segments. The higher power/energy dissipation has also significantly reduced battery life in portable systems. While circuit-level techniques continue to reduce power and energy, all levels of computer systems are being used to address power and energy issues. PACS 2002 was the second workshop in its series to address power-/energy-awareness at all levels of computer systems and brought together experts from academia and industry.

These proceedings include research papers spanning a wide spectrum of areas in power-aware systems. We have grouped the papers into the following categories: (1) power-aware architecture and microarchitecture, (2) power-aware real-time systems, (3) power modeling and monitoring, and (4) power-aware operating systems and compilers.

The first group of papers propose power-aware techniques for the processor pipeline using adaptive resizing of power-hungry microarchitectural structures and clock gating, and power-aware cache design by avoiding tag checks in periods when the tags have not changed. This group also includes ideas to adapt energy and performance dynamically by detecting regions of application at runtime where the supply voltage may be scaled to reduce power with a bounded decrease in performance. Lastly, a paper on multiprocessor designs trades off computing capacity and functionality for improved energy per cycle by scheduling simple tasks on low-end and low-energy processors and complex tasks on high-end processors.

The second group of papers target real-time systems including ideas on a low-complexity heuristic which schedules real-time tasks such that no task misses its deadline and the total energy savings are maximized. The other papers in this group (1) tune the system-level parallelism to the current-level of power/energy availability and optimize the system power utilization, and (2) perform adaptive texture mapping in real-time 3D graphics systems based on a model of human visual perception to achieve significant power savings without noticeable image quality degradation.

The third group of papers focus on power modeling and monitoring including statistical profiling to detect software hotspots of power, and using Petri Nets to model DRAM power policies. This group also includes a simulator for evaluating the performance and power of dynamic voltage scaling algorithms.

The last group concentrates on OS and compilers for low power. The first paper proposes application-issued directives to set the power modes in devices such as a disk drive. The second paper proposes policies for cluster-wide power

management. The policies employ combinations of dynamic voltage scaling and turning on and off to reduce overall cluster power.

PACS 2002 was a highly successful forum due to the high-quality submissions, the enormous efforts of the program committee and the keynote speaker, and the attendees. We would like to thank Ronny Ronen for an excellent keynote speech, showing the technological scaling trends and their impact on energy/power consumption in general-purpose microprocessors, and pinpointing recent microarchitectural strategies to achieve more power-efficient microprocessors. We would like to also thank Antonio Gonzalez, Andreas Moshovos, John Kalamatianos, and other members of the HPCA-8 organizing committee who helped arrange for local accomodation and publicize the workshop.

February 2002 Babak Falsafi and T.N. Vijaykumar

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