

Software Documentation and the Verification Process

David Lorge Parnas

Department of Computing and Software
Faculty of Engineering, McMaster University
Hamilton, Ontario, Canada L8S 4L7
`parnas@qusunt.cas.mcmaster.ca`

Abstract. In the verification community it is assumed that one has a specification of the program to be proven correct. In practice this is never true. Moreover, specifications for realistic software products are often unreadable when formalised. This talk will present and discuss more practical formal notation for software documentation and the role of such documentation in the verification process.