Simulations for Thermal Analysis of MOSFET IPM Using IMS Substrate

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Abstract. The project was focused on the thermal aspects of the new IPM module design. The investigations were aimed to estimate the influence of the particular design of the MOSFET transistor location versus the steady-state thermal feature of the considered IPM and to determinate its thermal impedance as well as to evaluate its equivalent RC network (ladder) model. It required working out the 3-D thermal model of the considered system that was used in numerical simulations and next, tested with commercial software, ANSYS 5.7 based on Finite Element Method (FEM).

1 Introduction

In any electronics equipment, the temperature rise above the permissible level results in its worse work or even in its destruction. Therefore, the proper thermal design, known as the thermal management is more and more important part of any design process in electronics industry. One can find that effective draining the heat off the source to ambient becomes the problem of the greatest importance, as one must keep the safe work temperature [1,2]. According to the general assumptions concerning the MOSFET IPM under consideration, the analysed system covered 50x40 mm^2 IMS (Insulated Metal Substrate) plate as the substrate on which two MOSFET Toshiba transistors 2SK2866 in TO-220AB packages were to be placed symmetrically and fastened by soldering technique.
The investigations were aimed to evaluate the influence of the particular design of the transistor location versus the steady-state thermal feature of the considered IPM.

2 Thermal Model of IPM

The Fig. 1 introduces two possible designs of the module with two considered layouts for the transistor packages. The both designs use the IMS substrate that is introduced in Fig. 2. section. The preliminary simulations proved that the layout introduced in Fig. 1 a) should be considered as the optimal one, so the further simulations were led for this layout. As the structure is fully symmetrical, only one of its halves is taken to further investigations.

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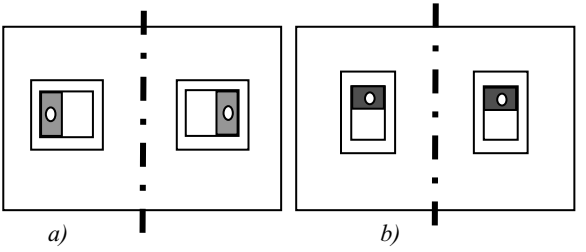

Fig.1. Two possible locations of the transistors on the IMS plate with symmetry axis as the dot line (copper foil is marked as an additional rectangular surrounding the transistor)

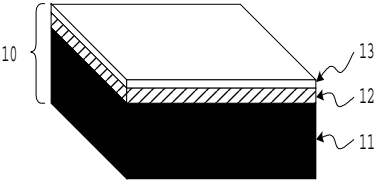

Fig.2. General view of IMS plate presenting the construction layers: 10 – the whole structure (2.22mm); 11 – aluminium baseplate (2.0mm); 12 – polymer insulating (0.12mm); 13 – copper foil for circuit pattern (0.10mm)

The final view of the 3-D thermal model of IPM used in the simulations is shown in Fig.3. It covers one half of the IPM with the transistor fastened by a homogeneous solder layer to the IMS plate. In the transistor thermal model three elements are distinguished only. There are the bottom copper layer (lead frame) soldered to the copper foil of IMS, the silicon chip placed on the lead frame and the epoxy layer covering the silicon chip.

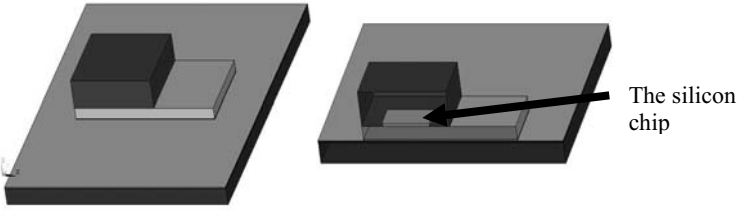

Fig.3. 3-D view of the IPM thermal model: (a) top view; (b) the cross section

The Table 1 collects dimensions of the elements for the model from Fig.3. The copper foil length and width are not determined since they can vary depending on the circuit pattern and they are one of the parameters changed during the investigations. The physical parameters of the materials the parts are made from are collected in the Table.2. It has been assumed that the thermal conductivity of silicon can vary according to the actual temperature in the following way:

$$\lambda = a_t T^{-b} \qquad (1)$$

where: a_t=4350, b=1.4, and T is the temperature [K].

Table 1. The dimensions of the elements of thermal model

Material	length [mm]	width [mm]	thickness [mm]	Comments
Al base plate (11)	50	40	2.0	IMS plate
Insulate layer (12)	50	40	0.12	IMS plate
Cu foil (13)	var	var	0.10	IMS plate
Solder	10	10	0.10	
Lead frame	10	10	0.7	Transistor
Silicon chip	4.8	4.8	0.30	Transistor
Epoxy				Transistor

Table 2. The physical parameters of materials

Material	ρ[kg/m^3]	c_p[J/kg K]	λ [W/m K]
Aluminium	2700	900	205
Insulator in IMS	2300	800	1.5
Copper	8960	385	398
Solder	9290	167	48
Epoxy	1270	1050	1.7
Silicon	2330	167	var

In the model, it has been assumed that the silicon chip is the only heat source in which the heat is dissipated homogeneously. The magnitude of heat dissipation has been fixed on the base of Toshiba transistor 2SK2866a data sheet [3]. Taking into account its catalogue maximum ratings, so called the P_D drain power dissipation has been chosen as equal to125W, which gives the heat generation of 18.1e^9 W/m^3 when taking into account the volume of the silicon chip.

The boundary conditions for the border planes have been chosen according to their role in the heat exchange in the real IPM construction. For the plane that corresponds to the symmetry axis the adiabatic boundary condition is the only one that can be applied. For the rest of border planes the boundary conditions using the ambient temperature T_a as the reference one have been used. It is the isothermal one for the bottom of IMS substrate aluminium layer, which is usually kept at the ambient temperature and the convection one for the other surfaces. In the simulation the convection coefficient of 7 W/m^{2}K that is typical for free convection inside a well-ventilated case and the ambient temperature equalled to 25^{0}C has been used.

The full geometry of the considered structure was introduced to Preprocessor of Ansys 5.7 software [4] and all the material properties as well. The manual meshing was chosen to optimize the mesh according to the areas of the greatest interest. Fig. 3 shows the introduced model, and Fig. 4 the optimized mesh.

3 The Simulation Results

We aimed to find the critical value for the Cu foil surface for the heat disposal, and to obtain the results we considered five different dimensions (see Table 1) outward to

the TO-220AB package; i.e. 0.5 mm, 1 mm, 2 mm, 4 mm, whole surface. The maximum temperature (always on the top part of the silicon chip) cannot exceed 125^0C as it is the upper edge of the permitted temperature range that allows the devices to operate safely.

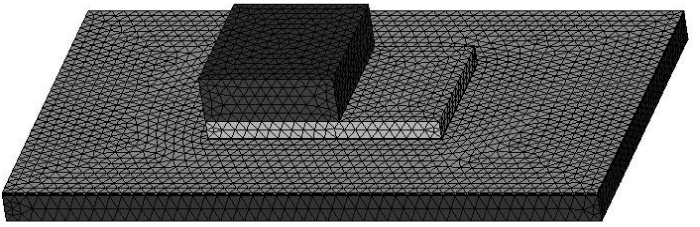

Fig. 4. Meshing. The figure shows the model for Cu on the whole surface

The Fig. 5 introduces the example of maximum temperature distribution for the structure (a – end view; b – section), where the Cu layer exceeds the surface of TO-220AB by 4 mm. The case when Cu covers the whole surface was checked to make no difference comparing to 4 mm. The figures 6 and 7 show calculated curves of the thermal resistance and the maximum temperature versus the copper width. Checking the temperature distribution, one sees that for the copper width less than 4 mm the possible temperature is exceeded, even for these ideal conditions of the heat removal. Only for 4 mm width the maximum temperature in the silicon chip gains the value of 124^0C and assures the safe operation of the electronic devices. The temperature does not lower when one enlarges the copper surface more than 4 mm. So the heat conditions are stable then.

To estimate the heat dissipation in the whole structure we prepared the heat vector diagram (Figs. 8 and 9). The Figure 8 introduces the heat flow for the case when copper covers 1 mm path beyond the transistor package surface, and the Figure 9 the one when the Cu path width amounts to 4 mm. The further widening of copper did not give any changes in the heat flow distribution.

4 Conclusions

The simulations have been led with the assumption that the temperature at the bottom of the whole package equals to an ambient one (25^0C), i.e. the cooling method is very efficient. Also the assumption of the convection coefficient at the value of 7 W/m^{2}K can be valid for efficient ventilating, only. That is why, the results should be considered as made in good cooling conditions. If any real conditions are worse, the maximum power range should not be obtained if the silicon is to be kept in a safe temperature. The maximum temperature value for silicon (125^0C) should be met then, without any exceptions. The simulations showed that the surface covered by Cu is very important here. If the circuit design does not allow to cover the surface with Cu in a sufficient way, the heat cannot be removed when the maximum power is applied. The width of 4 mm has resulted from our simulations.

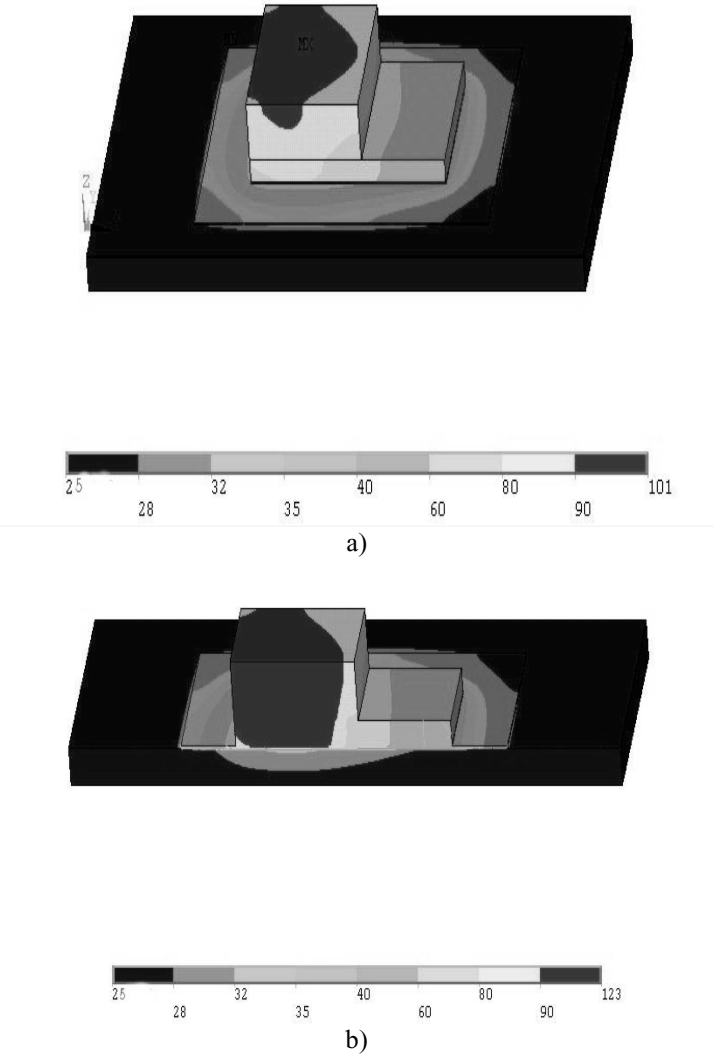

Fig. 5. The temperature [°C] distribution for Cu width 4.0 mm; a) end view, b) section

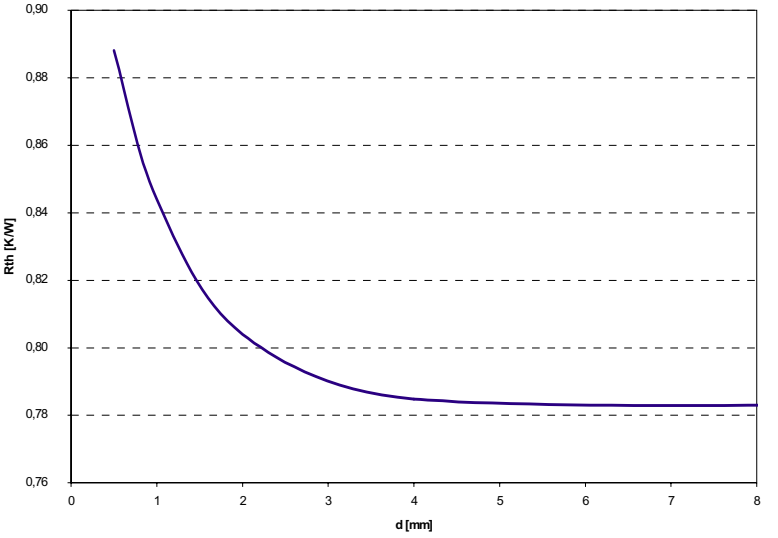

Fig. 6. Thermal resistance versus the growing width of copper

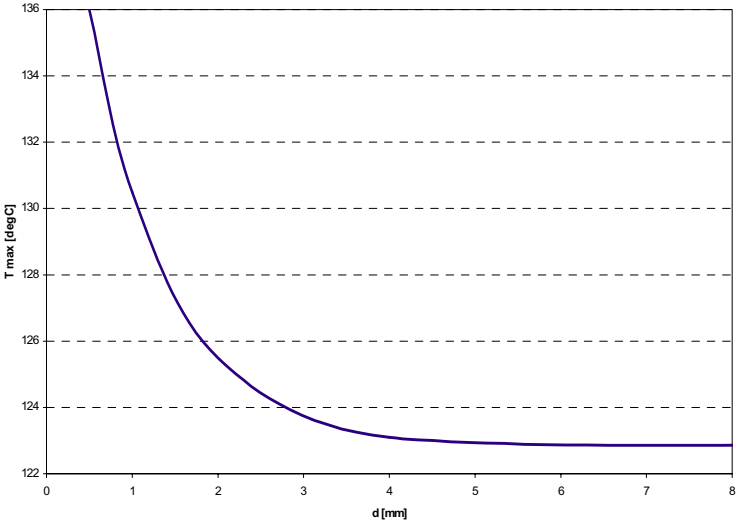

Fig. 7. Maximum temperature (upper surface of silicon chip) versus the growing width of copper

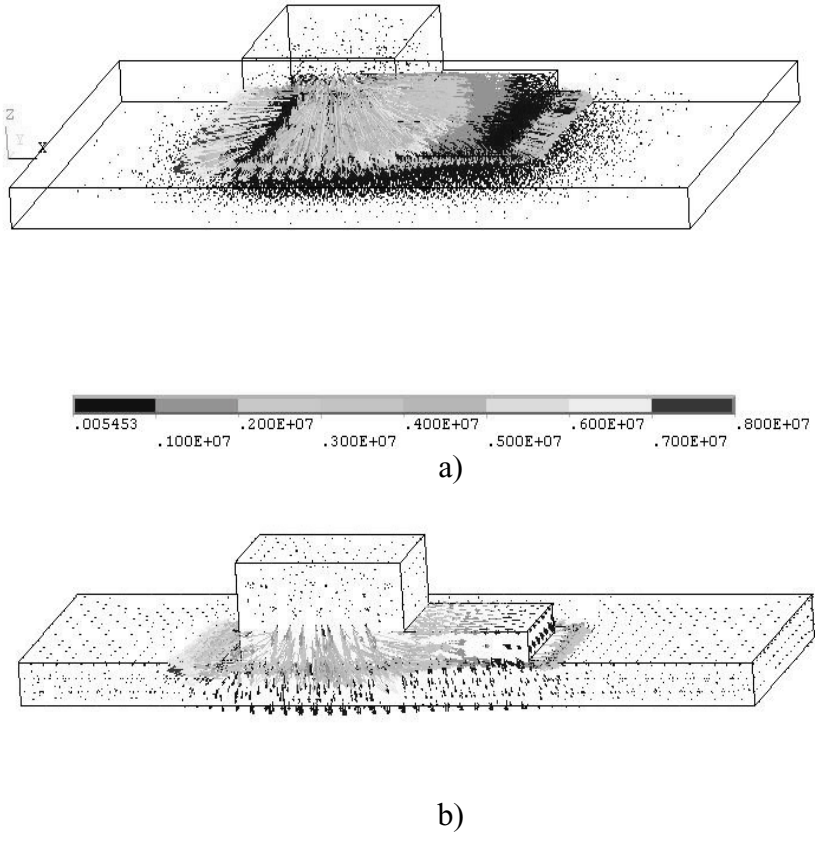

Fig. 8. Heat dissipation for Cu path width of 1 mm; a) end view, b) section

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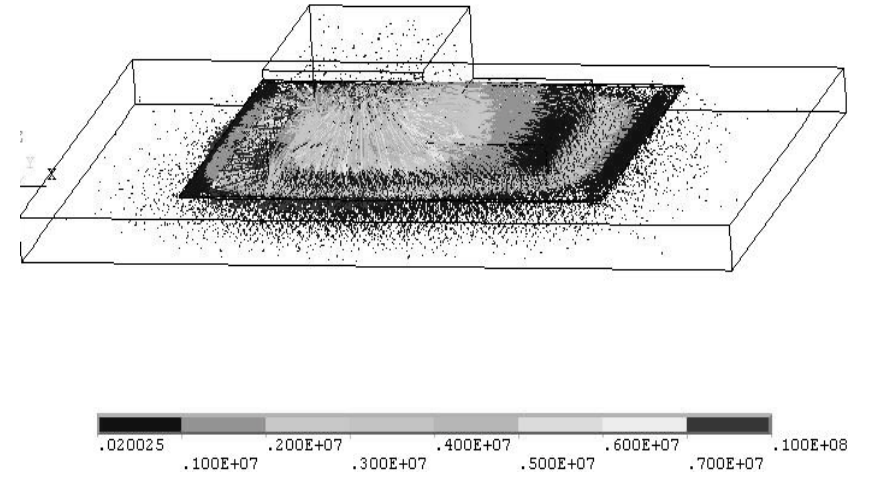

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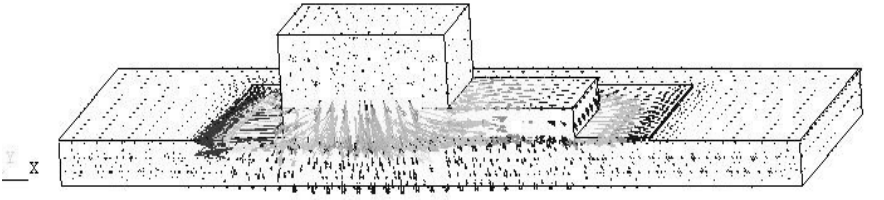

b)

Fig. 9. Heat dissipation for Cu path width of 4 mm; a) end view, b) section