# Run-Time Reconfiguration at Xilinx
## (invited talk)

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**Abstract.** Run-Time Reconfiguration (RTR) provides a pow erful, but
essen tial ly untapped mode of operation for SRAM-based FPGAs. Re-
search over the last decade has indicated that RTR can provide sub-
stan tial benefits to system designers, both in terms of overall perfor-
mance and in terms of design simplicity. While RTR holds great promise
for many aspects of system design, it has only recen tly been consid-
ered for commercial application. Two factors seem to be converging to
make R TR based system design viable. First, silicon process technol-
ogy has adv anced to the point where million gate FPGA devices are
commonplace. This permits larger, more complex algorithms to be di-
rectly implemented in FGPAs. This alone has led to a quiet revolution
in FPGA design. Today, coprocessing using large FPGA devices coupled
to standard microprocessors is becoming commonplace, particularly in
Digital Signal Processing (DSP) applications. The second factor is soft-
w are. Until recen tly, there was literally no softw are support available for
R TR. Existing ASIC-based design flows based on schematic capture and
HDL did not provide the necessary mechanisms to allo w implementa-
tion of RTR systems. Today, the JBits softw are tool suite from Xilinx
pro vides the direct support for coprocessing and for RTR. The combi-
nation of hardware and softw are for R TR has already begun to show
some impressive results on standard system design methodologies and
algorithms. Future plans to enhance both FPGA architectures and tools
such as JBits should result in a widening acceptance of this technology.