

Lecture Notes in Computer Science

Edited by G. Goos and J. Hartmanis

457

H. Burkhart (Ed.)

CONPAR 90 – VAPP IV

Joint International Conference on
Vector and Parallel Processing
Zurich, Switzerland, September 10–13, 1990
Proceedings



Springer-Verlag

Berlin Heidelberg New York London
Paris Tokyo Hong Kong Barcelona

Editorial Board

D. Barstow W. Brauer P. Brinch Hansen D. Gries D. Luckham
C. Moler A. Pnueli G. Seegmüller J. Stoer N. Wirth

Editor

Helmar Burkhart
Institut für Informatik, Universität Basel
Mittlere Staße 142, CH-4056 Basel, Switzerland

CR Subject Classification (1987): C.1, J.2

ISBN 3-540-53065-7 Springer-Verlag Berlin Heidelberg New York
ISBN 0-387-53065-7 Springer-Verlag New York Berlin Heidelberg

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, re-use of illustrations, recitation, broadcasting, reproduction on microfilms or in other ways, and storage in data banks. Duplication of this publication or parts thereof is only permitted under the provisions of the German Copyright Law of September 9, 1965, in its version of June 24, 1985, and a copyright fee must always be paid. Violations fall under the prosecution act of the German Copyright Law.

© Springer-Verlag Berlin Heidelberg 1990
Printed in Germany

Printing and binding: Druckhaus Beltz, Hembsbach/Bergstr.
2145/3140-543210 – Printed on acid-free paper

Preface

While parallel architectures were pure research vehicles some years ago, this situation has changed substantially. There are many commercial systems available now that compete for market segments in scientific computing. The 1990s are likely to become the decade of parallel processing.

The past decade has already seen the emergence of the two highly successful series of CONPAR and VAPP conferences on the subject of parallel processing. The *Vector and Parallel Processors in Computational Science* (VAPP) meetings were held in Chester (1981), Oxford (1984) and Liverpool (1987). The *International Conferences on Parallel Processing* (CONPAR) took place in Erlangen (1981), Aachen (1986) and Manchester (1988). Despite the importance of parallel architectures and parallel computing, the Standing Committees of both conference series got the impression that there are too many conferences, workshops, summer schools, and exhibitions at the moment. The idea of a joint conference came up. On one hand we succeeded because for the first time these conferences are being held together. During the preparations for this conference, however, several new meetings appeared, with the result that there is a tremendous number of events this year. The organizers of CONPAR 90 - VAPP IV are thus satisfied to see that their conference series is already quite mature. We have received such a lot of good and well-written papers that we had to reduce the number of published papers considerably. Whether CONPAR and VAPP continue as joint conferences in future is still open at the moment. Hopefully this joint conference series can be developed into *the* important European event.

This is the first time such a big conference on parallel processing is taking place in Switzerland. Returning home from the Frankfurt meeting in February 1989 where the final vote was given for a Zurich conference, it was a great relief to get so much support from colleagues. I would like to express my special thanks to Ernst Rothauser, who took the heavy load of coordinating all local arrangements and the organization.

I would also like to thank the other members of the Steering and Organizing Committees for their continuous help. Special thanks go to Peter Arbenz, Armin Friedli, Walter Gander, Hans-Jürgen Halin and Richard Wait. I wish to extend my sincere thanks to the members of the Program Committee for their contributions to the shaping of the conference program and their help in reviewing papers. I also express my gratitude to all other referees for their assistance in

this process. The idea of the Computation Race came up in an early lunch with Jürg Nievergelt. I would like to thank him as well as the Awards Committee for this and other enrichments of the conference program.

Two prominent computer architects offered their help in organizing this event. Professor Speiser will act as the Honorary Chairman and will address the conference with his keynote "Digital Electronics for 50 Years: No Limits to Growth?". Professor Händler, the founder of the CONPAR series, is acting as the Chairman of the Standing Committee. We are indebted to him for his continual advice on, and confidence in, our Zurich conference.

The preparation of the technical program was a time-consuming process. I would not have managed to fulfill all the deadlines without my assistants Stephan Gutzwiler and Stephan Waser, who carefully co-ordinated all steps and many times suffered with me. The secretaries Mrs. A. Mathys and Mrs. Rothauser helped a lot to ease our job. Let me thank them all.

No conference preparations can be made without initial funding. The Swiss Informatics Society/Swiss Chapter of the ACM and IEEE Switzerland Section provided this help without hesitation. GI-PARS, BCS-PPSG, and IEEE CS later co-operated.

We would like to thank ETH Zürich for acting as the host site, as it provides such a pleasant conference environment. Last but not least I would like to thank the University of Basel for providing an infrastructure which enabled us to organize the conference from a distance.

The proceedings in hand start with the keynote address given by the Honorary Chairman. Next come two papers given by invited speakers, V. Bhatkar and E. Odijk. The main part of the proceedings consists of 77 papers written by authors from 20 different countries. These contributed papers have been selected by an international program committee. The topics of the papers are manifold; please note that we have grouped the table of contents according to the session titles. We have also added the rules for the Computation Race for future reference. The results of this competition will be presented at the conference and possibly published later.

Now it is up to you, the conference participant and reader of these proceedings, to make the final assessment.

Contents

Keynote Address

- A. P. Speiser
Digital Electronics for 50 Years: No Limits to Growth? 1

Invited Presentations

- V. P. Bhatkar
Parallel Computing: An Indian Perspective 10
E.A.M. Odijk
POOMA, POOL and Parallel Symbolic Computing: An Assessment 26

New Models of Computation

- P. Evripidou and J-L. Gaudiot
A Decoupled Data-Driven Architecture with Vectors and Macro Actors 39
- R. W. Hartenstein, A. G. Hirschbiel and M. Weber
A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware 51
- H. Kikuchi, T. Yukawa, K. Matsuzawa and T. Ishikawa
Presto: A Bus-Connected Multiprocessor for a Rete-Based Production System 63

Performance Prediction, Analysis, and Measurement

- A. Basu, S. Srinivas, K.G. Kumar and A. Paulraj
A Model for Performance Prediction of Message Passing Multiprocessors Achieving Concurrency by Domain Decomposition 75

- G. Lyon and R. D. Snelick
Workloads, Observables, Benchmarks and Instrumentation 86

- F. Sötz
A Method for Performance Prediction of Parallel Programs 98

Parallel Linear Algebra

- S. Bondeli
Divide and Conquer: A New Parallel Algorithm for the Solution of a Tridiagonal Linear System of Equations 108
- J. Brehm, A. Böhm and J. Volkert
Sparse Matrix Algorithms for SUPRENUM 120
- E. M. Daoudi and G. Libert
Parallel Givens Factorization on a Shared Memory Multiprocessor 131

Logic Programming

Gao Yaoqing, Sun Chengzheng and Hu Shouren <i>Study of a Parallel Inference Machine for Parallel Execution of Logic Programs</i>	143
A. Gupta, A. Banerjea, V. Jha, V. Bafna and PCP Bhatt <i>Parallel Implementation of Logic Languages</i>	154
P. Kacsuk <i>Prolog Implementations on Parallel Computers</i>	166

Performance Monitoring and Debugging

B. Mohr <i>Performance Evaluation of Parallel Programs in Parallel and Distributed Systems</i>	176
M. Moser <i>The ELAN Performance Analysis Environment</i>	188
M. Zitterbart <i>Monitoring and Debugging Transputer-Networks with NETMON-II</i>	200

Algorithms for Matrix Factorization

Ch. H. Bischof and Ph. G. Lacroute <i>An Adaptive Blocking Strategy for Matrix Factorizations</i>	210
J. Du Croz, P. Mayes and G. Radicati <i>Factorizations of Band Matrices Using Level 3 BLAS</i>	222
M. Hegland <i>On the Computation of Breeding Values</i>	232

Large-Grain Data Flow

Kechang Dai <i>Code Parallelization for the LGDG Large-Grain Dataflow Computation</i>	243
D. C. DiNucci and R. G. Babb II <i>Development of Portable Parallel Programs with Large-Grain Data Flow 2</i>	253
O. C. Maquelin <i>ADAM: A Coarse-Grain Dataflow Architecture that Addresses the Load Balancing and Throttling Problems</i>	265
S. B. Murer <i>A Latency Tolerant Code Generation Algorithm for a Coarse Grain Dataflow Machine</i>	277

Compile-Time Analysis and Restructurers

R. Eigenmann, J. Hoeflinger, G. Jaxon and D. Padua <i>Cedar Fortran and Its Compiler</i>	288
---	-----

H. M. Gerndt and H. P. Zima <i>Optimizing Communication in Superb</i>	300
Sang Lyul Min, Yarsun Hsu and Hyoung-Joo Kim <i>A Design of Performance-optimized Control-based Synchronization</i>	312
K. L. Spier and B. K. Szymanski <i>Interprocess Analysis and Optimization in the Equational Language Compiler</i>	324
Architectures and Algorithms for Image Processing	
B. Chardonnens, R. D. Hersch and O. Kölbl <i>Transputer Based Distributed Cartographic Image Processing</i>	336
Gu Qing Zuo and An Zhong Wang <i>MPS – An Experimental Multi-Microprocessor Based Parallel System</i>	347
W. L. Nowinski <i>Parallel Implementation of the Convolution Method in Image Reconstruction</i>	355
D. Stokar, A. Gunzinger, W. Guggenbühl, E. Hiltebrand, S. Mathis, P. Schaeren , B. Schneuwly and M. Zeltner <i>SYDAMA II: A Heterogeneous Multiprocessor System for Real Time Image Processing</i>	365
Interconnection Networks	
A. Harassis, C. Jam and A. Ambler <i>Analysis and Design of Circuit Switching Interconnection Networks Using 4x4 Nodes</i>	374
R. Holzner and S. Tomann <i>Design and Simulation of a Multistage Interconnection Network</i>	385
R. J. Richter <i>A Reconfigurable Interconnection Network for Flexible Pipelining</i>	397
Load Balancing and the Mapping Problem	
J. E. Boillat and P. G. Kropf <i>A Fast Distributed Mapping Algorithm</i>	405
F. Dehne and M. Gastaldo <i>A Note on the Load Balancing Problem for Coarse Grained Hypercube Dictionary Machines</i>	417
P. Eklund and M. Kaufmann <i>Hierarchical Wiring in Multigrids</i>	423
Efficient Use of Vector Processors	
L. Gross, P. Sternecker and W. Schönauer <i>Optimal Data Structures for an Efficient Vectorized Finite Element Code</i>	435

O. Haan and W. Waelde
FFTVP LIB, a Collection of Fast Fourier Transforms for Vectorprocessors 447

H. Weerpals
Improving the Vector Performance via Algorithmic Domain Decomposition 458

Communication Issues

J-Y. Blanc and D. Trystram
Implementation of Parallel Numerical Routines Using Broadcast Communication Schemes 467

P. Istavrinos and L. Borrmann
A Process and Memory Model for a Parallel Distributed-Memory Machine 479

L. Mugwaneza, T. Muntean and I. Sakho
A Deadlock Free Routing Algorithm with Network Size Independent Buffering Space 489

Process Partitioning and Work Distribution

R. Beccard and W. Ameling
From Object-Oriented Programming to Automatic Load Distribution 502

F. Bieler
Partitioning Programs into Processes 513

R. Jakob and H. F. Jordan
An MIMD Execution Environment with a Fixed Number of Processes 525

Performance Considerations

B. A. W. Baugstø, J. F. Greipsland and J. Kamerbeek
Sorting Large Data Files on POOMA 536

R. Knecht
Parallelizing Divide-and-Conquer Algorithms - Microtasking versus Autotasking 548

E. Schnepf
The Performance of Linear Algebra Subprograms on the Siemens S Series 559

Reconfigurable and Scalable Systems

K. Boyanov and K. Yanev
A Family of Highly Parallel Computers 569

F. Höpfl, J. Schirrmacher and M. Trent
A Distributed Shared Memory Multiprocessor Kit with Scalable Local Complexity ... 581

M. Thapar and B. Delagi
Scalable Cache Coherence for Large Shared Memory Multiprocessors 592

Concurrency Control

V. Issarny <i>Design and Implementation of an Exception Handling Mechanism for Communicating Sequential Processes</i>	604
H-J. Plewan and P. Schlenk <i>Creating and Controlling Concurrency in Object Oriented Systems - A Case Study</i> ..	616
J. Rost and E. Maehle <i>A Distributed Algorithm for Dynamic Task Scheduling</i>	628

Transputer Tools and Applications

J.-M. Adamo and Ch. Bonello <i>TéNOR++: A Dynamic Configurer for SuperNode Machines</i>	640
G. W. Chege, R. W. Taylor and J. M. Tealby <i>Parallel Modelling of Electromagnetic Field Scattering: A New Approach Using the Edinburgh Concurrent Supercomputer Facility</i>	652
G. J. Shaw, A. Stewart and L. C. Waring <i>3D Multigrid Correction Methods for Transputer Networks</i>	665

Cellular/Systolic Architectures and Algorithms

J. H. Gonçalves Romero <i>A Comparative Study of Two Wavefront Implementations of a LU Solver Algorithm</i>	672
S. G. Sedukhin <i>Systolic Array Architecture for Two-Dimensional Discrete Fourier Transform</i>	682
A. Zsótér, T. Legendi and G. Balázs <i>Design and Implementation of M1 Cellprocessor</i>	692

Implementation Issues for Novel Architectures and Languages

H. Garsden and A. L. Wendelborn <i>A Comparison of Microtasking Implementations of the Applicative Language SISAL</i>	697
Guang R. Gao, H. H. J. Hum and Yue-Bong Wong <i>An Efficient Scheme for Fine-Grain Software Pipelining</i>	709
D. H. Grit <i>Sisal on a Message Passing Architecture</i>	721

The TOPSYS Tool Environment

Th. Bemmerl <i>The TOPSYS Architecture</i>	732
---	-----

Th. Bemmerl and Th. Ludwig <i>MMK - A Distributed Operating System Kernel with Integrated Dynamic Loadbalancing</i>	744
Th. Bemmerl, R. Lindhof and Th. Treml <i>The Distributed Monitor System of TOPSYS</i>	756
Array Processors and Applications	
M. Clint, J. S. Weston and C. W. Bleakney <i>Hybrid Algorithms for the Eigensolution of Large Sparse Symmetric Matrices on the AMT DAP 510</i>	766
P. Flanders <i>Virtual Systems Architecture on the AMT DAP</i>	774
M. Schäfer <i>Numerical Simulation of Thermal Convection on SIMD Computers</i>	786
High-Performance Systems and Accelerators	
M. Makhaniok, V. Cherniavsky, R. Männer and O. Stucky <i>Massively Parallel Realization of Logical Operations in Distributed Parallel Systems</i>	796
N. N. Mirenkov <i>High-Performance Computer System "SIBERIA"</i>	806
M. Ward, P. Townsend and G. Watzlawik <i>EDS Hardware Architecture</i>	816
Visualization and Runtime Analysis	
F. Abstreiter <i>Visualizing and Analysing the Runtime Behavior of Parallel Programs</i>	828
Th. Bemmerl, O. Hansen and Th. Ludwig <i>PATOP for Performance Tuning of Parallel Programs</i>	840
S. Sharma <i>Real-Time Visualization of Concurrent Processes</i>	852
Algorithmic Studies for Hypercube-Type Systems	
M. Cosnard and J-L. Philippe <i>Achieving Superlinear Speedups for the Multiple Polynomial Quadratic Sieve Factoring Algorithm on a Distributed Memory Multiprocessor</i>	863
M. Cosnard and P. Fraigniaud <i>A Performance Analysis of Network Topologies in Finding the Roots of a Polynomial</i>	875
M. Vajterščík <i>Parallel Multigrid Algorithms for some Specialized Computer Systems</i>	887

Computation Race	897
Authors Index	899

Committees

STANDING COMMITTEE

W. Händler	Univ. Erlangen (FRG)
	Chairman
P.C.P. Bhatt	IIT Delhi (IND)
K. Boyanov	IMIS Sofia (BG)
H. Burkhardt	Univ. Basle (CH)
M. Cosnard	ENS Lyon (F)
L.M. Delves	Univ. Liverpool (UK)
I. Plander	Ac. Bratislava (CSFR)

STEERING COMMITTEE

H. Burkhardt	Univ. Basle (CH)
	General Chairman
A.P. Speiser	ABB Baden (CH)
	Honorary Chairman
W. Gander	ETH Zurich (CH)
M. Gutknecht	ETH Zurich (CH)
A. Kündig	ETH Zurich (CH)
E. Rothauser	IBM Ruschlikon (CH)

PROGRAM COMMITTEE

H. Burkhardt	Univ. Basle (CH)
	Chairman
H. Aiso	Keio Univ. (J)
R.G. Babb II	Oregon Univ. (USA)
V. P. Bhatkar	CDAC Pune (IND)
P.C.P. Bhatt	IIT Delhi (IND)
K.C. Dai	GMD Berlin (FRG)
L.M. Delves	Univ. Liverpool (UK)
R. Eigenmann	Univ. Illinois (USA)
Ph. de Forcrand	ETH Zurich (CH)
W. Gander	ETH Zurich (CH)
R. Gruber	EPF Lausanne (CH)
D. Haupt	RWTH Aachen (FRG)
Ch. Jesshope	Univ. Southampton (UK)
G. Joubert	Philips Eindhoven (NL)
M. Kaiserswerth	IBM Ruschlikon (CH)
A. Kündig	ETH Zurich (CH)
T. Lake	Glossa Reading (UK)
O. Lange	TU Hamburg (FRG)
T. Legendi	Cellware Budapest (H)
H. Liddell	Queen Mary Coll. (UK)
P. Meier	Univ. Zurich (CH)

T. Muntean	Univ. Grenoble (F)
J.D. Nicoud	EPF Lausanne (CH)
E. Odijk	Philips Eindhoven (NL)
J. Pachl	IBM Ruschlikon (CH)
D.A. Padua	Univ. Illinois (USA)
D. Parkinson	Queen Mary Coll. (UK)
R.H. Perrott	Univ. Belfast (UK)
B. Quatember	Univ. Innsbruck (A)
J.K. Reid	Harwell Lab. (UK)
L. Richter	Univ. Zurich (CH)
B. Sendov	Academy Sofia (BUL)
D. Sorensen	Univ. Houston (USA)
O. Sykora	Ac. Bratislava (CSFR)
M. Vajtersic	Ac. Bratislava (CSFR)
M. Vannesci	Univ. Pisa (I)
A. J. Vasconcelos	Unipede Brussels (B)
R. Wait	Univ. Liverpool (UK)
T. Yuba	Tsukuba-shi (J)
C. Yen	Beijing Polytech. (PRC)

AWARDS COMMITTEE

J. Nievergelt	ETH Zurich (CH)
	Chairman
M. Annaratone	ETH Zurich (CH)
J. Dongarra	Univ. of Tennessee (USA)
I. Duff	Harwell Lab. (UK)
W. Händler	Univ. Erlangen (FRG)
H. Jordan	Univ. Colorado (USA)
P. Kropf	Univ. Berne (CH)
E. Rothauser	IBM Ruschlikon (CH)
H. Simon	Nasa Ames (USA)
J. Staunstrup	Univ. Lyngby (DK)
P. Stucki	Univ. Zurich (CH)

ORGANIZING COMMITTEE

E. Rothauser	IBM Ruschlikon (CH)
	Chairman
P. Arbenz	ETH Zurich (CH)
A. Friedli	ETH Zurich (CH)
J. Halin	ETH Zurich (CH)
R. Henzi	Sulzer Winterthur (CH)
W. Juling	RWTH Aachen (FRG)
H. Liddell	Queen Mary Coll. (UK)
K.D. Reinartz	Univ. Erlangen (FRG)
R. Wait	Univ. Liverpool (UK)

Referees

M.Annaratone	ETH Zurich (CH)	B.B.Madan	IIT Delhi (IND)
P.Arbenz	ETH Zurich (CH)	E.Maehle	Univ. Paderborn (FRG)
R.G.Babb II	Oregon Univ.(USA)	R.Männer	Univ. Heidelberg (FRG)
V. P.Bhatkar	CDAC Pune (IND)	P.Meier	Univ. Zurich (CH)
P.C.P.Bhatt	IIT Delhi (IND)	Ma.Miyakawa	Tsukuba-shi (J)
V.C.Bhavsar	CDAC Pune (IND)	M.Moser	ETH Zurich (CH)
H.Bieri	Univ. Berne (CH)	T.Muntean	Univ. Grenoble (F)
A.Bode	TU Munich (FRG)	H.H.Nägeli	Univ. Neuchâtel (CH)
J.Boillat	Univ. Berne (CH)	J.D.Nicoud	EPF Lausanne (CH)
H.Burkhart	Univ. Basle (CH)	J.Nievergelt	ETH Zurich (CH)
A.Coen	Politech.di Milano (I)	E.Odijk	Philips Eindhoven (NL)
M.Cosnard	ENS Lyon (F)	K.Ohmaki	Tsukuba-shi (J)
K.C.Dai	GMD Berlin (FRG)	J.Pachl	IBM Ruschlikon (CH)
M.Dal Cin	Univ. Erlangen (FRG)	D.A.Padua	Univ. Illinois (USA)
K.Decker	Univ. Berne (CH)	D.Parkinson	Queen Mary College (UK)
L.M.Delves	Univ. Liverpool (UK)	R.H.Perrott	Univ. Belfast (UK)
J.Dongarra	Univ.of Tennessee (USA)	W.P.Petersen	IPS Zürich (CH)
I.Duff	Harwell Lab. (UK)	B.Quatember	Univ. Innsbruck (A)
R.Eigenmann	Univ. Illinois (USA)	J.K.Reid	Harwell Lab. (UK)
W.Erhard	Univ..Erlangen (FRG)	K.D.Reinartz	Univ. Erlangen (FRG)
C.Falcó-Korn	Univ. Basle (CH)	R.Reith	Univ. Basle (CH)
B.Faltungs	EPF Lausanne (CH)	L.Richter	Univ. Zurich (CH)
Flück	EPF Lausanne (CH)	M.G.Sami	Politech.di Milano (I)
Ph. de Forcrand	ETH Zurich (CH)	B.Sanders	ETH Zurich (CH)
A.Friedli	ETH Zurich (CH)	H.Schmeck	Univ. Kiel (FRG)
W.Gentzsch	FH Regensburg (FRG)	H.Scholian	ETH Zurich (CH)
R.Gruber	EPF Lausanne (CH)	P.Schorn	ETH Zurich (CH)
D.W.Gruntz	ETH Zurich (CH)	D.Sehr	Univ.of Illinois (USA)
A.Gunzinger	ETH Zurich (CH)	J.Seib	Univ. Mannheim (FRG)
M.Gutknecht	ETH Zurich (CH)	S.Sekiguchi	Tsukuba-shi (J)
Gutzmann	Univ. Erlangen (FRG)	B.Sendov	Academy Sofia (BUL)
St.Gutzwiller	Univ. Basle (CH)	H.Simon	NASA Ames (USA)
A.Hagerer	Univ. Passau (FRG)	F.Sötz	Univ.Erlangen (FRG)
W.Händler	Univ. Erlangen (FRG)	J.Staunstrup	TU of Denmark (DK)
T.Härder	Univ. Kaisersl. (FRG)	D.Stokar	ETH Zurich (CH)
D.Haupt	RWTH Aachen (FRG)	A.Strey	Univ. Erlangen (FRG)
R.Henzi	Sulzer Informatik (CH)	P.Stucki	Univ. Zürich (CH)
R.Herbin	EPLF Lausanne (CH)	O.Sykora	Ac. Bratislava (CSFR)
D.Hogreve	Univ. Berne (CH)	C.Szyperski	ETH Zurich (CH)
F.Hosfeld	KFA (FRG)	H.Thoma	Ciba-Geigy Basle (CH)
Ch.Jesshope	Univ. Southampton (UK)	J.Tusk	Philips Eindhoven (NL)
H.Jordan	Univ. of Colorado (USA)	Ch.Ullrich	Univ. Basle (CH)
G.Joubert	Philips Eindhoven (NL)	M.Ulot	Philips Eindhoven (NL)
W.Juling	RWTH Achen (FRG)	M.Vajtersic	Ac. Bratislava (CSFR)
M.Kaiserswerth	IBM Ruschlikon (CH)	M.Vannesci	Univ. Pisa (I)
J.P.Katoens	Philips Eindhoven (NL)	A.J.Vasconcelos	Unipede Brussels (B)
H.Kirrmann	ABB (CH)	U.von Matt	ETH Zurich (CH)
R.Klar	Univ. Erlangen(FRG)	R.Wait	Univ. Liverpool (UK)
P.Kropf	Univ. Berne (CH)	St.Waser	Univ. Basle (CH)
A.Kündig	ETH Zurich (CH)	D.Würtz	ETH Zurich (CH)
T.Lake	Glossa Reading (UK)	C.Yen	Beijing Polytechnic (PRC)
O.Lange	TU Hamburg (FRG)	T.Yuba	Tsukuba-shi (J)
H.Liddell	Queen Mary College (UK)		