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Preface

Ultra-low voltage nano-scale large-scale integrated circuits (LSIs) are becoming more important to ensure the reliability of miniaturized devices, to meet the needs of a rapidly growing mobile market, and to offset a significant increase in the power dissipation of high-end microprocessor units. Such LSIs cannot not be made without ultra-low voltage nano-scale memories because they need low-power large-capacity memories. Many challenges arise, however, in the process of achieving such memories as their devices and voltages are scaled down below 100 nm and sub-1-V. A high signal-to-noise (S/N) ratio design is necessary in order to cope with both a small signal voltage from low-voltage memory cells and with large amounts of noise in a high-density memory-cell array. Moreover, innovative circuits and devices are needed to resolve the increasing problems of leakage currents when the threshold voltage (V_t) of MOSFETs is reduced and serious variability in speed and leakage occur. Since the solutions to these problems lie across different fields, e.g., digital and analog, and even SRAM and DRAM, a multidisciplinary approach is needed.

Despite the importance of this field, there are few authoritative books on ultra-low voltage nano-scale memories. This book has been systematically researched and is based on the authors' long careers in developing memories, and low-voltage designs in the industry. Ultra-Low Voltage Nano-Scale Memories gives a detailed explanation of various circuits that the authors regard as important because the circuits covered range from basic to state-of-the-art designs. This book is intended for both students and engineers who are interested in ultra-low voltage nano-scale memory LSIs. Moreover, it is instructive not only for memory designers, but also for all digital and analog LSI designers who are at the leading edge of such LSI developments.

Chapter 1 describes the basics of digital, analog, and memory circuits, and low-voltage related circuits. First, the basics of LSI devices, leakage currents, and CMOS digital and analog circuits including circuit models are discussed. Then the basics of memory LSIs, DRAMs, SRAMs, and flash memory are explained, followed by a discussion of memory related issues such as soft errors, redundancy, and error checking and correcting (ECC) circuits. Issues related to voltage, such as the scaling law, power-supply schemes, and trends in power-supply voltages are also described. Finally, various power-supply management issues for future memory and on-chip voltage converters are briefly discussed.

Chapter 2 describes ultra-low voltage nano-scale DRAM cells. First, the trends in DRAM-cells and 1-T-based DRAM-cells are discussed. After that, the

design of the folded-data-line 1-T cell is described five ways: in terms of the lowest necessary V_t and word voltage, the signal charge and the signal voltage, noise sources, the gate-over drive of the sense amp, and noise reductions. Open-data-line 1-T cells and state-of-the-art DRAM cells, such as the two-transistor (2-T) DRAM cell, the so-called 'twin cell', as well as a double-gate fully-depleted SOI 2-T cell, and gain cells are also explained.

Chapter 3 describes ultra-low voltage nano-scale SRAM cells. An explanation of the recent trends in SRAM-cell developments, is followed by a discussion of the leakage currents, and the voltage margin of 6-T SRAM cells, as well as their improvements. Finally, the 6-T SRAM cell is compared with the 1-T cell in terms of its voltage margin and soft error immunity.

Chapter 4 describes various circuit techniques that are used to reduce subthreshold leakage currents in RAM peripheral circuits. The basic principles of how to reduce leakage are described, with particular emphasis on the use of gate-source reverse biasing schemes. Various biasing schemes are discussed in detail, followed by applications to RAM cells and peripheral circuits in both standby and active modes.

Chapter 5 deals with the issue of variability in the nanometer era. The main focus is leakage and speed variations that are caused by variations in V_t. Various solutions with redundancy and ECC, layout, controls of internal supply voltages, and new devices such as planar double-gate fully-depleted SOI are discussed.

Chapter 6 describes the reference voltage generators that provide reference voltages for other converters. Various generators such as V_t-referenced, V_t-difference, band-gap generators, voltage trimming circuits, and burn-in test capability are described in detail.

Chapter 7 describes voltage down-converters in terms of their basic design concept, transient characteristics and phase compensation as well as their power-supply rejection ratio. Half-V_{DD} generators are also briefly discussed.

Chapter 8 deals with the circuit configurations of various voltage-up converters and negative voltage generators. Basic voltage converters with capacitors, Dickson-type voltage multipliers, and switched-capacitor-type voltage multipliers are explained and compared. Level monitors are also discussed.

Chapter 9 describes high-voltage tolerant circuit techniques that manage the voltage differences between peripheral circuits as well as between internal circuits and interface circuits of chips operating at a high external voltage.

We are indebted to many people, especially to our research colleagues at the Hitachi Central Research Laboratory, Tokyo who have collaborated with us, and one particular member of the administrative team, Ms. Anzai. They have offered support, advice, and the material needed to complete our work. Without their support this book would not have been possible.

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Tokyo, September 25, 2006

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