Run-time Adaptation for Reconfigurable Embedded Processors

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Abbreviations

AC	Atom container: a part of the reconfigurable fabric that can be dynamically reconfigured to contain an atom, i.e. an elementary data path
AGU	Address generation unit
ALU	Arithmetic logic unit
ASF	Avoid software first: a reconfiguration-sequence scheduling algorithm, as presented in Sect. 4.5
ASIC	Application-specific integrated circuit
ASIP	Application-specific instruction set processor
BC	Bus connector: connecting an → AC to the atom infrastructure
BRAM	Block → RAM: an on-chip memory block that is available on Virtex → FPGAs
cISA	core Instruction Set Architecture: the part of the instruction set that is implemented using the (nonreconfigurable) core pipeline; can be used to implement → SIs as well, as presented in Sect. 5.2
CLB	Configurable logic block: part of an → FPGA, contains multiple → LUTs
CPU	Central processing unit
DCT	Discrete cosine transformation: a computational kernel that is used in H-264 video encoder
EEPROM	Electrically erasable programmable read only memory
FB	Forecast block: indicated by an → FI, containing a set of → SIs with a → FV per SI
FI	Forecast instruction: a special → HI that indicates an → FB
FIFO	First-in first-out buffer
FPGA	Field programmable gate array: a reconfigurable device that is composed as an array of → CLBs, → BRAMs, and further components
FPS	Frames per second

FSFR	First select, first reconfigure: a reconfiguration-sequence scheduling algorithm, as presented in Sect. 4.5
FSL	Fast simplex link: a special communication mechanism for a MicroBlaze processor
FSM	Finite state machine
FV	Forecast value: the expected number of → SI executions for the next computational block, part of the information in an → FB
GPP	General purpose processor
GPR	General purpose register file
GUI	Graphical user interface
HEF	Highest efficiency first: reconfiguration sequence-scheduling algorithm, as presented in Sect. 4.5
HI	Helper instruction: an assembly instruction that is dedicated to system support (e.g., an → FI); not part of the → cISA and not an → SI
HT	Hadamard transformation: a computational kernel that is used in H-264 video encoder
IP	Intellectual property
ISA	Instruction set architecture
ISS	Instruction set simulator
KB	Kilo byte (also KByte): 1,024 byte
LSU	Load/store unit
LUT	Look-up table: smallest element in an → FPGA, part of a → CLB; configurable as logic or memory
MB	Mega byte (also MByte): 1,024 → KB
MinDeg	Minimum degradation: an atom replacement algorithm, as presented in Sect. 4.6
MUX	Multiplexer
NOP	No operation: an assembly instruction that does not perform any visible calculation, memory access, or register manipulation
NP	Nondeterministic polynomial: a complexity class that contains all decision problems that can be solved by a nondeterministic Turing machine in polynomial time
OS	Operating system
PCB	Printed circuit board
PRM	Partially reconfigurable module
PSM	Programmable switching matrix

RAM	Random access memory
RFU	Reconfigurable functional unit: denotes a reconfigurable region that can be reconfigured toward an SI implementation
RISPP	Rotating instruction set processing platform
SI	Special instruction
SJF	Shortest job first: a reconfiguration sequence-scheduling algorithm, as presented in Sect. 4.5
SPARC	Scalable processor architecture: processor family from Sun Microsystems; used for the → RISPP prototype
VLC	Variable length coding: a computational kernel that is used in H-264 video encoder
VLCW	Very long control word: configuration bits for the coarse-grained reconfigurable atom infrastructure, i.e. determining the operation mode and connection of the → ACs, → BC, → AGUs, and → LSUs

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