Test and Diagnosis for Small-Delay Defects

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To my parents
MT

To my parents, Maojun and Cuicui:
Thanks for your encouragement and support
KP

To my students over the years and to the tradition of excellence that they have established
KC

Preface

Electronic devices play a very important part in modern human life. As the demand of the market increases, and the development of manufacturing technologies further advances, more and more transistors are being packed into chips with ever increasing operating frequencies for higher functional density. Nanometer-scale technology poses new challenges for both design and test engineers, since scaling technologies provides us not only with higher integration and enhanced performance in designs, but also with increased manufacturing-related defects.

The shrinking of technology has introduced more variation to designs and has made design features more probabilistic. Furthermore, the shrinking of technology, along with the long interconnects required by very large scale designs, has also increased on-chip coupling capacitances. Scaled power supply voltages can be applied to lower power consumption in the circuit. However, reducing the power supply voltage also compromises noise immunity, impacting the signal integrity of the design. On the other hand, the market is always requiring higher test quality and lower failure rates, measured in defects per million (DPM). As a result, testing has become one of the most challenging tasks for nanometer-technology designs, and the cost for testing per transistor is increasing as we try to meet these challenges while keeping product quality high.

Due to lack of high quality functional tests, several fault models and testing methodologies have been developed for performing structural tests. At-speed delay testing using the transition delay fault (TDF) model has been done for decades to detect timing-related defects to ensure higher test quality and in-field reliability. The small-delay defect (SDD) is one such type of timing defect; it can be introduced by imperfect manufacturing processes as well as by pattern-induced on-chip noises, e.g., power supply noise (PSN) and crosstalk, causing chip failures by introducing extra delay to the design. As technology scales to 45 nm and below, testing for SDDs is necessary to ensure the quality and reliability of high-performance integrated circuits.

Traditional at-speed test methods cannot ensure high test coverage for SDDs with a reasonable pattern count. As a result of semiconductor industry demand for high quality patterns, commercial timing-aware automatic test pattern generation

(ATPG) tools have been developed for SDD detection. However, these ATPG tools suffer from large pattern counts and long CPU runtimes. Furthermore, none of these methodologies take into account the impact of process parameters, variations, or on-chip noises (e.g., process variations, PSN, and crosstalk) which are potential sources of SDDs. It is vital to diagnose these SDD failures and show which are the major causes of chip failures.

This book presents new techniques and methodologies to improve overall SDD detection with very small pattern sets. Based on implementations of these procedures on both academic and industrial circuits, these methods can result in pattern counts as low as a traditional 1-detect pattern set and long path sensitization and SDD detection similar to or even better than n-detect or timing-aware pattern sets. The important design parameters and pattern-induced noises such as process variations, PSN, and crosstalk are taken into account in the proposed methodologies. A diagnostic flow is also presented to identify whether the failure is caused by PSN, crosstalk, or a combination of these two effects.

Despite increasing concerns regarding SDDs in integrated circuits fabricated using the latest technologies, the area lacks a comprehensive book that introduces effective and scalable methodologies for screening and diagnosing SDDs that can be used by researchers and students in academia as well as by design and design-for-test (DFT) engineers in industry. The book will greatly benefit people who are interested in SDD detection and diagnosis. Instructors and students can use this book as a text book or reference book for their testing course. DFT engineers in industry can use this book to increase the efficiency of their SDD test patterns and reduce their testing costs.

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Acronyms

ALAPTF	As late as possible transition
ASIC	Application specific integrated circuit
ATE	Automatic test equipment
ATPG	Automatic test pattern generation
BIST	Built-in self-test
CF	Critical fault
CLT	Central limit theorem
CMOS	Complementary metal oxide semiconductor
CPU	Central processing unit
CUD	Circuit under diagnosis
CUT	Circuit under test
DC	Design Compiler
DDP	Delay defect probability
DDPM	Delay defect probability matrix
DEF	Design exchange format
DFF	Data flip-flop
DFM	Design-for-manufacturability
DFT	Design for test
DPM	Defective parts per million
DS	Detected by simulation
DSPF	Detailed standard parasitic format
DTC	Delay test coverage
DTPG	Diagnostic test pattern generation
DUT	Design under test
EDA	Electronic design automation
EMD	Embedded multi-detection
FCFI	First come first impact
GB	Gigabyte
HB	Hybrid method
IC	Integrated circuit
IEEE	Institute of electrical and electronics engineers

IP	Intermediate path
IWLS	International workshop on logic and synthesis
LOC	Launch-on-capture
LOS	Launch-on-shift
LP	Long path
LPthr	Long path threshold
MB	Megabyte
NLDM	Non-linear delay model
PDF	Probability density function
PDN	Power distribution network
PI	Primary input
PLL	Phase locked loop
PO	Primary output
PPSFP	Parallel-pattern single-fault propagation
PSN	Power supply noise
PV	Process variation
PVT	Process-voltage-temperature
PathDF	Path delay fault
RTL	Register-transfer level
SCAP	Switching cycle average power
SDD	Small-delay defect
SDF	Standard delay format
SDQL	Statistical delay quality level
SDQM	Statistical delay quality model
SE	Scan enable
SI	Signal integrity
SLAT	Single location at-a-time
SLthr	Slack threshold
SOC	System on chip
SP	Short path
SPEF	Standard parasitic exchange format
SRC	Semiconductor Research Corporation
SSTA	Statistical static-timing analysis
STA	Static-timing analysis
STAFAN	Statistical fault analysis
TA	Timing-aware
TDF	Transition-delay fault
TF	Total fault
TPG	Test pattern generator
TPI	Test point insertion
VCD	Value change dump
VDSM	Very deep sub-micron
VLSI	Very large scale integration
VLV	Very-low-voltage