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Sleiman Bou-Sleiman • Mohammed Ismail

Built-in-Self-Test and Digital Self-Calibration for RF SoCs

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Sleiman Bou-Sleiman
Analog VLSI Lab
The Ohio State University
Columbus, OH, USA
bousles@ece.osu.edu

Mohammed Ismail
Analog VLSI Lab
The Ohio State University
Columbus, OH, USA
ismail@ece.osu.edu

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To my loving family

Sleiman Bou-Sleiman

To the memory of my father,
Ismail El-Naggar

Mohammed Ismail

Preface

Single-chip radio systems, or Radio Frequency System-on-Chips (RF SoC), have become increasingly popular in recent years driven by the many aspects and intersections of technology, market demands, and consumer needs. Consumers now expect flawless and seamless communication capabilities in their increasingly connected world. Satisfying these demands is contingent on the abilities of scientists and engineers to continually advance the state-of-the-art in microelectronics processes and circuit designs. On the technology side, the improvements in silicon MOS have enabled high performance and highly integrated circuits, taking CMOS from a purely digital to a mixed-mode technology. For companies, the ability to provide platforms and systems built around a common technology, in smaller form factors and with more horsepower is a critical aspect of their survival in a deeply competitive market. The successful merge of the latest technology with the best design practices is the catalyst to first time design success.

The continual physical shrinking of device dimensions is allowing for more integration between the previously segmented digital logic, memory, analog, and radio frequency domains. While this co-existence may indicate a cost reduction on paper, in reality it might well turn out in the red. The smaller device sizes, while faster, are becoming increasingly unreliable. Although able to meet the performance requirements for high-speed analog and RF, the devices are not guaranteed to always run at their typical sweet spot. The drifts from the optimal operation are due to many factors related to the silicon process and its response to changes in voltage and temperature, or what is collectively named *PVT* (Process, Voltage, Temperature) variations. These variations are a problem in all the integrated domains of the chip; however, RF and millimeter-wave (mm-wave) circuits fail, in a more disproportionate manner, at sustaining proper operation over PVT. The reason being that RF devices, unlike digital circuits, do not function exclusively as on-off switches at either edges of operation but also exercise all the continuous states in between, and at very high frequencies. This makes them more prone to performance degradations and loss of yield when fabricated, in contrast to digital chips that can achieve near perfect yield. Putting both RF and digital together on a single chip, the hybrid system obviously inherits the lower yield, negating all the integration advantages.

Therefore, the RF portions, in a sense, represent the SoC's Achilles' heel; in essence, an overly powerful and densely integrated chip can be made useless by a smaller underperforming portion of the chip.

The ultimate goal is to increase the functional yield of the RF blocks by actively maintaining them in their optimal operating region. This proves to be a non-trivial task, as the operating conditions of the system at all times need to be known. While fabrication testing is one way to test how a chip performs after production, it cannot be all-inclusive of all operating conditions. Moreover, it is quite costly to fully verify each single chip rendering the validation task quite prohibitive. A solution would be to build self-testing, and eventually self-healing, systems. However, this demands a shift in design paradigms to include testing, early on, in the design phase, or what is dubbed as Design-for-Testability (DfT). While DfT's primary goal is to ease external testing of complex chips, an additional upgrade is highly desirable: the integration of the full testing functionality on-chip.

Built-in-Self-Test (BiST) techniques have already established themselves in the validation of digital blocks but are now becoming an increasingly active domain of research and development in RF. The notion of migrating RF test functionality to inside the chip brings us one step closer to cognitive-like radios. Self-awareness in RF systems is therefore a product of efficient on-chip test generation and result acquisition and interpretation. If RF/mm-wave blocks and systems can test for, and extract, their performance, then the ability to calibrate and cancel discrepancies can also be built into the system. Hence, Built-in-Self-Calibration (BiSC) can be layered on top of BiST to result in auto-correcting RF impairments at the block and system levels.

In this book, we discuss both BiST and BiSC in the context of RF SoCs. In Chapter 1, we describe CMOS' roadmap towards RF and mm-wave capabilities. The beneficial and adverse effects of technology scaling are highlighted showing the possibilities of increased integration as well as the problems associated with decreased device and circuit robustness. Chapter 2 describes the basics of communication systems and transceivers, while highlighting the most critical performance issues. System- and block-level metrics are presented along with RF built-in-testing schemes to reduce the costs of production testing. In Chapter 3, we express the requirements for building efficient true self-test mechanisms using on-chip resources not only as value-added elements but also as necessary components for successful first-pass success of RF and mm-wave SoCs. Simple additional circuits for test are therefore desirable; however, on-chip testing of radio frequency signal needs special attention, as these signals' properties are not easily interpretable. Hence, an efficient RF detector is presented with different implementations covering the RF and mm-wave spectra. In Chapter 4, the detector is used under different built-in-test schemes for parametric extraction of RF blocks. The self-testing of metrics such as gain, linearity, and quadrature mismatch is described with example test-benches and circuits. Chapter 5 takes the proposed on-chip test implementations and uses them to aid in the development of calibration techniques. These techniques aim at leveraging the strengths of the more robust parts of the system to cover up the weaknesses of the others. Therefore, the digital domain is fully exploited to augment the capabilities of RF circuits by providing them with the digital notion of programmability: an added degree of flexibility and tunability with the goal of enabling performance steering capabilities. Examples of RF Built-in-Self-Calibration using DSP-driven approaches are briefly highlighted and shown to re-adjust a failing circuit's operating conditions.

This book is intended for RF design engineers, system-on-chip design engineers as well as graduate students and researchers in the field. The material strives to present an approach and a description of a process that fits perfectly into the premise of, and promise of, highly performing first-time-right design of RF SoC moving into the nanometer regimes.

The work in this book has its roots in the PhD work of the first author at the Analog VLSI Lab at the Ohio State University. Both authors would like to acknowledge the support of colleagues at the Analog VLSI Lab and Electroscience Laboratory at the Ohio State University.

Columbus, OH

Sleiman Bou-Sleiman
Mohammed Ismail

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