# High Quality Test Pattern Generation and Boolean Satisfiability

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# Preface

The content of the book describes work that has been carried out in the Group of Computer Architecture at the University of Bremen, Germany over the last 5 years. Therefore, we would like to thank all the members of the group for their valuable help. Special thanks go to Daniel Tille and Görschwin Fey for many helpful discussions and support. Both are also co-authors of our previously published book *Test Pattern Generation using Boolean Proof Engines* which describes among other things the basics principles on which the content of this book is based on.

Various chapters of this book are based on scientific papers. Therefore, we would like to acknowledge the work of the co-authors of these papers Görschwin Fey, Hoang M. Le, Juergen Schloeffel and Daniel Tille. Since large parts of the work has been done in collaboration, our special thanks go to the Mentor Graphics Development group in Hamburg, Germany, especially to René Krenz-Bååth (now Hochschule Hamm-Lippstadt). Finally, we would like to thank Lisa Jungmann for her help with the cover design as well as Robert Wille, Judith End and Tom Gmeinder for proof-reading.

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Bremen

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# Contents

# List of Figures

# List of Tables

# List of Acronyms

| | |
|---|---|
| ARAP | As-Robust-As-Possible |
| ATE | Automatic Test Equipment |
| ATPG | Automatic Test Pattern Generation |
| BCP | Boolean Constraint Propagation |
| BDD | Binary Decision Diagram |
| CNF | Conjunctive Normal Form |
| CUT | Circuit Under Test |
| DCA | Dynamic Clause Activation |
| DFT | Design-For-Test |
| DTPG | Deterministic Test Pattern Generation |
| GDFM | Gate Delay Fault Model |
| IC | Integrated Circuit |
| IG | Implication Graph |
| ISAT | Incremental SAT |
| LC | Logic Class |
| LWL | Learned Watch List |
| ODC | Observability Don't Care |
| PBO | Pseudo-Boolean Optimization |
| PB-SAT | Pseudo-Boolean SAT |
| PDF | Path Delay Fault |
| PDFM | Path Delay Fault Model |
| PI | Primary Input |
| PO | Primary Output |
| PPI | Pseudo Primary Input |
| PPO | Pseudo Primary Output |
| RTPG | Random Test Pattern Generation |
| s-a-0 | Stuck-at-0 |
| s-a-1 | Stuck-at-1 |
| SAFM | Stuck-At Fault Model |
| SAT | Boolean Satisfiability, Satisfiable |

| | |
|---|---|
| SDD | Small Delay Defect |
| SWL | Structural Watch List |
| TF | Transition Fault |
| TFM | Transition Fault Model |
| UNSAT | Unsatisfiable |

# List of Symbols

| | |
|---|---|
| $\downarrow$ | falling transition |
| $\uparrow$ | rising transition |
| $\cdot$ | Boolean AND operator |
| $+$ | Boolean OR operator |
| $\odot$ | resolution operator |
| $\oplus$ | Boolean XOR operator |
| $\bar{\cdot}$ | Boolean NOT of $\cdot$ |
| $\rightarrow$ | implies |
| $\leftrightarrow$ | equivalence |
| $\Phi$ | CNF, set of clauses |
| $\Phi_{\text{dyn}}$ | dynamically extended CNF |
| $\Phi_F$ | fault-specific constraints |
| $\Psi$ | set of pseudo-Boolean constraints |
| $\psi$ | pseudo-Boolean constraint of $\Psi$ |
| $\eta$ | Boolean encoding |
| $\kappa$ | conflict |
| $\lambda$ | arbitrary literal |
| $\omega$ | clause of $\Phi$ |
| $\omega_C$ | conflict clause |
| $@x$ | at decision level $x$ |
| $\mathbb{B}$ | set of Boolean values $\{0,1\}$ |
| $\mathscr{C}$ | circuit |
| $\mathscr{F}$ | set of flip-flops |
| $F$ | fault |
| $f$ | flip-flop $\in \mathscr{C}$, faulty line of gate |
| $\mathscr{F}(g)$ | transitive fanin of $g$ |
| $\mathscr{G}$ | set of gates |
| $g$ | gate $\in \mathscr{C}$ |
| $h$ | successor gate of $g$ |
| $\mathscr{I}$ | set of primary inputs |
| $i_1, \ldots, i_n$ | primary inputs of $\mathscr{C}$ |

| | |
|---|---|
| $\mathscr{J}$ | J-stack |
| $\mathscr{L}_x$ | multiple-valued logic with $x$ values |
| $\mathscr{O}$ | set of primary outputs |
| $o_1, \ldots, o_m$ | primary outputs of $\mathscr{C}$ |
| $\mathscr{P}$ | structural path of $\mathscr{C}$ |
| $\mathscr{S}$ | set of signal lines or connections |
| $s$ | signal line, connection |
| $t_i$ | initial (current) time frame |
| $t_{i+1}$ | final (next) time frame |
| $V$ | vector |
| $v$ | (Boolean) value |
| $X$ | set of Boolean variables, don't care value |
| $x_1, \ldots, x_n$ | Boolean variables |