

# Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs



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*To our families*



# Preface

As VLSI technology scales into nanometer regime, chip design engineering faces several challenges. One profound change in the chip design business is that engineers cannot realize the design precisely into the silicon chips. Chip performance, manufacture yield, and lifetime thereby cannot be determined accurately at the design stage accordingly. The main culprit here is that many chip parameters—such as oxide thickness due to chemical and mechanical polish (CMP) and impurity density from doping fluctuations—cannot be determined or estimated precisely and thus become unpredictable at device, circuit, and system levels, respectively. The so-called manufacturing process variations start to play an essential role, and their influence on the performance, yield, and reliability becomes significant. As a result, variation-aware design methodologies and computer-aided design (CAD) tools are widely believed to be the key to mitigate the unpredictability challenges for 45 nm technologies and beyond. Variational characterization, modeling, and optimization, hence, have to be incorporated into each step of the design and verification processes to ensure reliable chips and profitable manufacture yields.

The book is divided into five parts. Part I introduces basic concepts of many mathematic notations relevant to statistical analysis. Many established algorithms and theories such as the Monte Carlo method, the spectral stochastic method, and the principal factor analysis method and its variants will also be introduced. Part II focuses on the techniques for statistical full-chip power consumption analysis considering process variations. Chapter 3 reviews existing statistical leakage analysis methods, as leakage powers are more susceptible to process variations. Chapter 4 presents a gate-level leakage analysis method considering both inter-die and inter-die variations with spatial correlations using the spectral stochastic method. Chapter 5 tries to solve the similar problems in the previous chapter. But a more efficient, linear-time algorithm is presented based on a virtual grid modeling of process variations with spatial correlations. In Chap. 6, a statistical dynamic power analysis technique using the combined virtual grid and the orthogonal polynomial methods is presented. In Chap. 7, a statistical total chip power estimation method will be presented. A collocation-based spectral-stochastic-based method is applied to obtain the variational total chip powers based on accurate SPICE simulation.

Part III emphasizes on variational analysis of on-chip power grid networks under process variations. Chapter 8 introduces an efficient stochastic method for analyzing the voltage drop variations of on-chip power grid networks, considering log-normal leakage current variations with spatial correlation. Chapter 9 presents another stochastic method for solving the similar problem in the previous chapter. But model order reduction has been applied in this method to improve the efficiency of the simulation. Chapter 10 introduces a new approach to variational power grid analysis, where model order reduction techniques and variational subspace modeling are used to obtain the variational voltage drop responses.

Part IV of this book is concerned with statistical interconnect extraction and modeling under process variations. Chapter 11 presents a statistical capacitance extraction method using Galerkin-based spectral stochastic method. Chapter 12 discusses a parallel and incremental solver for stochastic capacitance extraction. Chapter 13 gives a statistical inductance extraction method by collocation-based spectral stochastic method.

Part V of this book focuses on the performance bound and statistical analysis of nanometer analog/mixed-signal circuits and the yield analysis and optimization based on statistical performance analysis and modeling. Chapter 14 presents performance bound analysis technique in s-domain for linearized analog circuits using symbolic and affine interval methods. Chapter 15 presents an efficient stochastic mismatch analysis technique for analog circuits using Galerkin-based spectral stochastic method and nonlinear modeling. Chapter 16 shows a yield analysis and optimization technique, and Chap. 17 describes a yield optimization algorithm by an improved voltage binning scheme.

The content of the book comes mainly from the recent publications of authors. Many of those original publications can be found at [http://www.ee.ucr.edu/~stan/project/sts\\_ana/main\\_sts\\_ana\\_proj.htm](http://www.ee.ucr.edu/~stan/project/sts_ana/main_sts_ana_proj.htm). Future errata and update about this book can be found at [http://www.ee.ucr.edu/~stan/project/books/book11\\_springer.htm](http://www.ee.ucr.edu/~stan/project/books/book11_springer.htm).

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