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Analog IC Placement Generation via Neural Networks from Unlabeled Data

Springer

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ISSN 2191-530X ISSN 2191-5318 (electronic)
SpringerBriefs in Applied Sciences and Technology
ISBN 978-3-030-50060-3 ISBN 978-3-030-50061-0 (eBook)
https://doi.org/10.1007/978-3-030-50061-0

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To all my friends

—António Gusmão

To Carla, João and Tiago

—Nuno Horta

To Alina, Íris and Ana

—Nuno Lourenço

To Daniela and Martim

—Ricardo Martins

Preface

The proliferation of electronic devices in recent years has triggered the increasing complexity of integrated circuits (ICs). While most of these electronics' high-level functions are implemented using digital circuitry, analog and mixed signal (AMS) circuits are still necessary and irreplaceable in the implementation of most interfaces and transceivers due to the inherent analog nature of those functionalities. While in digital design, an automated flow is well established, for AMS ICs the absence of effective and established computer-aided-design (CAD) tools for electronic design automation (EDA) poses the largest contribution to their bulky development cycles. To address this, long, iterative and error-prone designer intervention over the entire design flow is mandatory. Given the economic pressure for high-quality yet cheap electronics and challenging time-to-market constraints, there is an urgent need for EDA tools that increase the analog designers' productivity and improve the quality of resulting ICs.

In this book, an innovative approach to automate the placement task of analog IC layout design is presented, where artificial neural networks (ANNs) are trained to produce valid layouts at pushbutton speed. Standard ANN applications usually exploit the model's capability of describing a complex, harder to describe, relation between input and target data. For that purpose, ANNs are a mechanism to bypass the process of describing the complex underlying relations between data, by feeding it with a great number of previously acquired input/output data pairs that then the model attempts to copy. However, in the context of analog IC placement generation, the issue arises during the stages of data acquisition, since due to the complexity of the current placement generation flow, output data or labels are very costly to produce, i.e., producing output data in the form of a placement solution for a given input data (a specific circuit topology) is time consuming, and also, the production of a variety of these labels required for the usual neural network application is unrealistic. Therefore, a different approach is taken, since it is quite costly to produce the needed amount of target placements but it is not as complex to describe the relation that makes a placement robust, the model is trained to produce placements that fulfill the defined input/output data relation. The encoded relations are current-flow and symmetry constraints, that, according to analog IC designers,

are the most elementary and essential constraints to be considered. In this approach, the system relies on a mix of labeled and unlabeled data that consists of previously designed circuit topologies at sizing-level only, which are easier to obtain.

This book details the description of the input/output data relation that should be fulfilled. The developed description is mainly reflected in two of the system's characteristics, the shape of the input data and the minimized loss function. An efficient modulation of these components should be such that once fully trained, the model should be producing output data that fulfills the desired relation for the given training data, additionally, the model should be capable of efficiently generalizing the acquired knowledge for new examples, i.e., never seen input circuit topologies. In order to address the latter, an abstract and segmented description of both the input data and the objective behavior are developed so the model can identify, in new scenarios, sub-blocks found in the training data. The result is a device level description of the input topology focusing, for each device, on describing its relation to every other device in the topology. Through this description, an unfamiliar overall topology can be decomposed into devices subject to the same constraints as a device in one of the training topologies. Similarly, the desired relation encoded in the loss function directly quantifies the degree to which these device level constraints are being satisfied along with some optimization metrics, such as layout area or device overlap (both being minimized).

The trained ANNs are demonstrated to produce a variety of valid placement solutions even outside the scope of the seen training/validation sets, showing that the model is effectively identifying common components between newer topologies and reutilizing the acquired knowledge. Ultimately, the used methodology efficiently adapts to the given problem's context (high label production cost) and results in an efficient, inexpensive and fast model.

This book is organized into six chapters.

Chapter 1 gives an introduction to AMS systems-on-chip (SoC) design, with special focus given to automatic device placement in analog IC layout generation and the limitations that the current design flow faces. The standard procedures are presented. Furthermore, the concept of machine learning (ML) and the use of this branch of artificial intelligence (AI) as a step towards the production of EDA tools for analog and mixed signal ICs is introduced.

Chapter 2 thoroughly studies ANNs through the deconstruction of the ML model. Its several parts are described, and a comparison of the different used methods for each of these components is made, such as the functioning of each neuron, the learning process that makes use of optimization tools, the hyperparameters that define the model's architecture, and the influence of the selected features.

Chapter 3 explains the constraints which influence the process of layout generation, along with the description of four main approaches of existing EDA tools for analog placement/for analog IC layout.

Chapter 4 details the envisioned solution based on a past approach that is limited to a single circuit topology and punishes valid, innovative predictions. Attention is put into the development of the input features that expand the solution's scope and

increase generalization, and, the introduction of a new loss function that evaluates the prediction made through the fulfillment of the circuit's topological constraints.

Chapter 5 details the tests and analysis performed on the different ANN models. These models differ by the format of their input vector or by the loss function used during training, while the network's architecture is kept the same. The objective is to compare the impact of these key parts of the model.

Chapter 6 presents the conclusions of this book, as well as future directions for further applications of ANNs towards the automation of the placement process of analog IC layout design.

The work described in this book was funded by FCT/MCTES through national funds and when applicable co-funded EU funds under the project UIDB/EEA/50008/2020. Including internal research project LAY(RF)^2.

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Acronyms

AI	Artificial Intelligence
AMS	Analog and Mixed-Signal
ANN	Artificial Neural Networks
CAD	Computer Aided Design
CFSSA	Cascode Free Single Stage Amplifier
EDA	Electronic Design Automation
FSSA	Folded Single Stage Amplifier
IC	Integrated Circuit
ML	Machine Learning
MSE	Mean Squared Error
MSE-NP	Mean Squared Error—Non Polynomial Features
MSE-NPS	Mean Squared Error—Non Polynomial Features with Device Scrambling
MSE-P	Mean Squared Error—Polynomial Features
MSE-PS	Mean Squared Error—Polynomial Features with Device Scrambling
TLF	Topological Loss Function
SoC	Systems-on-Chip
SSA	Single Stage Amplifier