SERVAS! Secure Enclaves via RISC-V Authenticryption Shield

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Abstract

Isolation is a long-standing challenge of software security. Traditional privilege rings and virtual memory are more and more augmented with concepts such as capabilities, protection keys, and powerful enclaves. At the same time, we are evidencing an increased need for physical protection, shifting towards full memory encryption schemes. This results in a complex interplay of various security mechanisms, increasing the burden for system architects and security analysts.

In this work, we tackle the isolation challenge with a new isolation primitive called authenticryption shield that unifies both traditional and advanced isolation policies while offering the potential for future extensibility. At the core, we build upon an authenticated memory encryption scheme that gives cryptographic isolation guarantees and, thus, streamlines the security reasoning. We showcase the versatility of our approach by designing and prototyping SERVAS – an innovative enclave architecture for RISC-V. Unlike current enclave systems, SERVAS facilitates efficient and secure enclave memory sharing. While the memory encryption constitutes the main overhead, entering or exiting a SERVAS enclave requires only 3.5x of a simple syscall, instead of 71x for Intel SGX.

1 Introduction

Modern IT systems need to secure a multitude of applications against software attacks. Unfortunately, software vulnerabilities penetrate the whole software stack, affecting not only application software [12, 19, 80, 82] but also the operating system (OS) itself [10, 20, 28, 33, 36]. In the worst case, attackers can gain full control over the device [10, 33, 36].

To reduce the impact of vulnerability exploitation, different isolation mechanisms are deployed on all levels, e.g., to separate privileges [23], isolate individual processes [103], protect virtual machines [1,2,25,48], and segregate applications into smaller parts, also denoted as in-process isolation. Typical in-process isolation mechanisms are segmentation [43] and capabilities [95], memory coloring using, e.g., protection

keys [40, 77, 86], or enclaves. Enclaves give strong security guarantees even in the event of a system compromise and found ample resonance both in academia [9, 13–15, 22, 31, 32, 38, 53, 57, 62, 70, 73, 81, 83, 90, 100] and industry [6, 7, 34, 64].

In addition, cloud computing scenarios increasingly demand physical protection, for which transparent memory encryption is being deployed on modern CPUs [2,64]. While memory encryption works well for small workloads, worst-case throughput penalties surpass 400% for Intel SGX [37].

Unfortunately, reasoning about the security of the interplay between these mechanisms is becoming more and more complex when considering the whole zoo of isolation mechanisms. For example, the security of an application might depend on protection keys in combination with the Memory Management Unit (MMU) and the memory mappings configured by the operating system [47, 54, 103]. Unifying these isolation mechanisms is desirable from a security standpoint. On the other hand, most isolation mechanisms cover only a subset of isolation challenges. For example, SGX enclaves can isolate small portions of unprivileged user code, but their underlying memory encryption is not utilizable for other purposes.

In this work, we pursue a three-fold goal: First, we simplify the overall security reasoning by introducing a strong and generic isolation primitive. Second, we explore the synergies and features our isolation primitive offers over traditional isolation mechanisms. Third, we design a secure and feature-rich enclave architecture – arguably the most intricate endeavor. New Isolation Primitive. We introduce a new isolation primitive that unifies various isolation policies and is denoted as RISC-V Authenticryption Shield (RVAS). At its core, RVAS uses memory encryption to map isolation properties to the well-studied field of cryptography, counteracting both physical and software attacks. More specifically, if decryption succeeds, we know that the CPU and the memory are in a particular state. Thus, RVAS achieves memory isolation with cryptographic guarantees.

We design RVAS as an extension to the RISC-V instruction set architecture (ISA). RVAS builds upon an authenticated memory encryption scheme whose associated data input, which we call encryption tweak, is exposed to software. By controlling the encryption tweak, one can achieve domain separation and, thus, enforce a variety of different isolation mechanisms simultaneously, e.g., privilege separation, process isolation and virtual memory protection, segmentation, and page coloring. Traditionally, each of these mechanisms requires to securely store and manage trusted metadata (e.g., the address mapping or the page colors). RVAS implicitly secures this metadata by feeding it into the encryption tweak.

Achieving a proper generalization of encryption tweaks is non-trivial, however. Hence, RVAS composes the tweak of both critical CPU-internal data and software-defined values to account for a broad range of use cases.

SERVAS Enclaves. To showcase the versatility of RVAS, we use it to design a novel enclave system dubbed SERVAS, which has several advantages over existing enclave systems:

SERVAS protects enclaves against software and physical attacks by relying on a single mechanism, namely RVAS' cryptographic isolation. In contrast, Intel SGX protects enclaves against *physical* attacks via memory encryption while also preventing *software* attacks through a trusted metadata storage (*i.e.*, the so-called EPCM [43]). The EPCM needs to be maintained for each enclave page and kept in sync with the Translation Lookaside Buffer (TLB), for which SGX requires TLB flushes upon enclave invocations [21].

Our RVAS design makes the EPCM trusted metadata storage obsolete, which yields three advantages: First, we avoid TLB flushes and thus, achieve better enclave invocation performance. Second, we remove trust from the entire address translation, *i.e.*, the MMU and the TLB configuration, such that our security reasoning boils down to a proper encryption tweak management. Third, Intel SGX fixes the amount of encrypted enclave memory at boot time to typically 128 MB [35]. RVAS encryption, in contrast, can be applied to the whole DRAM and also to non-enclave code.

SERVAS introduces the novel concept of secure sharing of enclave memory. Secure sharing is a key requirement for many application scenarios, but it is impractical with current enclave systems (e.g., Intel SGX). Thus, enclave-to-enclave communication currently demands costly encryption and copying operations in software. SERVAS enables zero-cost secure data exchange by sharing specific encryption tweaks between eligible enclaves. Moreover, selective code deduplication reduces memory demands if the same enclave is invoked multiple times.

SERVAS is compatible with advanced enclave features such as dynamic enclave memory, swapping, and multithreading. As a proof of concept, we prototype RVAS on an FPGA by using the CVA6 RISC-V CPU together with an openly available encryption core. A small stateless Security Monitor (SM) running in RISC-V machine mode¹ ensures a proper tweak configuration for strongly-protected SERVAS enclaves.

We show that entering and exiting SERVAS enclaves only takes 3.5x the time of a syscall. Our evaluation indicates an overhead between 16.7% and 24.5% over the used encryption core for a broad selection of macrobenchmarks. We plan to open-source our prototype.

In summary, our contributions are as follows:

- A generic isolation primitive using authenticated memory encryption denoted as RISC-V Authenticryption Shield.
- A novel enclave architecture called SERVAS that leverages the RISC-V Authenticryption Shield.
- A novel and fast and secure memory sharing mechanism between enclaves.
- An evaluation of SERVAS in a set of micro- and macrobenchmarks.

Outline. The remaining paper is structured as follows: In Section 2, we discuss challenges of memory isolation. In Section 3, we discuss our generic isolation primitive RVAS. In Section 4, we present our SERVAS design, discuss how we use our components to build enclaves, and elaborate key points of their life-cycle. Section 5 gives implementation details of RVAS and SERVAS. It elaborates on the specifics of the instruction set extension, the construction of the tweak, and the API of our Security Monitor. Additionally, this section discusses how tweaks are cached and the benefits of separating them into a tweak cache. In Section 6, we give a security analysis. We evaluate our prototypes of RVAS and SERVAS in Section 7. We discuss related work in Section 8, future work in Section 9, and conclude the paper in Section 10.

2 Challenges of Memory Isolation

The fragmentation of isolation mechanisms makes it hard to analyze their security, especially if multiple mechanisms are combined. In this section, we give an overview of the most widely used isolation schemes and present their challenges concerning security and functional limitations we want to overcome. This overview paves the way for understanding how the RVAS design can solve these challenges in general (cf. Section 3) and for enclaves in particular (cf. Section 4).

2.1 Process Isolation

Process isolation comprises separating privileges between an operating system and user processes and isolating processes from each other. Privilege separation is achieved via privilege rings – one of the coarsest protection mechanisms available in CPUs that protect privileged CPU resources from unprivileged access. However, to be secure, privileged software also needs to protect its own memory and user memory using the virtual memory subsystem, as follows:

Challenge C₁: "The privileged software must ensure that the virtual memory mappings of **all** unprivileged processes (i) cannot access privileged memory, and (ii) are not unintentionally aliasing with each other."

¹This is loosely comparable to CPU microcode used for Intel SGX logic.

Unfortunately, analyzing the security of process isolation is far from trivial [47,54,103] and requires a deep understanding of the memory management facilities of modern operating systems. Moreover, the virtual memory mapping is a favored attack target [24] since a single bit flip in the page tables can suffice for privilege escalation attacks [87].

2.2 In-Process Isolation

Segmentation is an isolation mechanism to more finely separate parts within an application from each other. It usually confines memory accesses within predefined address ranges. Segmentation also forms the basis of hardware capabilities [95]. However, these systems are not suitable for enforcing policies across application boundaries. E.g., a segment to protect an application's cryptographic key is typically not respected by other applications (in case of shared memory) or by the OS.

Challenge C_2 : "Segmentation should also allow flexible cross-application policies."

Memory Coloring is another in-process isolation mechanism labeling each memory block with a different "color". The memory only becomes accessible to the application if the corresponding color is loaded in a special register. Unfortunately, the number of colors is often quite limited [72], inhibiting fine-grain use cases. Moreover, memory coloring is not enforced across application boundaries, making it unsuitable for sharing data with other applications.

Challenge C_3 : "Memory coloring should provide significantly more colors and also allow cross-application policies."

2.3 Enclaves

Memory Mapping. Enclaves present an inverse problem of process isolation: an unprivileged software – the enclave – wants to protect itself from privileged software that manages the enclave's virtual memory mapping. This leads to:

Challenge C_4 : "The memory mapping of enclaves must be protected against privileged software."

Protecting memory mappings against privileged attackers is challenging because privileged software is in legitimate charge of managing memory. For example, if the OS maps memory to a wrong location, the enclave could be tricked into accessing the wrong buffer, leaking secrets, or corrupting its sensitive memory. Also, by mapping code pages in a bogus way, the enclave could be forced to execute unintended functions or bypass security checks. Furthermore, manipulation of page table attributes could violate security assumptions and, e.g., cause data pages to become executable. Three security invariants need to hold, to prevent such attacks:

Attribute Invariant \mathcal{IA} : "Enclave pages must only be mapped with their intended page table attributes."

Spatial Invariant \mathcal{IS} : "A physical enclave page must only be mapped to its corresponding virtual page."

Temporal Invariant \mathcal{IT} : "At any time for every virtual enclave page, there must be at most one valid physical page mapping."

The *temporal invariant* specifically addresses double mapping attacks: If an attacker obtains two valid mappings for the same virtual enclave page, the OS could silently replace the underlying physical page in order to replay old data to the enclave and, thus, tamper with its execution. This is especially relevant for dynamic enclave memory, swapping, and shared memory, where the memory utilization varies over time.

Protected Sharing is an important feature required for the interaction between applications. In an unprotected setting, this interaction is achieved via shared memory. However, in the context of enclaves, there is a hard isolation boundary that prohibits secure, shared memory by design. In Intel SGX, data exchange is only possible via untrusted application memory, and enclaves need to manually encrypt data being sent.

Challenge C_5 : "Shared memory must allow for efficient and confidential interaction between different enclaves."

2.4 Memory Encryption

Apart from these architectural challenges, the DRAM presents a substantial physical attack surface, allowing passive [5,39,60] and active [50] attacks to infer or tamper with secret data stored in memory. To isolate data from physical attacks and ensure its integrity, encrypting and authenticating the DRAM is necessary. Memory encryption should not be restricted to specific code (e.g., enclaves) or specific parts of the DRAM.

Challenge C_6 : "The DRAM shall be hardened against active and passive physical attacks."

3 RISC-V Authenticryption Shield (RVAS)

RVAS harnesses authenticated memory encryption as a single, generic mechanism to cryptographically enforce the challenges for memory isolation expressed in Section 2. At its core, we use a Memory Encryption Engine (MEE) for encrypting the DRAM and incorporate a security context into its tweak input (*i.e.*, the associated data). If encrypted data is accessed with the wrong security context, the MEE triggers an authentication error. Since the MEE gives cryptographic security guarantees for detecting authentication issues, the security argumentation for all the isolation policies boils down to one question: *Who controls the security context?*

The composition of the security context arguably lies at the heart of RVAS. For readability, we also call it "tweak" in the rest of the paper. The tweak consists of both software-and CPU-defined components, allowing for fine-grained, unforgeable isolation. We designed an Instruction Set Architecture (ISA) extension for configuring the tweak (cf. Section 5), which makes RVAS a powerful and generic isolation primitive based on strong cryptographic segregation.

In this section, we first discuss the composition of the RVAS tweak. Second, we sketch how RVAS solves the challenges defined in Section 2. We will concretely instantiate and analyze SERVAS enclaves addressing challenges C_2 – C_6 in Sections 4 and 6. Finally, we highlight requirements for the MEE to support RVAS.

3.1 RVAS tweak design

A core contribution of RVAS lies in the way we compose the tweak used by the Memory Encryption Engine (MEE) from both software-defined values and CPU-defined security state.

Our tweak design is depicted in Figure 1 and comprises hardware-managed integrity counters, segment and address information, privilege levels, page table attributes, as well as software-defined memory colors. All tweak components can be selectively enabled, depending on the specific use case (e.g., unprotected applications, privilege separation only, enclaves).

Integrity Counter. The MEE maintains integrity counters for each memory block, which it increments at each write operation. Integrating the counter into the tweak ensures that the correct memory block is used at any time. This counter prevents replay attacks where an attacker with access to the physical memory reverts a memory block to its former state. Segmentation & Address Information. This part of the tweak holds metadata about the address being accessed and whether it matches software-defined segments that can be configured at each privilege level. The address information can hold an absolute address or an address offset relative to one of the segments. The segment information is represented as a segment bitmap indicating whether an address lies within one or multiple segments.

Privilege Level. This part of the tweak holds the current CPU privilege level (e.g., M-mode, S-mode, U-mode) and ensures that memory is only accessible at a specific level.

Page Table Attributes cover read, write and execute permissions, amongst others. The inclusion of the page table attributes in the tweak ensures that the page mapping cannot be altered without being detected.

Memory Color. This field is extremely versatile and can be configured by software on each privilege level. By choosing appropriate colors, one can segregate memory pages at runtime and also facilitate sharing across security domains.

3.2 Solving the Challenges

Process Isolation with RVAS' cryptographic strength could significantly enhance the security of processes inside encrypted virtual machines (cf. [2]). To solve challenge C_1 , we incorporate two tweak components: First, privilege separation is achieved via the privilege bits in the tweak. The CPU implicitly provides the privilege level. Thus privileged memory is inherently separated via encryption from unprivileged



Figure 1: Overview of the RVAS tweak composition.

software without the need for inspecting page tables. Second, to also isolate different processes, one can include a process identifier in the memory color field, which cryptographically separates them.

For process isolation, the memory color is chosen by the OS. To grant it occasional access to user memory (e.g., for syscall handling), one can tie the privilege level to the so-called RISC-V Supervisor User Memory (SUM) bit, which is comparable to x86 Supervisor Mode Access Prevention (SMAP). That is, the OS can temporarily increase the privilege level to U-mode.

In-process Isolation. To solve the challenge C_2 for segmentation, the tweak's *Segment and Address Information* field can be used. By including segmentation registers from all privilege levels, we can enforce cross-privilege policies. We use a segment-relative address offset in the tweak such that segmentation policies can be portable between different applications, as we will show for cross-enclave shared memory.

To solve the challenge C_3 for memory coloring, our memory color field of the tweak facilitates a huge number of colors (e.g., 2^{80} as opposed to 16 for Intel MPK). Thus, RVAS makes *trusted metadata storages* for memory colors (*i.e.*, tagged memory) obsolete [102]. Having so many unique colors available even gives brute-force resistance when used as a shared secret, as we will demonstrate. Furthermore, RVAS can choose between memory colors from all privilege levels. **Enclaves** are the most involved isolation mechanism addressed in this paper, touching upon the challenges C_2 – C_6 . In the following, we sketch how RVAS solves the challenges C_4 and C_5 . A more detailed explanation will be given in Section 4 and Section 5, followed by a security evaluation in Section 6.

Current enclave systems like Intel SGX [64] use trusted metadata stores, *i.e.*, the Enclave Page Cache Map (EPCM), for shadowing page table entries for each enclave page, along with an enclave identifier. During an access, the EPCM is checked to verify that the page mapping has not been manipulated, thus ensuring the attribute invariant \mathcal{LA} and the spatial invariant \mathcal{LS} . However, the EPCM has a few drawbacks: (1) It increases the Trusted Computing Base (TCB). (2) It takes up memory. (3) The enclave's TLB entries must be flushed during context switches [21, 43]. (4) It permits only a single owner enclave for each page, precluding flexible enclave memory sharing by design.

To overcome these limitations and solve challenge C_4 , we leverage RVAS and make the EPCM obsolete: First, we use the page table attribute field in the tweak to uphold \mathcal{IA} . Second, the address and segmentation information field links between the virtual offset of the enclave and its physical page. Moreover, we use the memory color field to label enclave

pages with a unique enclave identifier. This identifier ensures our spatial invariant \mathcal{IS} , since pages can only be mapped correctly to their legitimate enclave. Note that for the relevant parts of the tweak we use M-mode privileges such that only a trusted software entity can initialize enclave pages in this particular way. Since the temporal invariant \mathcal{IT} involves dynamic memory management, we will discuss it later.

To overcome the protected sharing challenge \mathcal{C}_5 , the mem-

ory color field of the tweak (C_3) can be combined with an enclave-defined segment (C_2). The segment specifies the shared memory. The relative addressing of segments allows the enclave to choose the exact location of shared memory. The memory color essentially comprises a shared secret established between two or more enclaves. Only if the memory color is exactly the same, the enclaves will have the same encryption tweak and, thus, can access the shared memory. Memory Encryption guarantees protection against active and passive physical attacks, thus solving challenge \mathcal{C}_6 . For RVAS, a MEE needs to fulfill three basic properties: (1) confidentiality, authenticity, and integrity of the data, (2) offer replay protection, (3) the used cryptographic primitive must be tweakable with tweak_len bits. Integrity is typically ensured by storing authentication codes in a tree structure. The replay protection from (2) is usually done with some data structure incorporating authenticated counters. The counters are typically fed into the encryption scheme as a tweak or nonce [21, 30, 85, 92, 94]. To fulfill (3), we require a tweakable block cipher or authenticated encryption scheme with sufficiently large tweak size or associated data, such as [4, 27, 96–98]. SGX's underlying MEE is more explicit about the used cryptographic primitives and would require changes to fulfill the third property.

4 SERVAS

This section introduces our SERVAS enclave architecture to highlight the most complex use case of RVAS. We first give an overview of the design, then describe the threat model, and finally, explain how we enable secure enclaves on top of the authenticryption shield.

4.1 Overview

SERVAS is an innovative and highly flexible isolation mechanism for securely executing enclaves. As shown in Figure 2, SERVAS consists of the RISC-V Authenticryption Shield (RVAS) and a software Security Monitor (SM) that manages the whole enclave's lifecycle.

Our SERVAS system follows SGX's design choices to keep a minimal TCB while simultaneously avoiding the drawbacks of large trusted metadata storages (*i.e.*, the EPCM). Instead, we feed the relevant security metadata into the RVAS tweak. By carefully controlling the encryption tweak, SERVAS maintains cryptographic segregation of various security domains.

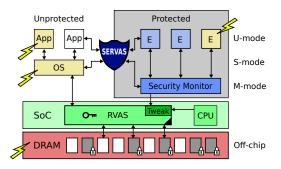


Figure 2: Overview of SERVAS: Thunderbolts show the physical and software attack surface. *App.* denotes unprotected user-mode applications and *E* denotes enclaves. RVAS encrypts and authenticates pages in the untrusted DRAM. Pages with a lock symbol belong to enclaves.

Additionally, SERVAS also enables dynamic enclave memory and natively supports secure sharing of enclave memory, avoiding costly software-based encryption [3].

In our design, the Security Monitor (SM) is the trusted intermediary that acts as a universal entry and exit point for enclaves. Hence, any interactions between untrusted software components and enclaves are safeguarded by the SM. Moreover, the SM is responsible for loading enclaves, initializing their memory pages, handling syscalls and interrupts, shared memory, and swapping. To perform its tasks, the SM is capable of controlling most parts of the tweak.

In the following, we discuss our threat model and show how RVAS helps us build an enclave architecture.

4.2 Threat Model

SERVAS protects enclaves that consist of security-sensitive code and perform operations on sensitive data. Our threat model is mostly in line with Intel SGX [21, 64] and considers a powerful, privileged software and physical attacker. Software running outside the enclave (*i.e.*, the OS and user applications) is viewed as untrusted and might be subject to compromise. We assume the adversary has full control of the OS and can launch rogue applications and enclaves. Unlike SGX, the adversary can tamper with the memory mapping of enclaves (e.g., page tables) and also exercise unrestricted software access to the physical DRAM.

Our Trusted Computing Base (TCB) comprises both software and hardware components. On the software side, we only trust the enclaves themselves and a small Security Monitor (SM) for enclave management. The enclave developer is responsible for adequately implementing enclaves. Vulnerabilities in the enclave itself cannot be prevented by SER-VAS [11, 58]. Also, malicious enclaves [78] are outside our threat model but could be addressed by orthogonal defenses [89].

The SM is running in RISC-V M-mode and can also be viewed as an integral part of our CPU hardware. For example, Intel SGX implements its enclave management via CPU microcode [21]. We assume that the SM is stored on a trusted on-chip ROM or verified as part of a secure boot process [56].

On the hardware side, the TCB covers our System on Chip (SoC), including the CPU core and RVAS. Anything outside the SoC is untrusted. In particular, the attacker can tamper with the DRAM and mount bus probing or cold-boot attacks [60]. SERVAS effectively removes CPU components involved in the page mapping and address translation from the TCB: unlike SGX, which needs to store trusted metadata in the EPCM [21], SERVAS avoids having an EPCM, thus slightly decreasing the TCB complexity of our SoC.

Denial-of-service attacks are outside of our threat model. It is up to the OS and the applications to invoke an enclave.

Side-channel attacks, whether performed in software or in hardware, are an orthogonal challenge, for which plenty of literature is available that could also be applied to SERVAS. We will discuss side-channel security in Section 6. Fault attacks on the encrypted DRAM [45] are detected by RVAS' authenticated encryption, while fault attacks on the SoC [49,68] are outside our scope.

4.3 Building Enclaves

SERVAS enclaves are built on top of RVAS with the assistance of our Security Monitor (SM). The SM uses the RVAS ISA extension to configure the tweak and enforce our *spatial-* (\mathcal{IS}) , *temporal-* (\mathcal{IT}) , and *attribute invariant* (\mathcal{IA}) , as specified in Section 2.3 over the lifecycle of an enclave.

We ensure that enclaves are separated even across otherwise identically structured processes, as follows: We include address information, to confine enclave execution, such as page mappings, page permissions and virtual address range checks as part of RVAS' segmentation and address information, privilege level and page table attributes fields. We further embed page ownership information as part of the memory color.

In total, we define four different page types for specific usecases in SERVAS: PT_ENCLAVE denotes general-purpose memory for private enclave code and data. It must reside in an enclave-specific virtual memory range. PT_SHCODE enables different instances of the same enclave to deduplicate read- and execute-only pages. Thus, it can reduce the memory overhead significantly. We also define PT_SHDATA, a page type that allows enclaves to set up secure cross-enclave data sharing by providing a shared secret before the access. Finally, the SM exclusively uses PT_MONITOR pages to store information about the loaded enclaves in memory. This page is referenced when switching to an enclave to load the enclave's state or save its register content if interrupted (e.g., by a timer interrupt). In the following, we present how the page types link to different types of memory.

Secure Static Page Mapping. To keep \mathcal{IS} and assure a secure virtual-to-physical page mapping of any enclave-related page, we initialize the page with mapping information in the tweak. Moreover, segment and address information, and page table attributes assure that the mapping is only valid for a specific virtual address and well-specified access permissions.

For private enclave memory, we use a unique Runtime Identifier (RTID) of the enclave as the tweak's memory color to bind the page to its enclave. This single ownership principle helps to distinguish enclave instances and satisfies the *temporal invariant* \mathcal{IT} . PT_MONITOR memory solely belongs to the SM, which we enforce by including the privilege mode in the tweak.

To share enclave code or read-only enclave data and to help reduce memory load and TLB pressure, developers can mark pages as PT_SHCODE. In this case, a so-called Enclave Identifier (EncID) substitutes the RTID. The EncID uniquely identifies an enclave codebase or binary via a cryptographic authentication code. Since multiple owners exist, PT_SHCODE pages need to be read-only to enforce \mathcal{IT} .

Secure Dynamic Page Mapping. SERVAS enclaves may use dynamic memory, which has been allocated by the host user-mode application. To do so, the enclaves ask the SM to cryptographically initialize the memory as before.

While static enclave mappings are secured by the SM, dynamic mappings that change at enclave runtime demand special care. To prevent double mapping attacks and enforce the security invariant \mathcal{IT} , we first require the enclave (runtime) to keep track of all of its valid page mappings in a private bitmap (similar to SGX [63]). Thus, when the enclave receives new memory from the host, it can consult its private bitmap and refuse this memory if it is already in use. Second, if an enclave releases dynamic memory, it explicitly invokes the SM, which invalidates the page by destroying its integrity. This invocation prevents use-after-free scenarios and upholds \mathcal{IT} . Note that the private bitmap only needs to enumerate pages *inside* the enclave's address range.

Enclave Data Sharing. SERVAS introduces a novel concept of enclave data sharing. PT_SHDATA memory is writable and can be used for data exchange at native speed (*i.e.*, without copying or re-encryption [3]). As with dynamic memory, the SM performs the setup of shared data pages for enclaves and requires that the respective enclaves acknowledge any mapped page. PT_SHDATA memory is identified by a shared secret that is directly managed by the enclaves. The SM can further assist in establishing a shared secret between the two enclaves by acting as a trusted entity attesting the respective enclaves to each other.

Upholding our security invariants for data sharing is critical and highlights the versatility of our RVAS design. Enclaves can enforce \mathcal{IS} by simply keeping the shared secret confidential, that is, by securely generating and distributing shared secrets with the help of SM. Data sharing also seamlessly scales to multiple enclaves. A user-mode range register points to the

desired shared virtual memory range to uphold \mathcal{IT} , by preventing double mapping attacks (e.g., aliasing PT_SHDATA with existing PT_ENCLAVE pages)

Enclave Life Cycle. The Security Monitor (SM) is responsible for the whole enclave life cycle and is loaded as part of a secure boot procedure. This procedure is part of the ongoing work of the RISC-V groups [56]. In line with other enclave designs [57], our SM provides an API for managing all aspects of an enclave's lifetime: loading, entering, exiting, interruption, managing, and initializing memory for the enclave's code, stack, dynamic memory, shared memory and swapping. Furthermore, it provides functionality for local attestation and sealing. To perform operations involving the enclave's virtual memory, the SM can override most parts of the tweak that is passed to RVAS. Thus, the SM can initialize enclave memory as if the enclave itself did it. For the detailed API description, we defer to Appendix A.

Enclaves can be distributed as encrypted binaries to prevent the host application from accessing the enclave's code or data. A user-mode application can choose to load and run an enclave within its own virtual address space. Enclave binaries are then decrypted (if necessary) and authenticated within the SM, where their code and data are initialized with the page type PT_ENCLAVE or PT_SHCODE. A loaded enclave can be entered at its single developer-specified entry point.

For encrypted enclaves and use-cases that require deployment on specific systems, an AEAD encryption scheme (e.g., ASCON [27]) with a developer key derived from a per-CPU key can be used. Encryption eliminates the need for code obfuscation [61] to prevent theft of intellectual property. Additionally, secrets can be directly embedded in the enclave code. The decryption happens in software within the SM. Loading an enclave also authenticates it and generates a load-time hash forming the EncID, achieving load-time attestation. To store enclave secrets, the SM provides a sealing functionality.

Swapping is essential to handle out-of-memory situations. Enclave systems like Intel SGX can only use a limited physical memory. In contrast, SERVAS allows using all of the available memory for enclaves, making out-of-memory situations happen less frequently. Nevertheless, for real-world workloads, a swapping mechanism is key. Swapping of enclave pages requires interaction between the OS and the SM. To ensure the SM's correct operation and maintain our security invariants, we exclude PT_MONITOR and PT_SHDATA pages from being swapped. When the OS selects an enclave page to be swapped out, it provides a temporary page to the SM to safely move the page to. The SM will then re-encrypt the page-to-swap to this temporary page by using an AEAD encryption scheme.

Afterward, to uphold \mathcal{IT} , the SM invalidates the original physical enclave page. The involved metadata (*i.e.*, AEAD-tag, used nonce, virtual address, range information, and page permissions) are saved on a per-enclave PT_MONITOR page. This metadata ensures that only the one specific version of

the page can later be swapped in and prevents any roll-back attacks. The OS can then write the temporary page safely to the disk and repurpose it for other applications.

5 SERVAS Implementation Details

In this section, we detail the implementation and parameterizations of our prototype implementation of SERVAS. An overview of how SERVAS uses RVAS for this matter can be seen in Figure 3a. First, we highlight the required ISA extensions and then show how the tweak for RVAS is assembled. Second, we detail the new page types introduced by SERVAS and describe the security monitor managing the enclaves. Finally, we explain how a tweak cache can reduce the hardware footprint of SERVAS.

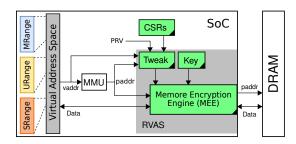
5.1 Instruction Set Extension Details

Realizing SERVAS only requires minimal changes. First, we extend the existing RISC-V ISA with additional Control and Status Registers (CSRs) to set the tweak of RVAS in software. Second, we add a so-called authentication exception, which is raised by the RVAS whenever the decryption fails with an integrity check error during a read, write, or fetch operation. Handling this exception in our SM is a key ingredient for the security of SERVAS.

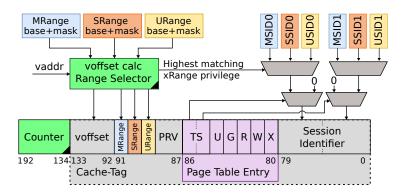
The additional Control and Status Register (CSR) for the machine- (M), supervisor- (S), and user- (U) mode that we refer to as MRange, SRange, and URange, can be seen in Figure 3b. The ranges consist of a base address and a size and specify regions in the virtual address space, which allows us to differentiate between memory accesses. Any access to an xRange must pass RVAS. The MRange is used by the SM to declare the memory of the enclave. The SRange and URange give enclaves control over additional encrypted ranges for enclave-specific needs like shared memory.

To include software-controllable Session Identifiers (SIDs) in the tweak, we add two CSRs for each privilege mode, namely xSID0 and xSID1. To decide which of the two SID registers is used for the tweak, we repurpose two additional selector bits in the currently unused most significant bits part of the PTEs as tweak-select (TS).

Tweak Override. Moreover, we define special load- and store-tweak registers, which are only accessible in machine mode to our SM. These registers can be used to override any tweak parameters used by RVAS and also disable them, except for the RVAS-managed integrity counters. This "tweak override" allows the SM to cryptographically initialize a page in lieu of the enclave without trusting the OS-supplied page mapping. Any further accesses by the lesser-privileged modes must adhere to the same tweak used for initialization, which is cryptographically enforced by RVAS.



(a) Blocks with black corners show components that are part of RVAS.



(b) Composition of the RVAS tweak fed into the MEE. The counter is part of RVAS's replay protection. TS denotes our tweak-select bits stored in the page table entry (PTE).

Figure 3: Overview of RVAS and the tweak construction for the MEE. PRV denotes the current privilege mode.

Lastly, we assume an additional per-CPU key for encrypted loading of enclave binaries, which is fused into the chip and only accessible to our SM via CSRs.

5.2 Tweak

RVAS uses the tweak to incorporate additional information about the CPU state into its MEE, allowing us to achieve a strong software-defined cryptographic separation between enclaves. As shown in Figure 3b, the tweak incorporates integrity counters, page mapping information, privilege information, range checks, and software-controllable session identifiers. For SERVAS, we propose to use RVAS with a tweak size of 192 bits in total. It is structured as follows:

Counter. Similar to SGX's 56-bit counters, we reserve 58 bits of the tweak for the *integrity counter* to guarantee freshness and protect against replay attacks [21,75,85]. The counters are managed inside RVAS and not exposed to software.

xRange. We use 3 bits to encode whether the accessed address is within URange, SRange, or MRange, respectively. These bits constitute the bitmap in the *segment and address information* field of the RVAS tweak design. The range boundaries can be set from their respective privilege levels via the xRange registers. If an address matches an xRange register, its tweak bit is set to one. This matching enforces a strong domain separation between the specified memory ranges. The rightmost xRange bit set to one determines the voffset calculation and the choice of the xSID registers (e.g., URange has precedence).

voffset is the virtual address offset and complements xRange as part of RVAS' *segment and address information* field. The voffset is computed from the base address of the rightmost matching xRange register at cache line granularity. For 48-bit virtual addresses [88] and 64 B cache lines [21], the bit field is $48 - log_2(64) = 42$ bits.

PRV encodes the current privilege mode of the CPU in two bits. Having these bits in the tweak gives us a strong privilege

separation. This field corresponds to the *privilege level* field in the RVAS tweak design.

PTE. Since the untrusted OS manages the page mapping, we include seven bits from the PTE in the tweak. These PTE bits includes the U bit, deciding whether a page is accessible in user mode, the G bit, defining if it is a global mapping, and the three RWX bits, stating the read, write and execute privileges of the page. We also include two of the software-defined reserved tweak select TS bits in the tweak for selecting which of the SID registers are used. The PTE maps to the *page table attributes* field of the RVAS tweak design.

SID. We allocate 80 bit for the Session Identifier (SID), which corresponds to the *memory color* field in the RVAS tweak design. The rightmost matching xSID register determines whether MSID, SSID, or USID is used. TS determines whether one or both xSID0 and xSID1 registers are used. If both are used (*i.e.*, TS = 11b), the resulting SID is truncated to 80 bit.

5.3 Page types

SERVAS defines various page types, which use a specific combination of the tweak components, as seen in Table 1.

PT_NORMAL marks any untrusted page. This page type is located outside of any of the xRange regions and is accessible from any privilege level with the page permission configured in the PTE. While RVAS can also encrypt PT_NORMAL memory, one could bypass encryption to achieve native performance for non-enclave applications.

PT_ENCLAVE denotes pages in the MRange and is intended to be used with a single enclave instance from user mode. The pages can have any combination of page permissions, as specified by the PTE. The TS bits specify the use of the MSID0 register that holds the unique, SM-defined, RTID value for the enclave instance.

PT_SHCODE can be used to share non-writable pages between different instances of the same enclave. This shar-

ing allows to reduce memory requirements and TLB pressure significantly. This page type adheres to the MRange and uses the MSID1 CSR, which holds a unique Enclave Identifier (EncID) for the loaded binary.

PT_SHDATA can be used to safely share data between instances of enclaves, also between different enclaves. Such pages can only reside in the URange, which the SM assures at initialization time. For memory inside the URange, RVAS feeds the virtual address *offset* relative to the URange base into the tweak. This relative offset ensures cross-address-space accessibility of the shared memory. To counteract runtime attacks, PT_SHDATA pages can never be executable.

The TS bits from the page table indicate that both USID registers are used for the SID. Enclaves load the shared secret to the USID0 and USID1 registers before accessing the shared memory region. With the help of the SM, two or more enclaves can agree on an 80-bit shared secret, which separates different shared-memory regions from each other. By specifying URange appropriately, an enclave can constrain shared memory to a particular region and, thus, prevent accidental double mapping attacks.

PT_MONITOR denotes pages used by the SM to store metadata for each enclave and thread. PT_MONITOR must only be accessible by the SM, *i.e.*, in the M mode.

5.4 Security Monitor (SM)

The SM manages enclaves and their transitions between the different privilege modes. It runs with machine-mode privileges, stores its tiny code base and the stack on-chip, and is loaded as part of a secure boot process. Both areas are protected using a Physical Memory Protection (PMP) such that only the SM can access it.

Stateless SM. In principle, the SM can run completely stateless and only requires a small (approx. 1KiB) stack during operation. No static state needs to be kept between SM invocations since all enclave management data is stored inside dynamically allocated PT_MONITOR pages managed by the operating system. The SM also allocates a unique RTID to each enclave instance. Our prototype currently stores the previously allocated 64-bit RTID in memory and increments it for each new enclave to guarantee uniqueness. To remove this tiny 64-bit state, one could simply sample the RTID from one of

Table 1: Tweak decision table: • denotes an arbitrary value, ugrwx and TS correspond to the respective PTE bits, and PRV holds the current privilege level.

MRange	SRange	URange	PRV	PTE	TS	SID	Label
0	0	0	•	•	•	•	PT_NORMAL
1	0	0	U	•	01	MSID0	PT_ENCLAVE
1	0	0	U	!W	10	MSID1	PT_SHCODE
0	0	1	U	!X	11	USID0+1	PT_SHDATA
•	•	•	M	rw	•	0	PT_MONITOR

the RISC-V hardware performance counters, e.g., the elapsed CPU cycles mcycle or other CPU events mhpmcounter. The SM only needs to ensure that they are monotonically counting CPU-global events that assuredly occur between two enclave creations (e.g., memory accesses). For a worst-case estimate, we use mcycle incrementing at 5GHz speed. Thus, it will overflow the 64-bit range only after 117 years of continuous operation. After the device reboots, no enclave is running, and we can sample the RTID freshly.

Enclave metadata is stored in OS-managed but RVAS-protected per-enclave and per-thread PT_MONITOR pages. In order to access PT_MONITOR pages, the SM leverages the tweak override feature to ensure its exclusive access.

Other pages are similarly initialized by the SM using the tweak override to force their page type (e.g., PTE bits, privilege mode, and other tweak-associated CSRs such as xRange and $xSID\{0,1\}$).

API The SM provides an API that works like syscalls but trap into the SM instead. The API allows to manage the lifecycle of the enclave or interact with the SM, *i.e.*, creating, entering, exiting, page preparation, page destroying, in-place re-encryption, and acquiring a sealing key. A detailed description of the API can found in Appendix A.

SM Prototype. Our prototype implements all of the above API functionality. In total, our SM has a very small code size of 1232 Lines of Code (LoC). Of this, 381 LoC are taken up by the ASCON implementation, which is used for loading encrypted enclaves, and deriving the sealing key.

5.5 Caching

For SERVAS, we extend the cache to store the tweaks next to each cache line, referred to as the inline variant. This extension allows us to compare the tweak stored in the cache line to the tweak for the access and ensures that the entire tweak can be reconstructed for any write-back operations. Our tweak design described in Section 5.2 consists of 192 bit. However, as the MEE of RVAS manages the 58 bit integrity counter, we only need to store the remaining b_{SERVAS} 134 bit tweak in our extended cache. These remaining bits b consist of b_{xrange} bit for URange, SRange, and MRange, b_{pte} bits from the PTE, b_{prv} bits from the privilege level, b_{sid} bits for the SID and $b_{voffset}$ bits for the voffset. Each of the N_{cache} cache lines in the data- and instruction cache are augmented with the tweak. Note, that N_{cache} might vary between the two caches. Therefore, the required storage S_{Total} can be calculated as the sum of additionally stored bits in the data- (S_{Data}) and instruction cache (S_{Instr}) .

$$b_{SERVAS} = b_{voffset} + b_{xrange} + b_{prv} + b_{pte} + b_{sid}$$
 (1)

$$S_{Data} = S_{Instr} = b_{SERVAS} \cdot N_{cache} \tag{2}$$

$$S_{Total} = S_{Data} + S_{Instr} \tag{3}$$

Cache Optimization. For many real-world scenarios, we

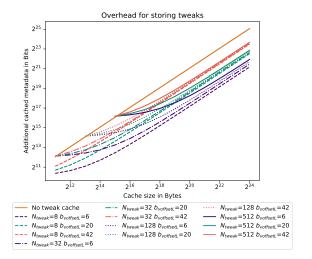


Figure 4: Overhead of the tweak cache in bits compared to the inline variant for a different number of tweak cache entries N_{tweak} . $b_{voffsetL}$ denotes whether 6, 20 or 42 bits of the voffset are stored in the main cache. The cache line size is 512 bit.

only have a limited number of different tweaks, which could be deduplicated in a separate Tweak Cache (TC) [46]. This deduplication would help to significantly shrink the tag size in the caches and, thus, the area overhead. For simplicity, we refer to the data and instruction caches as the *main caches*. For our design, such a TC could be implemented using an index-based indirection in the main cache and a separate TC, whereas the index is stored along the cache line to link the cache and TC. Appropriately sizing a cache is generally tightly coupled to the system's expected workload. In the case of the TC, it also depends on the expected number of enclaves running in parallel. Therefore, a precise parameterization of such a cache exceeds the scope of this paper. However, in the following, we want to discuss the parameters that can be used to tune the cache and their effects.

First, insertion into the TC can be handled by using a non-linear function like a lightweight cryptographic hashor permutation-based function to derive the set index from the tweak pseudorandomly, similar to [79, 91]. This index generation makes finding the correct index for already present tweaks in the TC efficient. Moreover, since the TC index can be computed in parallel to the main cache lookup, the latency can be mostly hidden by choosing a primitive matching the cache latency. Therefore, only one additional cycle for the tweak comparison may be required. For tweak replacements in the TC, all associated cache lines, *i.e.*, all cache lines with that specific index, need to be flushed. Each time a new tweak is inserted into the cache, there is a probability that another cache line is evicted. To reduce the probability of two or more tweaks taking turns in evicting each other, the cache can be:

(1) made larger or (2) be split into multiple ways [41]. A more detailed analysis and simulation can be found in Appendix B.

Next, we define a range in virtual memory that uses the same tweak (except for $b_{voffsetL}$ bits of the voffset) as a tweak zone that each enclave has a number of. In general, the main cache stores more cache lines than the TC stores tweaks. Hence, if the expected size of tweak zones is relatively small, additional $b_{voffsetH}$ bits of the upper voffset can be stored more cheaply in the TC, than the main caches.

Moreover, to size the TC to improve upon the inline variant, we must take two main constraints into account: (1) additional ways in the TC require additional parallel comparator logic and (2) the stored bits in the TC and the additional bits in the main cache must be smaller than the inline variant. For the inline variant, the tweak is compared in parallel to the cache tag. Hence, to handle (1) there should be fewer ways in the TC than in the main cache to reduce the overhead of comparators. Addressing (2) is more difficult since it relies on assumptions on the size of tweak zones, the size of the main caches and the TC's desired size. We need to reconstruct the tweak b_{SERVAS} from Equation (1), but the voffset can be split into an upper $b_{voffsetH}$ and a lower part $b_{voffsetL}$, with the latter being stored along the cache line in the main cache. Additionally, $b_{tweakidx}$ bits are required in the main cache to link the correct entry in the TC, the width of which depends on the number of entries N_{tweak} in the TC. The remaining bits stem from the N_{tweak} entries in the TC times the rest of the tweak and a valid bit b_{valid} . The overhead in each cache can then be aggregated into $S_{TotalOpt}$:

$$b_{voffset} = b_{voffsetH} + b_{voffsetL} = \text{const.}$$
 (4)

$$b_{tweakidx} = \log_2(N_{tweak}) \tag{5}$$

$$S_{DataOpt} = S_{InstrOpt} = (b_{voffsetL} + b_{tweakidx}) \cdot N_{cache}$$
 (6)

$$S_{tweak cache} = (b_{valid} + b_{SERVAS} - b_{voffsetL}) \cdot N_{tweak}$$
 (7)

$$S_{TotalOpt} = S_{DataOpt} + S_{InstrOpt} + S_{tweak}$$
 (8)

We evaluate the number of additional bits required as a function of the main cache size and 512 bit cache lines in Figure 4. The graph shows the number of additional cached tweak bits for the inline variant as the top line. The other lines represent TC configurations that differ in the number of tweak entries N_{tweak} and the split between $b_{voffsetL}$ and $b_{voffsetH}$. One can observe that the break-even point for each N_{tweak} is when the TC has as many tweaks as the main cache has cache lines. After that, the fewer bits are stored in the increasingly large main cache, *i.e.*, the smaller the $b_{voffsetL}$, the smaller this overhead becomes. Additionally, with larger caches the $b_{voffsetL}$ quickly becomes the dominating factor and clusters them into groups. For the same reason $b_{tweakidx}$ also contributes to this, but due to its smaller size, the effect is less pronounced.

5.6 Encryption Bypass Optimization

Our prototype implementation encrypts the whole system's physical memory. However, in the future we intent to make it configurable, such that the MEE only encrypts pages that require this protection, e.g., enclaves. Hence, SERVAS can also be used as an extension for enclaves only. This variant can be achieved with some logic in RVAS that uses information from the xRange registers to decide if a request has to go through the MEE or access the memory directly. Some MEEs like MEMSEC read and verify the integrity of data before new data is written to a location. In a bypass implementation, this verification would cause issues when initialization enclave pages since the MEE attempts to verify the integrity of unprotected memory locations. However, when initializing encrypted pages, the SM is already able to override any supplied tweak information. One would need to simply extend this initialization mechanism by intermittently ignoring any integrity violations.

A limitation of the performance bypass is that the inherent overhead of the integrity protection trees introduced by the MEE persists. While sparse integrity trees could address this problem, no open-source memory encryption schemes with sparse integrity trees have been proposed to the best of our knowledge.

6 Security Analysis

In this section, we analyze the security of SERVAS and its interaction with RVAS. RVAS cryptographically enforces the tweak (cf. Section 2) and solves the challenges of memory isolation \mathcal{C}_1 - \mathcal{C}_6 . Moreover, only the trusted SM can override the tweak, effectively preventing forgery, thus, enforcing the domain separation. However, attacks might aim at breaking the *spatial*- (\mathcal{IS}) and *temporal invariant* (\mathcal{IT}) . In the following, we discuss how SERVAS upholds these variants in a number of attack scenarios.

6.1 Side-channel Attacks and Defenses

Our threat model explicitly excludes side-channel attacks to adopt Intel SGX's threat model. Additionally, we see microarchitectural attacks as specific to the underlying hardware implementation of the CPU which needs to be fixed for enclave and non-enclave code alike, hence, is out of scope of this paper. However, in the following, we want to briefly discuss several attacks a system equipped with SERVAS might encounter.

Physical Attacks such as differential power analysis [52] could break RVAS. RVAS can use more expensive memory encryption schemes such as MEAS [85] to protect from physical attacks on the memory encryption.

Enclave Shared Memory opens a harmless side-channel, allowing Flush+Reload attacks on the shared memory. For

data sharing, enclaves need to trust each other anyways and can access the shared memory directly rather than via a sidechannel. For code pages, we ensure that only instances of the same enclave can optionally deduplicate code.

Controlled-channel Attacks [99] extract side-channel information from an application's inability to access certain memory locations, e.g., by leveraging the OS's ability to keep control over page tables, thus, unmapping pages to trace accesses. Attacks have been shown on Intel SGX Enclaves (SGXStep [16], CopyCat [67]). For SERVAS, these types of attacks also apply. However, provably secure interruptibility [17] and constant-time code can be used as a mitigation technique

Cache Attacks Modern CPUs involve many microarchitectural buffers, all of which could present a side-channel. To close them in software, one can flush core-local buffers when entering or leaving the enclave [93] or use constant-time code. For securing cross-core buffers such as last-level caches, many partitioning schemes [26, 42] and randomization-based approaches [74, 76, 84, 91] exist to provide protection on a hardware level.

Transient Execution Attacks [18, 51] present a threat for many modern high-performance CPUs in both enclave and non-enclave execution mode. To combat this threat, we can use techniques and additional instruction as proposed by MI6 [14]. Furthermore, Wistoff et al. [93] have shown how transient execution attacks on the CVA6 RISC-V CPU can be prevented with the addition of a single instruction.

6.2 Attacks on Physical Memory

Both the OS and a physical attacker can attempt to access enclave data stored in physical memory. While a physical attacker could read out enclave memory via bus probing attacks or cold-boot attacks [60], the OS has direct access to physical memory. However, the OS cannot provide all the necessary tweak information. Hence, the attack is mitigated by RVAS detecting the integrity corruption.

Finally, an attacker could install a tampered DRAM module that duplicates the memory on each address and allows to toggle between the two. This results in a violation of the invariant \mathcal{IT} , and allows for roll-back attacks. Similarly, the OS could move around encrypted enclave data and their authentication codes in order to replay stale data. However, the integrity counters of RVAS protect against roll-back attacks.

6.3 Attacks on Virtual Memory

Memory Isolation. Enclaves run in the virtual memory of a host application. Thus, the host application or the OS could try to access enclave data via its virtual address space. SERVAS mitigates these attacks by supplying the memory color field of RVAS with data that is either unforgeable by the OS (e.g.,

MRange, MSID) or secret, *i.e.*, only known by the enclave. Without a correct tweak, RVAS fails and traps to the SM.

Page Mapping Attacks. The OS has full control over the page table entries (PTEs) and can arbitrarily map pages and page permissions. Noted as the memory mapping challenge C_4 (cf. Section 2), this allows for a range of attacks.

Downgrade Attack. A compromised OS can map an unprotected page to an address in the MRange of an enclave and trick it into writing secrets to this unprotected rogue page. However, when entering the enclave, the SM sets its respective MRange registers. This register changes the address and segment information supplied to RVAS. Additionally, the rogue page has not been initialized by the SM. Thus, the integrity of the page is violated, and the decryption fails.

Page Remapping Attacks. The OS can attempt to violate invariants \mathcal{IS} and \mathcal{IT} in various ways. It could remap enclave pages to a different enclave or change the mapping order within an enclave's range. This remapping allows to manipulate the control flow or divert the data access to different parts of the enclave, *i.e.*, to set an encryption key to zero. Further, since the PTEs also hold the page's permission bits, the OS could make a data page executable and, for example, exploit a vulnerability in the enclave itself to divert the control flow.

To counteract these attacks, the RVAS tweak includes all relevant mapping information, including a session identifier (e.g., the Runtime Identifier (RTID) or the Enclave Identifier (EncID)), the virtual page offset within an enclave as well as the page permission bits specified by the enclave developer. Thus, any deviation from the intended memory mapping results in a decryption error and denies the access.

Swapping Attacks. The OS can attempt to swap out enclave pages while maintaining the original page intact. Without the updated PTE, the MMU will not raise a page-fault during access by the enclave. Thus, the OS would have two copies of the same virtual enclave page, which clearly violates our *temporal invariant* \mathcal{IT} . SERVAS prevents this as follows: the SM overwrites and, thus, invalidates the original page before the swapped-out copy is released to the OS.

The OS could try to misuse the swapping mechanism to violate \mathcal{IT} . When the attacker requests a page to be swapped, the SM invalidates the physical page and hands over an encrypted copy to the OS. Now, the OS swaps the page in but keeps the old copy of the swapped page on disk. The attacker then requests to swap out the same page again. Upon the next swap-in operation, the OS replays the first copy to perform a roll-back attack. To counteract this attack, the swapped pages are protected with an AEAD scheme. The authentication tag is linked to the page's virtual address and securely stored on a per-enclave PT_MONITOR page. To enforce \mathcal{IT} , the tag is checked during swap-in, preventing any replays.

Shared Data Page Attacks. Enclave shared memory opens a new attack vector, where the OS could replace an arbitrary enclave page with a shared memory page (using the zero key), thus tricking the enclave into leaking its secrets. We close this

attack as follows: Accessing shared memory is only possible within the URANGE register, which is initially disabled. Thus, the enclave has to explicitly configure the URANGE register (after configuring the shared memory key).

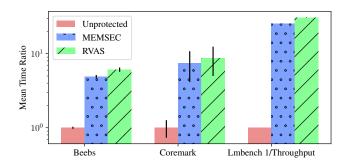
The security of shared memory further depends on the 80 bit shared key stored in the USID{0,1} CSRs. A malicious OS could start a malicious enclave and map the pages of an existing shared memory range to its virtual memory. This enclave then sets its range registers and brute-forces the shared key as part of an online attack. Note that this attack can only target shared memory, as the xRange separates other enclave page types.

Our SM can prevent brute-force attacks: (1) The SM can terminate the enclave that used the wrong shared key after one or a few access attempts. As spawning a new attacker enclave takes time, this acts as dynamic rate-limiting. (2) The SM can perform explicit rate-limiting in its exception handler, thus further reducing the speed of the brute-force attack.

Shared Code Page Attack. SERVAS allows different instances of the same enclave to share non-writable pages to deduplicate code and minimize memory usage. This deduplication is achieved using the Enclave Identifier (EncID) in the tweak as a memory color. An attacker might try to generate an enclave which yields the same EncID as the victim enclave. This challenge refers to finding a second pre-image to a cryptographic authentication code. In a first attack scenario, the attacker could generate a large number of enclaves in an offline brute-force search until the EncID collides with the victim enclave. Full cryptographic strength (e.g., 128 bit security) for the EncID, prevents this attack. However, SERVAS only supports a 80 bit SID inside the tweak, which requires truncating the full EncID. A simple truncation would drastically facilitate this offline attack. To counteract this, our SM performs a key derivation on the EncID that involves the secret CPU key, before truncating it. In a second scenario, the attacker performs an online brute-force attack by mapping the shared code pages of a victim enclave into the attacker's enclave address space at the same virtual offset. If the truncated EncIDs match, the attacker enclave can access the shared code pages. If not, an authentication exception is raised, and the attacker can retry with a new enclave yielding a different EncID. As before, the SM can terminate the attacking enclave and apply a time penalty for each authentication exception.

7 Evaluation

Our prototype is based on the CVA6 [101] platform consisting of a 64-bit RISC-V CPU. For SERVAS, we extended this platform with the RVAS ISA extensions, the storage of tweaks in the cache, and a MEE for RVAS. The ISA extensions of SER-VAS allow the security monitor to set the tweak in software. Here, we endow CVA6 with additional CSRs and a tweak logic, as depicted in Figure 3. We further extend the write-through cache to handle the tweak, *i.e.*, storing these bits next



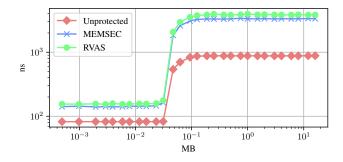
(a) Benchmark results for the CVA6 core using no memory encryption, MEMSEC, or RVAS. Numbers in red are given as ratios to the unprotected configuration.

to the data entries and considering the tweak in the hit logic. We increased the default cache line size from 16 B to 64 B, a common choice for many CPUs. We use MEMSEC [92], an open-source, AXI compatible framework supporting various encryption schemes for the MEE. To fulfill our requirements (cf. Section 3), we configured MEMSEC to use ASCON-128. We use this cryptographic primitive for RVAS because it is the only cipher that is supported by the MEMSEC framework in TEC-Tree mode. Furthermore, we extend MEMSEC to process the tweak as ASCON's associated data. MEMSEC is placed between the cache and the memory controller to transparently encrypt all data leaving the processor. We transport the tweak from the core to MEMSEC using the user-defined signals of the AXI4 communication fabric.

7.1 Performance Overhead

To measure the performance overhead introduced by RVAS, we deployed it on a Xilinx Kintex-7 FPGA KC705 board and ran a variety of macrobenchmarks on a Linux 5.10 kernel. To simulate different workloads, we use BEEBS [71] and CoreMark [29]. For BEEBS, we excluded the crc32, ludcmp. st, matmult-float, and rijndael benchmarks, since they caused lockups on the unmodified CVA6 CPU. For the results in Figure 5a, we aggregated all BEEBS benchmarks into a single metric by using the geometric mean, while the full BEEBS results are given in the Appendix C in Figure 12. For the fastrunning CoreMark, we plot the mean over 1 000 runs, while for the slower BEEBS, we average over 25 runs. For each run, CoreMark uses 10 internal iterations, while for BEEBS, we use 4 internal iterations. Due to the resource-constrained prototype (256 MB accessible DRAM and 50 MHz CPU frequency), we cannot run more heavyweight benchmarks.

Figure 5a depicts the results of our evaluation normalized to an unprotected baseline, *i.e.*, the CVA6 core without any memory encryption. The use of stock MEMSEC configured for an authentication tree constitutes the main overhead for all benchmarks. As we will discuss in Section 7.3, the memory



(a) Memory read-write latency.

Figure 7: Benchmarking and memory latency results on the CVA6 platform in an unprotected, MEMSEC and RVAS configuration.

encryption overhead can be significantly reduced in practice. The overhead of RVAS over MEMSEC is caused by the additional rounds of ASCON we use to process the tweak as part of its associated data. Here, RVAS adds two additional calls to ASCON's permutation function in the MEE. The RVAS prototype adds an overhead between 16.7 % for CoreMark, 20.0 % for LMbench [65] and 24.5 % for BEEBS compared to MEMSEC. Figure 6a shows the results of the read-write latency test of LMbench for different configurations. More concretely, this benchmark measures the read-write latency for different sized data chunks and visualizes the impact of the 32 kB L1 data cache of CVA6 and the latency of the external DDR3 memory. While MEMSEC increases the average readwrite latency for a memory access from 850 ns to 3300 ns, the two additional rounds of RVAS only increase the latency by additional 290 ns on average. These results are encouraging, given that we instantiated our RVAS prototype with the general-purpose MEMSEC encryption framework. An encryption engine that is tailored towards RVAS (e.g., by optimizing block sizes) will further reduce the overhead. We discuss possible optimizations in Section 7.3.

Table 2: Micro-benchmarking results for SERVAS.

	cycles median	relative to getpid
Syscall getpid	10 353	1.0x
SERVAS SM Call "null"	9 029	0.9x
SERVAS Enter	18 866	1.8x
SERVAS Exit	17 393	1.7x
SERVAS Create	438 841	42.4x
Context Switch Sem.	757 301	73.1x

Furthermore, we evaluate SERVAS using the microbenchmarks shown in Table 2 on CVA6 equipped with RVAS. To reduce the scheduling- and cache-related differences in the measurement results, we repeat each test 10 000 times. To get a sense of the switching overhead of SERVAS, we measure the number of cycles an eenter/eexit takes and compare it with a simple "getpid" system call. The "null SM call" is the equivalent of a getpid system call, but instead of calling into the OS, we invoke the SM. Any SM-related action (e.g., eenter/eexit) also includes this baseline overhead for an SM call. Calling an enclave function only takes 3.5x the time of a simple system call. This call includes the time for entering (18866 cycles), executing a simple function within the enclave which only returns a fixed value, as well as exiting (17 393 cycles) the enclave. We implemented a context-switch benchmark using a semaphore and shared memory for synchronization to compare this with traditional process-based isolation. Process-based context switching takes 73.1x of a simple system call. For comparison, entering and exiting an Intel SGX enclave takes 71x the time of a system call [55], thus being twenty times slower than invoking a SERVAS enclave. This result highlights the benefit of SERVAS not requiring an expensive TLB flush [21,43] when invoking an enclave.

7.2 Hardware Overhead

The hardware overhead of RVAS consists of the MEE, the ISA extension, and the cache with the additional tweak bits. We synthesize our modified CVA6 for a Xilinx Kintex-7 series FPGA. Compared to the default CVA6, the design increases by 20.27% in terms of lookup tables (LUTs) and 19.13% in terms of flip-flops. From these 20.27% additional LUTS, 61.84% result from the introduced MEE, 37.26% of the extended cache, and the rest by the ISA extension. RVAS requires that each cache line is tagged with 125 bit for the memory encryption tweak due to CVA6 implementing 39 bit virtual address spaces. While the tag overhead depends on the design of the cache and the size of the cache lines, for our 512-bit cache lines, the overhead is 25%. However, this overhead could be reduced using the optimizations in Section 5.5.

7.3 Prototype Limitations

Our RVAS design, as a prototype implementation, is not optimized for performance. Due to a lack of openly available high-performance MEE that support authentication, we used the MEMSEC [92] framework. As seen in Figure 5a, the MEE is significantly responsible for the overall performance overhead. According to ARM, full memory encryption induces a runtime overhead of 7.5 % to 25 % and a storage overhead of 7.8 % to 26.7 % [75]. Different workloads on Intel SGX may run up to 3–19x slower [66]. Given recent advances in the RISC-V community, we also expect high-performance MEEs to become openly available in the future. Currently, our prototype transparently encrypts the whole external DRAM. An encryption bypass could selectively disable encryption for unprotected data and improve the system performance.

Caches. The CVA6 platform we used for the evaluation features a write-through cache that slows down write operations

on encrypted memory. Adopting a write-back cache could significantly improve write performance. In our current prototype implementation, every cache line is tagged with the full tweak, yielding the area overhead mentioned in Section 7.3. To reduce this storage overhead to a minimum, a dedicated Tweak Cache, as elaborated in Section 5.5, could be installed.

8 Related Work

Intel SGX [21,64] is a set of instructions to manage and interact with enclaves on the x86 platform. While SGX enclaves use the same userspace virtual memory as the accompanying application, the pages, which can be up to 128 MB and are only accessible by the enclave, are located in the Processor Reserved Memory (PRM) region in the memory. The PRM holds the 4 kB pages belonging to the enclave in the Enclave Page Cache, and the Enclave Page Cache Map (EPCM) is a trusted metadata storage storing the state of the EPC. In contrast to SGX, SERVAS is not limited to a statically allocated memory region (i.e., the PRM) but dynamically reuses the whole physical memory for both unprotected code and enclaves. Furthermore, our approach does not require a trusted metadata storage such as the EPCM but instead feeds this metadata directly into the encryption. Finally, SERVAS does not require flushing of the TLB.

CrypTag [69] assures safety for memory allocations by utilizing the unused upper bits of pointers to supply a tag to a memory encryption for specific instruction or data accesses. In contrast, RVAS supports various policies and incorporates information on the CPU state or specified by a SM (cf. Section 3). On the hardware side, RVAS adds all the necessary logic to enforce these policies. The cache area overhead of CrypTag is up to 20 %, which is comparable with RVAS.

VAULT [83] aims to reduce the paging overhead by making the EPC of Intel SGX available to the full system memory. Unlike SERVAS, VAULT does not overcome the limitation of SGX regarding efficient shared memory.

SMARTS [94] implements a Memory Protection Unit (MPU) as a framework that can perform partial memory encryption. The physical DRAM is partitioned into an untrusted, a trusted, and a metadata region. In contrast to SMARTS, SERVAS is not bound to a static boot-time memory configuration and allows fully dynamic management of enclave pages at runtime. AMD Secure Encrypted Virtualization (SEV) [1,2,25,48] is a set of CPU extensions to execute virtual machines in untrusted environments. AMD SEV [1] comprises secure memory encryption (SME) [25], SEV-encrypted state (SEV-ES) [48], and SEV-secure nested paging (SEV-SNP) [2]. Combined, they allow for protection against memory replay, data corruption, memory aliasing, and memory re-mapping attacks. In contrast to AMD-SEV, SERVAS focuses on enclaves rather than virtual machines. Moreover, AMD-SEV does not offer integrity protection against physical attacks.

Intel MKTME [44] is a proposal to transparently encrypt memory pages. Based on the PTE, one out of 64 different encryption keys can be selected. Similar to SEV, MKTME does not provide cryptographic authentication. Unlike SEV, it needs to rely on a trusted hypervisor.

Other systems. Sanctum [22], Keystone [57], CURE [9], and TrustZone [6] are other recent enclave and TEE designs tackling challenges such as cache-based attacks and enclave-to-peripheral binding. However, in contrast to SERVAS, all these designs do not explicitly protect the external memory from physical attacks using memory encryption.

9 Future Work

We see usage scenarios of RVAS beyond traditional enclaves to provide, for example, fine-grained intra-enclave isolation, and system-level enclaves. SERVAS could be used to supersede other protection mechanisms such as memory protection keys [43], pointer authentication [59], pointer tagging [8], and memory coloring [69]. Furthermore, RVAS presents a building block that could be used to enable secure virtualization (cf. AMD-SEV) without the need for different encryption keys and with additional protection against physical attacks. SERVAS specifies a number of configuration registers on each privilege level. These registers can allow for additional protection in the kernel by creating kernel-level enclaves. Our current prototype implementation uses ASCON as it is a lightweight cryptographic primitive already available in MEMSEC. However, realizing RVAS with other encryption primitives, such as AES, would be possible but requires additional analysis, which we leave open for future work.

Protection against malicious enclaves. While outside the threat model of enclaves, the host application can be protected from a potentially malicious enclave [78] using techniques similar to SGXJail [89]. RVAS' memory colors could be leveraged for this purpose.

10 Conclusion

This paper presented an innovative isolation primitive called authenticryption shield that unifies traditional and advanced isolation policies and offers potential for future security applications. We illustrated how it streamlines security reasoning by building on top of a tweakable memory encryption scheme, thus giving cryptographic isolation guarantees. We demonstrated how the versatility of our approach allowed us to design and prototype an innovative and novel enclave architecture for RISC-V called SERVAS, that even also allows for native and secure sharing between enclaves. As a generic extension for the RISC-V ISA and a small Security Monitor, we showed how SERVAS, at a size of just 1232 LoC, can manage all enclaves throughout their life-cycle. Additionally, we thoroughly assessed SERVAS's performance and showed that

entering or exiting takes only about 3.5x of a getpid syscall. We prototyped and evaluated SERVAS on the CVA6 RISC-V hardware and plan to make the prototype publicly available.

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A SM API

The SM provides a number of API functions that allow applications, the OS, or the enclave to interact with the SM. Therefore, we define the following API functions offered by our SM:

ecreate is used for loading and initializing an enclave. It is called with the virtual location of the encrypted enclave code, its virtual target location, a memory area for the enclave stack, and two pages used for storing per-enclave and per-thread metadata. Once invoked, the SM decrypts the enclave and initializes its stack and metadata pages, using the tweak override. A hash of the decrypted enclave is stored in the per-enclave page for later use (e.g., eqetsealkey).

eenter is called by the user-mode application with the perenclave and per-thread pages generated by ecreate. When calling eenter, the SM saves relevant CPU registers on the per-enclave page, initializes the enclave CSRs, and starts the enclave code at its predefined entry-point.

eexit is called by the active enclave to return to the user application. Here, the SM restores the register state from before entering the enclave (apart from return value registers) and resets the enclave's CSRs. Finally, the program counter is set such that the program continues after its last eenter call. **Interruption.** When an enclave is interrupted, the SM stores the enclave register state in its per-thread page, wipes the registers, and hands over execution to the OS. When the interrupted process invokes eenter again, the SM restores the saved enclave state and resumes execution.

eprepare makes the SM initialize and zeroes an enclave page to an enclave-defined page type using the tweak override. It allows for any page type apart from the PT_MONITOR. This allows an enclave to initialize pages dynamically allocated by the user-mode application.

edestroy makes the SM destroy a physical enclave page by choosing an otherwise unused value for the tweak override before writing the entire page.

emod offers in-place re-encryption of a page. Called with the virtual address of the page, the old page type, and the new page type. This call can be used to deliberately change page table permission bits or to rekey a shared PT_SHDATA page. This call has to be made if an mprotect or mmap syscall altered tweak-relevant bits of the PTE. The SM closely follows the procedure from eprepare, but preserves the pages content. **egetsealkey** is used to acquire a deterministic sealing key derived from the enclave hash and the CPU key. This call allows the enclave to safely encrypt its secrets for persistent storage.

B Cache Eviction Probability

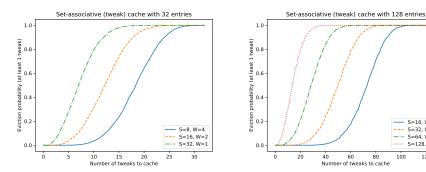
Intuitively, the size of a Tweak Cache (TC) and its number of ways determine its eviction probability. This probability corresponds to the likelihood that, e.g., one enclave experiences

self-eviction. To do so, we simulate the eviction probability with two experiments as follows: First, we simulate the probability that at least one tweak is evicted when accessing a certain number of tweaks in Figure 9. Second, we simulate the total eviction probability, *i.e.*, the probability that a tweak is evicted when accessing a certain number of tweaks in Figure 11. Both experiments are evaluated with random set indices for our TC, which approximates the distribution of the cryptographic index derivation function. We use TCs with capacities of 32 and 128 entries and one to eight ways. We repeat each experiment 10000 times. As seen in Figure 9 and Figure 11, the eviction probability of a tweak entry can be significantly reduced by increasing the number of ways or increasing the number of possible tweak entries.

To put this into perspective, we assume that one enclave uses 6 tweaks, and we can accept a total eviction probability for our system of only 5 %. With parameters in mind, we can run roughly 2 enclaves in parallel on a system with a small TC, *i.e.*, with only 32 entries and 2 ways, with low probability of the enclaves interfering with each other, as seen in Figure 10a. On the larger configuration in Figure 10b with 128 entries and 4 ways, about 11 enclaves could run with the same low eviction probability.

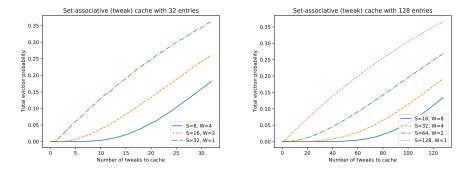
C Detailed Evaluation Results

Figure 12 shows the individual results of the BEEBS benchmark suite when run on RVAS, compared to the MEMSEC encryption engine we used. Both are normalized relative to an unprotected implementation (*i.e.*, without enclaves or memory encryption).



(a) TC with 32 entries. (b) TC with 128 entries. Figure 9: The probability of evicting at least one entry for tweak caches with 32 or 128 entries and 1, 2, 4 or 8 ways.

S=16, W=8
--- S=32, W=4
--- S=64, W=2
--- S=128, W=1



(a) TC with 32 entries. (b) TC with 128 entries. Figure 11: The total eviction probability for tweak caches with 32 or 128 entries and 1, 2, 4 or 8 ways.

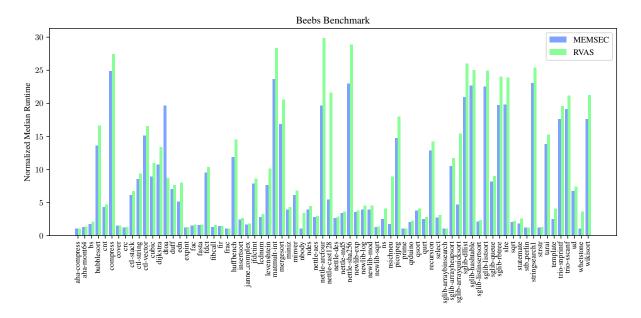


Figure 12: Individual results of the BEEBS benchmark suite, normalized to an unprotected implementation.