# A Fully Fault-Tolerant Representation of Quantum Circuits

Alexandru Paler\*, Ilia Polian\*, Kae Nemoto\*\*, and Simon J. Devitt<sup>+,-,\*\*</sup>

\*University of Passau, Innstr. 43, 94032, Passau, Germany
+Ochanomizu University, 2-1-1 Otsuka, Bunkyo-ku, Tokyo 112-8610, Japan.
-Graduate School of Media and Governance, Keio University, Fujisawa, Kanagawa 252-0882, Japan.

Abstract. We present a quantum circuit representation consisting entirely of qubit initialisations (I), a network of controlled-NOT gates (C) and measurements with respect to different bases (M). The ICM representation is useful for optimisation of quantum circuits that include teleportation, which is required for fault-tolerant, error corrected quantum computation. The non-deterministic nature of teleportation necessitates the conditional introduction of corrective quantum gates and additional ancillae during circuit execution. Therefore, the standard optimisation objectives, gate count and number of wires, are not well-defined for general teleportation-based circuits. The transformation of a circuit into the ICM representation provides a canonical form for an exact fault-tolerant, error corrected circuit needed for optimisation prior to the final implementation in a realistic hardware model.

# 1 Introduction

Quantum computing promises speed-ups for a number of relevant computational problems. Building a scalable and reliable quantum computer is one of the challenges of modern science. As the size of quantum computers increases, the focus of interest shifts from their basic physical principles to structured design methodologies that will allow us to realise large-scale systems.

In general, quantum circuit optimisation methods are used to minimise the implementation costs like the number of gates or the number of wires [WD10]. Classical circuit optimisation assumes fixed gate lists even in the presence of gate errors, but classical circuits are more robust towards errors, whereas quantum information is fragile [NC10, Ch. 8]. Classical gate failures are usually solved either by hardening the circuit (e.g. modifying transistor sizes), or by introducing various types of information redundancies that mitigate the failures. Gate hardening is not considered realistic in quantum computing architectures, and a feasible solution requires quantum error-correcting codes (QECC) [DMN13]. The structure and design of QECC allows encoded quantum gates to be applied directly to the encoded quantum data.

<sup>\*\*</sup>National Institute of Informatics, 2-1-2 Hitotsubashi, Chiyoda-ku, Tokyo, Japan

In contrast to the classical case, the most practical implementations of QECC and fault-tolerant quantum circuits are composed of gates which are non-deterministic even in the absence of errors [FMMC12]. They either work correctly or require a correction, which is only determined during the execution of the circuit. Most such correction gates do not need to be dynamically included into the executing circuit, because their effect can be classically tracked through the subsequent gates [PDNP14]. This is not true for all possible corrections occurring during the execution of a quantum circuit and some need to be actively applied to the quantum data[FMMC12]. This means that the overall circuit is dynamic, because its gate list needs to be modified during its execution based on certain measurement results. Reducing the incidence of such gates is difficult because when a fully error-corrected, fault-tolerant circuit is examined, it is exactly these measurement based corrections that appear to give quantum computing its power [Fow12]. In general, fault-tolerant quantum circuits are constructed from Clifford and T (Section 1.1) gates, and the T gate is the main source of the complications [AMMR13] for which dynamic corrections cannot be avoided.

The separation of circuit gates into Clifford and T gates is generally performed at the higher level circuit design layer in order to make fault-tolerant error constructions more amenable to practical implementation. The physical mapping of these circuits to an actual error corrected architecture is then done with a specific QECC and hardware architecture in mind, preserving fault-tolerance. Faulttolerance is understood as the set of procedures by which the cascade of quantum errors (bit and phase flips) caused by the circuit [DMN13] is restricted allowing the underlying QECC to be effective when mapped to actual operations in a hardware model. In standard fault-tolerant constructions (those that are widely used in state-of-the-art hardware models [DFS+09,YJG+12,NTD+14,JMF+12]), the only dynamic corrections needed are when we implement logical layer corrections for T gates. These correctional gates are constructed using ancillae initialised into high-fidelity states (see Section 1.5) and gate teleportation protocols [FMMC12]. Our results are quite similar to those present in Ref. [DKP07], however this work focuses on producing a representation that is compatible with fault-tolerant error correction protocols.

The solution to having all the required corrections into the logical layer of the computation is to translate circuits into a regular representation that replaces correctional gate dynamics with the dynamics of reading and interpreting the circuit outputs. Such an approach is similar to the model of measurement based quantum computing (MBQC) [BBD $^+$ 09], where a computation is solely described by the interpretation of the measurements performed on a specifically initialised quantum state. A circuit is described in this work as an ICM sequence, where the I part contains qubit initialisations, the C part is a subcircuit consisting entirely of CNOT gates, and the qubits are measured in the M part. This work represents a separate and distinct approach from the work of [MSD14], where NCV (reversible) circuits were mapped into Clifford and T gate circuits, because the ICM representation is regular and consists entirely of ancillae, CNOTs and measurements.

The ICM representation is the extension of the methods presented in [Fow12] to fit into the measurement based paradigm [BBD<sup>+</sup>09]. The presented algorithmic formulation will output the ICM representation for arbitrary quantum and reversible circuits. Such a formulation, although it requires an increased number of ancillae, allows us to directly synthesise fully fault-tolerant error corrected circuits for an underlying higher level circuit (including all required ancillary protocols), represents the realistic resource requirements of fault-tolerant quantum computations for state-of-the-art quantum architectures [DSMN13,Got13] and provides an elegant form for further circuit optimisation techniques for QECC models such as topological codes [PF13,Dev13].

The paper is organised as follows: Section 1.1 offers a short introduction to quantum computing, illustrates the concepts of controlled and rotational gates, discusses the reversibility aspects of computing and the applications of information and gate teleportations. Section 2 details the non-deterministic resource requirements of arbitrary quantum circuits, introduces the ICM representation and presents the algorithm used for achieving it. The algorithm is benchmarked using circuits from the RevLib library and the results are discussed in Section 3. Finally, conclusions and future work are formulated.

# 1.1 Quantum and reversible computing

Quantum circuits represent and manipulate information in qubits (quantum bits). The quantum state of a qubit is the vector  $|\psi\rangle = (\alpha_0, \alpha_1)^T = \alpha_0 |0\rangle + \alpha_1 |1\rangle$ . Here,  $|0\rangle = (1, 0)^T$  and  $|1\rangle = (0, 1)^T$  are quantum analogues of classical logic values 0 and 1, respectively.  $\alpha_0$  and  $\alpha_1$  are complex numbers called amplitudes with  $|\alpha_0|^2 + |\alpha_1|^2 = 1$ .

A state may be modified by applying single-qubit quantum gates. Each quantum gate corresponds to a complex unitary matrix, and gate function is given by multiplying that matrix with the quantum state. The application of X gate to a state results in a bit flip:  $X(\alpha_0, \alpha_1)^T = (\alpha_1, \alpha_0)^T$ . The application of the Z gate results in a phase flip:  $Z(\alpha_0, \alpha_1)^T = (\alpha_0, -\alpha_1)^T$ . The matrices of the Pauli gates I, X, Y, Z are:

$$I = \begin{pmatrix} 1 \ 0 \\ 0 \ 1 \end{pmatrix} Y = \begin{pmatrix} 0 \ -i \\ i \ 0 \end{pmatrix} X = \begin{pmatrix} 0 \ 1 \\ 1 \ 0 \end{pmatrix} Z = \begin{pmatrix} 1 \ 0 \\ 0 \ -1 \end{pmatrix}$$

Further important single-qubit quantum gates in the context of this work are H, P, T, where  $T^2 = P$  and  $P^2 = Z$ .

$$H = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \ P = \begin{pmatrix} 1 & 0 \\ 0 & i \end{pmatrix} \ T = \begin{pmatrix} 1 & 0 \\ 0 \ e^{i\frac{\pi}{4}} \end{pmatrix}$$

Quantum measurement is defined with respect to a basis and yields one of the basis vectors with a probability related to the amplitudes of the quantum state. Of importance in this work are Z- and X-measurements. Z-measurement is defined with respect to basis ( $|0\rangle$ ,  $|1\rangle$ ). Applying a Z-measurement to a qubit in state  $|\psi\rangle = \alpha_0|0\rangle + \alpha_1|1\rangle$  yields  $|0\rangle$  with probability  $|\alpha_0|^2$  and  $|1\rangle$  with probability

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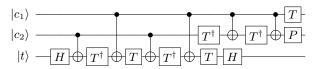


Figure 1: Toffoli gate using CNOT, T,  $T^{\dagger}$  and H gates [NC10, Ch. 4].

 $|\alpha_1|^2$ . Moreover, the state  $|\psi\rangle$  collapses into the measured state (i.e. only the components of  $|\psi\rangle$  consistent with the measurement result remains). X-measurement is defined with respect to the basis  $(|+\rangle, |-\rangle)$ , where  $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$  and  $|-\rangle = \frac{1}{\sqrt{2}}(|0\rangle - |1\rangle)$ .

### 1.2 Rotational gates

The exponentiation of the Pauli matrices results in the rotational gates  $R_x$ ,  $R_y$ ,  $R_z$  parametrised by the angle of the rotation [NC10, Ch. 4]. Hence the bit flip is a rotation by  $\pi$  around the X-axis, implying that  $X = R_x(\pi)$ , and the phase-flip is a rotation by  $\pi$  around the Z-axis, such that  $Z = R_z(\pi)$ . Furthermore,  $P = R_z(\pi/2)$  and  $T = R_z(\pi/4)$ . The V and  $V^{\dagger}$  gates are parametrised X-rotations,  $V = R_x(\pi/2)$ . The Hadamard gate is  $H = R_z(\pi/2)R_x(\pi/2)R_z(\pi/2) = PVP$ .

$$R_x(\theta) = \begin{bmatrix} \cos\frac{\theta}{2} & -i\sin\frac{\theta}{2} \\ -i\sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix} R_y(\theta) = \begin{bmatrix} \cos\frac{\theta}{2} & -\sin\frac{\theta}{2} \\ \sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix}$$
$$R_z(\theta) = \begin{bmatrix} e^{-i\theta/2} & 0 \\ 0 & e^{i\theta/2} \end{bmatrix} CNOT = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$$

#### 1.3 Controlled gates

An n-qubit circuit processes states represented by  $2^n$  amplitudes,  $\alpha_y$ , with  $y \in \{0,1\}^n$  and  $\sum_y |\alpha_y|^2 = 1$ . Measuring all qubits of the circuit results in one basis vector with the probability given by the corresponding amplitude,  $|\alpha_y|^2$ . Quantum gates may act on several qubits simultaneously. A gate operating on n qubits is represented by a  $2^n \times 2^n$  complex unitary matrix. One important two-qubit gate is the  $controlled-not \ CNOT(c,t)$  gate, where the c qubit conditionally flips the state of the t qubit when set to  $|1\rangle$ . In general, any quantum gate can be used in a controlled manner, and other versions are controlled-Z (CPHASE), controlled-V (C-V) and controlled- $V^{\dagger}$  (C- $V^{\dagger}$ ), where  $V^2 = X$ .

Similarly to how arbitrary classical Boolean functions can be constructed entirely from NAND gates, universal quantum computations can be constructed using a discrete set of gates. The universal gate set has to contain at least one coupling operation, and the most often used one is CNOT. A commonly used gate set in fault-tolerant quantum computing is  $UGS_{ft} = \{CNOT, H, T\}$  [NC10,



Figure 2: a) Toffoli gate using CNOT, controlled-V and controlled- $V^{\dagger}$  gates [NC10, Ch. 4]. b) The decomposition of the controlled-V using CNOT, T,  $T^{\dagger}$  and H gates

Ch. 4]. There are gate sets that are not universal, an example is the Clifford gate group, generated by the gates  $\{CNOT, H, P\}$ . Circuits comprised of gates exclusively from the Clifford group can be efficiently simulated on a classical computer [Got98], but the Clifford group together with the T gate is quantum universal. The T gate is one of the most expensive quantum gates to implement when QECC and fault-tolerant computation is taken into account [DSMN13,Got13]. Thus, there is ongoing research into reducing the T gate count of synthesised quantum circuits [Jon12,AMMR13,MSD14].

# 1.4 Reversibility

The linearity of quantum mechanics has the effect that information can not be erased, therefore, for an arbitrary computation, the number of input qubits equals the number of output qubits. Reversible circuits, as presented in [WD10,SM13], are the result of enforcing this requirement on classical Boolean circuits. The interest in classical reversible computing was initially motivated by Landauer's principle, which states that the erasure of information is dissipating energy [Moo12]. The hope was that computers might become more energy-efficient if classical computations would be reversible. Therefore, FANINs and FANOUTs are not allowed into the circuits. The majority of the classical gates are not linear maps. For example the inputs a and b of the AND(a,b) = c gate are impossible to infer from the output c. However, the NOT gate is reversible because its output is the negation of the input, and no information is erased.

The reversibility of classical circuits is achieved by the Toffoli gate (Fig. 1), operating on three bits, where two of them control the bit-flip of the third:  $toffoli(a,b,c)=(a,b,c\oplus ab)$ . Arbitrary classical circuits can be completely constructed using Toffoli gates [NC10, Ch. 3]. While a quantum Toffoli performs effectively the same transformation on qubits, the key difference between quantum and reversible circuits is that the Toffoli gate is not universal for quantum computations because universality also require at least the H gate [Aha03]. Reversible circuits can be considered restricted quantum circuits operating only on computational basis states. However, it is possible to decompose the Toffoli gate into quantum gates (Fig. 1 and Fig. 2a). One decomposition (the quantum version) uses the gate set  $\{CNOT, H, T\}$   $\{T^{\dagger} = T^{7}\}$ , while a second decomposition uses the gates  $\{CNOT, V, V^{\dagger}\}$ . The second representation will be called



Figure 3: Circuits for teleporting the state of a source qubit to a neighbouring destination qubit.

the reversible version (although the V gate is quantum), because its lower gate cost makes it widely used in the designs of reversible circuits [SM13,WD10], although these costs generally don't account for the true nature of error corrected quantum circuits.

### 1.5 Information and Gate Teleportation

Quantum information (qubit states) cannot be copied [WZ82], but there are ways to *move* information from one qubit to another through quantum state *teleportation* (Fig. 3) [BBC<sup>+</sup>93]. The most general teleportation technique [NC10, Ch. 4] is implemented using a slightly different mechanism, but quantum computing models and architectures like [DFS<sup>+</sup>09,NTD<sup>+</sup>14,JMF<sup>+</sup>12,YJG<sup>+</sup>12,FMMC12] use the two circuits presented herein.

Each of the circuits requires an ancilla initialised into either  $|0\rangle$  or  $|+\rangle$ . For the first circuit, after applying the CNOT on the states  $|\psi\rangle=a|0\rangle+b|1\rangle$  and  $|0\rangle$ , the two-qubit state will be  $a|00\rangle+b|11\rangle$ . The measurement of the input qubit, in the X-basis is probabilistic, and depending on its result the final state of the ancilla will be either  $|\psi_1\rangle=a|0\rangle+b|1\rangle$  if  $|+\rangle$  is measured, or  $|\psi_2\rangle=a|0\rangle-b|1\rangle$  for  $|-\rangle$ . The execution of the second circuit, where instead a Z-basis measurement is used, will result in the state of the ancilla being  $|\psi_3\rangle=a|0\rangle+b|1\rangle$  after measuring  $|0\rangle$ , or  $|\psi_4\rangle=a|1\rangle+b|0\rangle$  after measuring  $|1\rangle$ . For both teleportations the final state is the desired one with 50% probability  $(|\psi_1\rangle$  and  $|\psi_2\rangle$ ), while otherwise correctional gates are required, because  $|\psi_1\rangle=Z|\psi_2\rangle$  and  $|\psi_3\rangle=X|\psi_4\rangle$ . The corrections are a direct result of the measurements being probabilistic. The correction mechanism is illustrated in the circuit diagrams by the double vertical lines connecting the measurements to the X/Z gates, indicating a classically controlled gate of either X or Z.

Information teleportation is a linear transformation of the destination qubit, such that its state is exactly the state of the source, but quantum gates are linear transformations, too. It follows that it is possible to construct teleported versions for single-qubit quantum gates. Such constructs are commonly used in the fault-tolerant implementation of quantum gates. The teleportation-based gate circuits for the V,T and P gates are shown in Fig. 4. The teleportations are again probabilistic and the output state requires corrections (derived in [PDNP14]). Gate teleportations are based on  $magic\ states\ [BK05]\ like\ |Y\rangle=\frac{1}{\sqrt{2}}(|0\rangle+i|1\rangle)$  and  $|A\rangle=\frac{1}{\sqrt{2}}(|0\rangle+e^{i\frac{\pi}{4}}|1\rangle)$ . The utilization of magic states and the above tele-

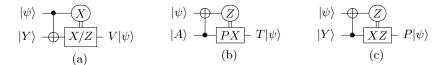


Figure 4: Teleported rotational gates using the magic states  $|A\rangle, |Y\rangle$ . a) The teleported V gate; b) The teleported T gate; c) The teleported P gate.

portation circuits is that they can be implemented using fault-tolerant QECC through a process known as state distillation [BK05,FMMC12], which accounts for the majority of resources necessary for a large-scale error corrected algorithm [DMN13].

The  $R_z(\pi/4)^{\dagger} = T^{\dagger} = R_z(-\pi/4)$  rotation is implemented using the same circuit as the gate T, the only difference being the interpretation of the measurement result in terms of any subsequent correction. Because the  $T,T^{\dagger},V$  and  $V^{\dagger}$  gates can be implemented by teleportations, it follows that the Toffoli gate (in both its quantum and reversible versions) can be decomposed into teleportation sub-circuits.

The magic states in the construction of fault-tolerant gates are assumed to be high-fidelity (As high as the fidelity of the underlying quantum information protected by the QECC). Otherwise, high-fidelity instances are obtained after distilling multiple low-fidelity states using circuits consisting entirely of CNOTs and measurements [BK05]. For example, the distillation of a single  $|Y\rangle$  state from low-fidelity  $|Y\rangle$  ancillae is reported in [BK05], reducing the infidelity, p, of the output from O(p), p < 1, of the seven inputs to  $O(p^3)$  on the output.

# 2 The ICM Representation

In state-of-the-art fault-tolerant quantum circuits, two sources of non-determinism can be distinguished. First, errors can occur during calculation due to undesired interaction with the environment. The errors are handled by quantum error-correcting codes [DMN13]. Second, as mentioned above, the realisation of gates by teleportation is inherently probabilistic. The outcome of the gate application is correct with 50% probability and requires a correction with 50% probability even in absence of errors.

Circuit gate dynamics, as presented in Section 1, is the consequence of applying specific quantum gates (e.g. T) by teleportation. Correctional gates may or may not be required, depending on the outcome of a measurement that is only available when the circuit is being executed. A further source of non-determinism is error-correction, which is not considered herein and is handled at a lower level in the overall design stack of a quantum circuit [FMMC12].

A circuit with a dynamic gate list is difficult to execute on a quantum computer, and is furthermore difficult to optimise. This section introduces the ICM representation, which replaces the non-deterministic gate dynamics with an exact

gate list. The resulting circuit still contains correctional mechanisms, but these are controlled by measurement results of introduced ancillae and active feedforward determining subsequent measurement choices. We essentially fan-out using extra ancillae to remove the complication of dynamic circuit construction with fault-tolerant and reversible quantum circuits.

# 2.1 Non-deterministic Resource Requirements

Gate corrections may or may not be required after each teleportation. They consist in applying  $X,\,Y,\,Z$  or P gates to the calculated result. Therefore, the total number of gates in the circuit depends on the number of corrections, and this number is not known a priori because the need for corrections is determined only during circuit execution (each individual teleportation has a 50:50 chance of each ancilla measurement result, so the possibilities grow exponentially in the number of teleported gates). Moreover, corrections require an introduction of additional ancillae qubits, thus making the computation total number of qubits unpredictable as well.

It can be shown that X, Y and Z corrections (Pauli corrections) do not have to be addressed immediately in a quantum way after an unsuccessful gate application. Instead they can be postponed to the end of calculation using Pauli tracking [PDNP14] and instead of applying an active quantum gate to the data, we simply reinterpret the meaning of the classical measurement results. However, this technique does not apply to P corrections necessary for implementing the T gate (Section 1.5). This is because the P correction does not commute through either the P gate of the target of a P correction does not commute through and changes the probability distribution of subsequent P-basis measurements.

For example, in the teleported T gate (Fig. 4b), applying a CNOT on two qubits  $|t\rangle = \frac{1}{\sqrt{2}}(|0\rangle + r|1\rangle)$  (where  $r = e^{\frac{i \cdot \pi}{4}}$ ) and  $|q\rangle = a|0\rangle + b|1\rangle$  results in  $|qt\rangle = (a|00\rangle + ar|11\rangle + b|10\rangle + br|01\rangle)/\sqrt{2}$ . The  $|0\rangle$  result of the first qubit's Z-measurement will result in the second qubit's state as if it were directly rotated by T:  $a|0\rangle + br|1\rangle$ . If the measurement result is  $|1\rangle$ , the state is  $ar|1\rangle + b|0\rangle$ , which after a PX correction is required [PDNP14], and it can be applied using the circuit from Fig. 4c.

The P correction requires us to dynamically change the circuit being executed as this correction cannot be classically tracked. A second ancilla is introduced in the  $|Y\rangle = |0\rangle + i|1\rangle$  state, a CNOT applied between the ancilla and the state to be corrected, and the input is measured according to Fig. 4c. For an n-qubit circuit C with a gate list GL(C), each probabilistic P correction increments the number of qubits by one, and inserts a P gate into the gate list.

The problem of applying the P gate dynamically is solved by introducing into the circuit the possibility to operate both a teleported identity gate, used when no correction is needed, and a teleported P gate. Similarly to a classical demultiplexer the measurement result of the teleported T gate is used to decide, at run-time, whether I or P gate is applied. Finally, after performing either the I or P correction, the corresponding state has to be routed to a single

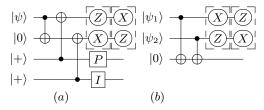


Figure 5: Teleportations: a) Selective destination; b) Selective source [Fow12].

qubit. This is realised by classically controlled teleportations in a manner similar to a classical multiplexer with the select signal being the measurement result of the teleported T gate. Classically controlled teleportations were described in [Fow12], and a circuit using these mechanisms will have a fixed number of qubits and a determined gate list. Compared to a dynamically changing circuit, these are larger, but the predictability of these parameters is useful for circuit optimisation.

For selective destination teleportation (Fig. 5) the first group of measurements  $(Z_1X_2)$  where the subscripts indicate the qubit's number) will teleport  $|\psi\rangle$  on the third qubit where it will be corrected by P. The second group of measurements  $(X_1Z_2)$  will teleport the state to the fourth qubit where the trivial correction I is applied, thus leaving the state unchanged. In the selective source teleportation the  $X_1Z_2$  measurements will select  $|\psi_1\rangle$  for teleportation on the third qubit, while the second measurement group  $(Z_1X_2)$  will teleport  $|\psi_2\rangle$  [Fow12]. The selective teleportation circuits require only Pauli corrections, which are not shown in the diagrams, because their application can be postponed to the end of the computation and classically tracked.

As a consequence, Pauli tracking can reduce but not completely eliminate the non-determinism of fault-tolerant circuits. This implies that standard synthesis methods which optimise gate count and/or number of qubits are not applicable to teleportation-based quantum circuits because these numbers are not well-defined. It is possible to circumvent the non-determinism by using "conditional-identity construction" which results in the maximal possible number of gates. The initial gate dynamics of a circuit, with all the classically controlled corrections replaced by classically controlled teleportations, is interpreted as the dynamics of the measurements .

### 2.2 ICM Correctness and Construction

The role played by the structured representation of circuits was recognised in [AG04], where stabiliser circuits were decomposed into a canonical sequence of sub-circuits constructed from a single type of gates. In the context of fault-tolerant quantum computing, the systematic derivations of the circuits [ZLC00] uses teleportation sub-circuits, too. However, the combination of the fault-tolerant constructions with the regular gate decompositions [SBM06], required for efficient synthesis algorithms, is limited by the realistic requirements of future

quantum computing architectures. Nevertheless, structured mapping techniques between various architectures were investigated in [HNYN11,CMS07]. These approaches were targeted at specific quantum hardware properties, such as nearest-neighbour interaction between qubits, but fault-tolerant constructions were not specifically addressed.

ICM is a structured representation, which consists in the regular representation of arbitrary quantum and reversible circuits using the  $UGS_{ft}$  gate set, where the single-qubit rotational gates are teleportation-based. Circuits are transformed into the ICM representation after decomposing all non- $UGS_{ft}$  gates into  $UGS_{ft} = \{CNOT, H, T\}$  component gates, and simultaneously introducing, where necessary, selective source and destination teleportation circuits into the resulting circuit.

The correctness of the ICM representation is based on the observation that the teleported gate circuits (Figs. 4c,4b and 4a) and the selective teleportation circuits (Fig. 5) consist entirely of qubit initialisations, CNOT gates and qubit measurements. Thus, decomposing an arbitrary circuit into elements that can be expressed entirely using the above mentioned sub-circuits, will consist only of initialisations, CNOTs and measurements. The circuit from Fig. 5a can be rewritten, such that the P gate will not be directly applied: in general,  $R_z$  rotations (e.g. the P gate) commute with the control of CNOT gates [NC10, Ch. 4]. As a result, the P gate can be moved on the left side of the CNOT, and  $P|+\rangle = |Y\rangle$ . The third qubit from Fig. 5a will be initialised into  $|Y\rangle$  instead of  $|+\rangle$ .

The ICM representation of an arbitrary quantum circuit is the result of applying algorithm presented in this paper. The algorithm is taking a circuit composed of gates from the set  $\{Toffoli, CNOT, C\text{-}V \text{ and } C\text{-}V^{\dagger}, H, P, T\}$ , and performs pattern replacements resulting in the circuit CICM (Line 1) consisting of gates from  $UGS_{ft}$ . The Toffoli gates are decomposed into single qubit rotations (either  $\{V, V^{\dagger}\}$  or  $\{H, T, T^{\dagger}\}$ ) and CNOT gates. The Hadamard gates are replaced with the series of Z- and X-axis rotational gates (P and V gates). Afterwards, each P and V gate is replaced using the corresponding teleportation-based gate implementations from Figs. 4c,4b,4a. The effect of replacing a gate G acting on qubit i is that an ancilla is introduced on the position i+1. Thus, all the gates following the initial application of G on i are moved to i+1 (Line 20).

The ICM representation is obtained by moving all the single-qubit measurements to the end of the circuit, and all the ancillae initialisations to the beginning of the circuit. The middle part of the resulting circuit consists entirely of CNOT gates. The single qubit measurements are then temporally staggered (e.g. Fig. 6), such that the results of previous measurements determine the basis choices for subsequent measurements to teleport data to pre-prepared ancillae. In the case of the teleported T gate, this procedure dictates to either apply P gate corrections or not, as required.

#### 2.3 Resource Analysis

Transforming arbitrary quantum and reversible circuits into the ICM representation requires the introduction of supplemental ancillae, CNOT gates and measurements. The obtained representation is an augmented version of the initial circuit, and there is a constant resource overhead associated with each gate transformation. In the following the gate cost of implementing a sub-circuit (gate) S is represented by gc(S), and the ancilla cost is denoted ac(S).

**Theorem:** The ICM representation of a quantum circuit C with  $n_T T$  gates,  $n_P P$  gates,  $n_V V$  gates,  $n_H H$  adamard gates and  $n_{Tf}$  Toffoli gates requires  $ac(C) = 5n_T + n_P + n_V + 3n_H + 42n_{Tf}$  ancillae and  $gc(C) = 6N_T + n_P + n_V + 3n_H + 55n_{Tf}$  additional gates.

**Proof:** The central quantum gate is T, which requires ac(T) = 5 ancillae and gc(T) = 6 CNOTs. One of the ancillae is the one initialised into  $|A\rangle$ , three other ancillae are used for the selective destination teleportation sub-circuit, and, finally, the fifth ancilla is introduced for the selective source teleportation and represents the output of the teleported T gate.

The P and the V gates introduce a single ancilla ac(P) = ac(V) = 1 initialised into the  $|Y\rangle$  state, and because the teleportation circuits require a single CNOT gc(P) = gc(V) = 1. The Hadamard gate being implemented as a sequence of P and V gates generates a gate cost of gc(H) = 3gc(P) = 3, and an ancilla cost of ac(H) = 3ac(P) = 3.

The quantum version of the Toffoli gate (denoted  $Toffoli_q$ ) decomposition contains 6 CNOTs, 7 T gates, one P and two H gates (Fig. 1), and thus  $gc(Toffoli_q) = 6 + 7gc(T) + (1 + 2 \times 3)gc(P) = 55$  and  $ac(Toffoli_q) = 7ac(T) + (1 + 2 \times 3)ac(P) = 42$ .

**Note:** The Theorem was formulated for the ICM decomposition of quantum Toffoli gates, but can easily be updated to include the reversible version of these gates (in the following denoted  $Toffoli_2$ ). These gates are decomposed into quantum gates, and the initial version contains 2 CNOT gates and 3 controlled-V gates (denoted by CV), which are further decomposed (Fig. 2b) into 2 Hadamard gates, 3 T and 2 CNOTs. Therefore, because gc(CV) = 2gc(H) + 3gc(T) + 2 = 26 and ac(CV) = 2ac(H) + 3ac(T) = 21, the gate cost of the reversible Toffoli is  $gc(Toffoli_2) = 3gc(CV) + 2 = 80$  and the ancilla cost  $ac(Toffoli_2) = 3ac(CV) = 63$ .

State distillation (see Section 1.5) is not analysed here, as it is an intrinsic requirement for any type of computation where magic states are required. An exhaustive and complete analysis of the distillation circuits overhead is presented in [DSMN13] and, as a consequence, the present ICM resource analysis is a continuation of that work.

```
Require: Circuit C composed from {Toffoli, CNOT, H, P, T}
1: Circuit CICM \leftarrow C
2: Replace in CICM the Toffoli gates with their decomposition (Figure 1 or Figure 2a)
3: Replace in CICM the H gates with PVP
4: forall P gates in CICM
    Introduce the ancilla a_p below the qubit having P
    Construct the circuit for the teleported P gate
7.
    Move all the gates following the initial P onto a_p
8: endfor
9: forall V gates in CICM
10: Introduce the ancilla a_v below the qubit having V
     Construct the circuit for the teleported V gate
     Move all the gates following the initial V onto a_v
14: forall T gates in CICM
15: Introduce the ancilla a_c below the qubit having T
16:
    Construct the circuit for the teleported T gate
17:
     Introduce 4 ancillae below the previous ancilla
     Construct the selective destination circuit where a_c corresponds to the first qubit,
and s_3 and s_4 are the third and fourth qubits respectively
19: Construct the selective source circuit where s_3 corresponds to the first qubit,
s_4 to the second qubit, and a_{out} is the third qubit
20: Move all the gates following the initial T onto the ancilla a_{out}
21: endfor
22: return CICM
```

# 3 Discussion

The ICM representation of an arbitrary circuit prepared into a fault-tolerant manner will not affect its properties. Therefore, fault-tolerance statistics will not be discussed. The results of executing the implementation of Algorithm 1 on circuits from the RevLib benchmark are presented in Table 1. The EQ circuits consisted of gates from the set  $\{CNOT, C\text{-}V, C\text{-}V^{\dagger}\}$  and the NCT circuits from the set  $\{Toffoli, CNOT, X\}$ . The best-case non-ICM representation consists of the teleportation-based gate construction where no P corrections is required for the T gate. The worst-case non-ICM scenario assumed that all the T gates require the P correction. For other types of gates the corrections can be tracked through the circuit [PDNP14], but tracking is not possible for the probabilistic P-correction (see Section 2.1). In order to illustrate the benefit of the ICM representation the time required for executing the critical path of the decomposed circuits was computed. The model presumed a time cost of 10 for initialisations, and a cost of 1 for the CNOTs and the measurements.

It can be seen that the time required by ICM circuits is predictable and better than the worst-case time of circuits before transformation. Note that longer time translates to higher decoherence and more stringent requirements on quantum error-correction.

Original circuit								Fault-tolerant circuit								
							Best-Case Non-ICM			Worst-Case Non-ICM			ICM			
Circuit	Qub.	X	C-X	Toff.	C-V	C-V <sup>†</sup>	Ancilla	CNOT	Time	Ancilla	CNOT	Time	Ancilla	CNOT	Time	
EQ/0410184_170	14	8	33	0	17	16	297	396	255	297	495	736	693	891	435	
EQ/3_17_15	3	1	3	0	2	4	54	69	56	54	87	177	126	159	100	
EQ/add16_175	49	0	32	0	48	16	576	736	287	576	928	1013	1344	1696	551	
EQ/add32_185	97	0	64	0	96	32	1152	1472	543	1152	1856	1973	2688	3392	1063	
EQ/add64_186	193	0	128	0	192	64	2304	2944	1055	2304	3712	3893	5376	6784	2087	
EQ/add8_173	25	0	16	0	24	8	288	368	159	288	464	533	672	848	295	
$EQ/c2_182$	35	15	121	0	116	53	1521	1980	366	1521	2487	1172	3549	4515	661	
$EQ/decod24-v0_40$	4	1	5	0	2	1	27	38	40	27	47	95	63	83	60	
$EQ/decod24-v1_42$	4	1	5	0	2	1	27	38	41	27	47	87	63	83	59	
$EQ/decod24-v2\_44$	4	1	5	0	1	2	27	38	41	27	47	95	63	83	60	
$EQ/decod24-v3\_46$	4	0	6	0	1	2	27	39	42	27	48	96	63	84	61	
EQ/fredkin_5	3	0	4	0	1	2	27	37	41	27	46	94	63	82	59	
EQ/graycode6_48	6	0	5	0	0	0	0	5	16	0	5	16	0	5	16	
EQ/miller_12	3	0	5	0	1	2	27	38	42	27	47	95	63	83	60	
EQ/peres_8	3	0	1	0	1	2	27	34	38	27	43	92	63	79	57	
EQ/toffoli_1	3	0	2	0	2	1	27	35	38	27	44	92	63	80	57	
EQ/toffoli_double_3	4	0	4	0	2	1	27	37	38	27	46	94	63	82	59	
NCT/0410184_169	14	8	27	11	0	0	297	412	248	297	511	788	693	907	431	
NCT/add16_174	49	0	32	32	0	0	864	1152	440	864	1440	1514	2016	2592	807	
NCT/add32_183	97	0	64	64	0	0	1728	2304	840	1728	2880	2938	4032	5184	1559	
NCT/add64_184	193	0	128	128	0	0	3456	4608	1640	3456	5760	5786	8064	10368	3063	
NCT/add8_172	25	0	16	16	0	0	432	576	240	432	720	802	1008	1296	431	
NCT/c2_181	35	18	35	63	0	0	1701	2240	345	1701	2807	1177	3969	5075	631	
NCT/cnt3-5_180	16	0	5	10	0	0	270	355	60	270	445	186	630	805	102	
NCT/graycode6_47	6	0	5	0	0	0	0	5	16	0	5	16	0	5	16	
NCT/ham7_106	7	0	19	6	0	0	162	229	145	162	283	441	378	499	245	

Table 1: Comparison between non-ICM and ICM representation

# 3.1 Example

The systematic transformations of the T gate and of the controlled-V gate decomposition from Fig. 2b are presented after applying Algorithm 1 and obtaining a circuit composed from  $UGS_{ft}$  (see Section 1.3). The ICM representation of the T gate (Fig. 6) takes the  $|in_0\rangle$  qubit, and after performing the CNOT with the  $|A\rangle$  ancilla, selectively teleports (the leftmost group of gates) the intermediary state to either the fourth or the fifth qubit.

The measurement of the first qubit  $(Z_1)$  is followed by either the measurement pattern  $Z_2X_3$  if the result of the teleported T needs a P correction, or the measurement pattern  $X_2Z_3$  if the result was correct up to Pauli corrections. The correctness of the teleported gate application is indicated by the measurement result. Applying the  $Z_2X_3$  pattern teleports the intermediary state on the output qubit marked by  $|out_0\rangle$ , and the fourth and fifth qubits are measured using  $X_4Z_5$ . Otherwise, the measurement  $Z_4X_5$  will result in teleporting the state of the fifth qubit on the sixth qubit. The measurement of specific qubit groups depends on the results of previous measurements.

The controlled-V gate ICM representation (Fig. 7 after applying Algorithm 1) has the input states  $c_{in}$  (control) and  $t_{in}$  (target) and outputs  $c_{out}$  and  $t_{out}$ . The individual decomposition of the single-qubit gates from Fig. 2b is highlighted by the dashed bounding boxes. The boxes containing three CNOTs are implementations of the Hadamard gate where for each constituent sub-gate a CNOT and a  $|Y\rangle$ -qubit are used. The ancillae introduced by the ICM transformation are affecting the distance between the control and the target of the initial CNOTs (not marked by bounding boxes). The order of the measurements is dictated by the temporal order of the bounding boxes, meaning that the measurements implementing the leftmost T and H can be applied in parallel. Afterwards, the measurements associated to the middle bounding boxes can be again executed

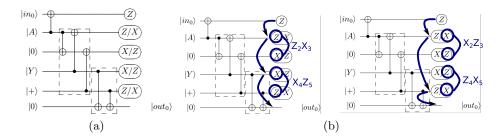


Figure 6: a) The ICM version of the T gate [Fow12]; b) The arrows sketch the information flow between the ancillas: a P gate correction is the result of the  $Z_2X_3X_4Z_5$  measurement pattern, and the  $X_2Z_3Z_4X_5$  measurement pattern is used if the teleported T gate application was correct.

in parallel. Finally, the last Hadamard gate from the initial circuit is applied by measuring the last three qubits.

#### 4 Conclusion

The usual assumptions made for quantum optimisation techniques do not necessarily hold for the fault-tolerant circuits because of their inherent dynamicity. A regular representation of quantum and reversible circuits was presented starting from the fault-tolerant implementation of quantum circuits. The ICM representation is a consequence of the results presented in [Fow12,PDNP14] and has the potential, when combined with the synthesis method from [AMMR13,AMM14], to be used for future circuit optimisation techniques.

The results indicate that, while making a quantum circuit fault-tolerant significantly increases its gate count and the number of required ancilla qubits, the ICM representation outperforms direct mapping without enforcing the ICM condition with respect to both predictability and worst-case execution time. The major advantage of this representation is that it produces a deterministic circuit description for a higher level circuit. A deterministic description is essential to allow for more global circuit optimisations in various error corrected implementations. Future work will investigate quantum circuit synthesis, optimisation and validation techniques based on the ICM representation.

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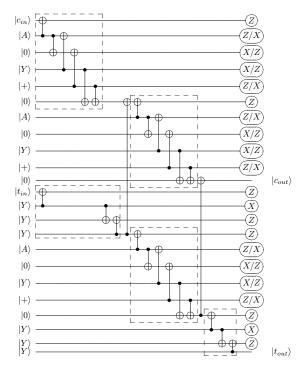


Figure 7: The ICM representation of the controlled-V gate. There are three ICM T-gate applications (see Fig. 6) and two ICM Hadamard applications (marked by bounding boxes in which three ancillae are measured using the ZXZ pattern)

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