

Performance-Portable Many-Core Plasma Simulations: Porting PIconGPU to OpenPower and Beyond ^{*}

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Abstract. With the appearance of the heterogeneous platform OpenPower, many-core accelerator devices have been coupled with Power host processors for the first time. Towards utilizing their full potential, it is worth investigating performance portable algorithms that allow to choose the best-fitting hardware for each domain-specific compute task. Suiting even the high level of parallelism on modern GPGPUs, our presented approach relies heavily on abstract meta-programming techniques, which are essential to focus on fine-grained tuning rather than code porting. With this in mind, the CUDA-based open-source plasma simulation code PIconGPU is currently being abstracted to support the heterogeneous OpenPower platform using our fast porting interface cupla, which wraps the abstract parallel C++11 kernel acceleration library Alpaka.

We demonstrate how PIconGPU can benefit from the tunable kernel execution strategies of the Alpaka library, achieving portability and performance with single-source kernels on conventional CPUs, Power8 CPUs and NVIDIA GPUs.

Keywords: OpenPower, heterogeneous computing, HPC, C++11, CUDA, OpenMP, particle-in-cell, platform portability, performance portability

1 Introduction

PIconGPU [2] is a fully-relativistic, multi-GPU, 3D3V particle-in-cell (PIC) code. As such it allows to model the mutual interaction between electromagnetic fields and charged particles, including effects of retardation in special relativity (SRT) and the collective motion of collisionless plasmas, by solving Maxwell's equations self-consistently for charged particles and electromagnetic fields. Besides the satisfied demand for large scales and high resolutions by computing the whole PIC cycle on GPUs, simulations of laser-ion acceleration from overdense

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targets [19] induce a further complexity in the dynamics of the plasma from collisional excitation and ionization processes. As the free electron density from ionization processes determines intrinsic observables such as the plasma wavelength, the modeling of underlying quantum processes needs to be taken into account and is not yet covered in the plain electrodynamics provided by PIC. Our approach to enhance the PIC algorithm is therefore to add a Monte Carlo step in the simulation with 0-D atom physics from SCFLY [4]. This method requires to calculate the transition rate matrix, representing the likelihood of change of the atomic configuration of each ion from one time step to the next. Each of the quantum processes has its own individual models, calibrated with experimental and theoretical estimates. Even when considering the reduction of possible transitions by using an effective number of states, removing physically forbidden and very unlikely transitions, the total number of transitions can grow quadratically with the number of considered configurations. In combination with the dependency of the transition matrix elements on local quantities, such as the energy distribution of neighboring electrons and photons of each individual ion in the plasma, the required amount of memory can easily grow into the size of several dozen gigabytes for a non-equilibrium system.

None of the accelerators that are currently available or announced for the near future fulfill these memory requirements. However, the accelerator's host system provides access to fast and large main memories and file systems. The host's CPUs are used as a first computing stage to reduce the full transition matrix to smaller lookup tables. CPUs excel at this task, since they typically provide better performance on trigonometric functions and implicit solvers. Accordingly, only relevant data needs to be streamed to the GPU.

The OpenPower platform couples various advanced hardware technologies on the same system [11] such as Power CPUs, NVIDIA GPUs, and fast CPU-GPU interconnect technology [7]. To fully utilize the compute power of this platform, it is currently necessary to use various programming models such as CUDA for GPU and OpenMP for CPU. However, this style of programming has the disadvantage that the code is difficult to maintain and it requires more work to switch algorithms between GPU and CPU implementations. A uniform programming model allows to selectively determine the kernel execution hardware depending on the algorithmic requirements. These requirements depend on the models of the individual physical process: some are memory bound, some compute bound, and the user chooses, based on domain knowledge and the relevance, on which hardware these processes should be executed.

Currently, widely utilized uniform parallel programming models such as OpenCL [17] do not fulfill all our requirements of a sustainable, open, maintainable, testable, optimizable, and single-source programming model. Loop and container based approaches such as RAJA [9], Kokkos [5], and OpenMP 4.0 [15] would require a complete redesign of the CUDA based PIConGPU code. With *Alpaka* [20], there exists an interface for parallel kernel acceleration which enables the programmer to compile single-source C++ kernels to various architectures, while providing all the requirements mentioned above. As a first step to selec-

tive kernel acceleration on the OpenPower platform, PIConGPU has been ported with the CUDA-like interface *cupla* [16] to Alpaka, which currently allows for an execution either on the CPU or on the GPU.

This paper is structured as follows. In Section 2, we give a brief overview on PIConGPU, Alpaka, and *cupla*. In Section 3, we provide our experiences on porting PIConGPU with *cupla* from CUDA to Alpaka. Finally, the ported prototype is evaluated on various architectures in Section 4.

2 Preliminaries

2.1 PIConGPU

PIConGPU is a multi-GPU particle-in-cell (PIC) code for three-dimensional field-particle interaction with high spatial resolution. The code decomposes its global simulation domains into a grid of cells. Cells are grouped into a cuboid volume called *super cell*, and multiple of these super cells are again grouped into a cuboid volume which defines the local simulation domain of a single GPU.

Additionally, there is a second, spatially continuous domain for finite size macro particles such as ions and electrons. They are able to move through the cells and interact with them, making PIC a particle mesh algorithm [3]. Macro particles are grouped in frames, where each frame contains as many macro particles as there are cells in a super cell. Frames are stored in a doubly linked list and correspond to a particular super cell.

Most of the operations on the cells are local stencils which include only a few neighboring cells and are therefore well suited to CUDA programming model of a multidimensional grid. PIConGPU is mapped to this model as follows: The local simulation domain is mapped to the grid of a single GPU. A super cell is mapped to a block that contains as many threads as there are cells — in our simulation this amounts usually to 256 cells. A thread calculates the field of a cell and its proportion of particles of its super cell.

2.2 Alpaka and *cupla*

Alpaka provides a uniform, abstract C++ interface to a range of parallel programming models. It can express multiple levels of parallelism and allows for generic programming of kernels either for a single accelerator device or a single address space with multiple CPU cores. The Alpaka abstraction of parallelization is influenced by and based on the groundbreaking CUDA abstraction of a multidimensional grid of blocks of threads. The four main execution hierarchies introduced by Alpaka are called *grid*, *block*, *thread*, and *element* level. The element level denotes an amount of work a thread needs to process sequentially. These levels describe an index space which is called *work division*. Other programming models call these levels differently e.g. OpenCL *work-groups* of *work-items*, OpenMP *teams* of *threads*, and OpenACC *gang*, *worker*, and *vector*.

Separating parallelization abstraction from specific hardware capabilities allows for an explicit mapping of these levels to hardware. The current implementation includes mappings to programming models, called back-ends, such as OpenMP, CUDA, C++ threads, and boost fibers [14]. Nevertheless, mapping implementations are not limited to these choices and can be extended or adapted for application-specific optimizations. Which back-end and work division to utilize is parameterized per kernel within the user code.

A fast approach to port CUDA code to Alpaka is provided by the CUDA-like Alpaka interface `cupla` [*qχap'la?*]. `Cupla` leaves most CUDA API calls unchanged, yet performs Alpaka calls in the background. Thus, `cupla` provides a simple and fast porting approach by reducing the number of lines of the original CUDA code a programmer needs to modify.

3 Porting with `cupla`

In this section we discuss the steps necessary to port the CUDA accelerated code of PIConGPU from GPU to CPU hardware. Our approach is to replace CUDA by the CUDA-like interface `cupla`. Afterwards, we can utilize Alpaka's CUDA and OpenMP 2.0 back-ends to execute our kernels on both GPUs and CPUs.

`Cupla` leaves most parts of the CUDA code unchanged such as memory allocations, memory copies, stream handling, device handling, and index queries. The programmer is still required to handle three porting steps. Firstly, the `cuda_runtime.hpp` include has to be replaced by `cuda_to_cupla.hpp` and all `.cu` files renamed to `.cpp`. Secondly, The `__host__`, `__device__`, and `__global__` keywords need to be replaced by equivalent `cupla` macros and CUDA global functions rewritten into parenthesis operators of C++ functors. The accelerator object of the accelerator template type has to be passed to these operators and the underlying device functions. Finally, each shared memory allocation has to be replaced by an equivalent `cupla` macro. Listing 1 shows equivalent CUDA and `cupla` code snippets of a kernel function initializing an array by a constant value. In contrast to the CUDA kernel, each thread of the `cupla` kernel loops over the `x` dimension of the element level.

The native PIC code consists of about forty thousand lines of code. This code is a mixture C++11 and platform-dependent CUDA code. R. Widera programmed about two days, applied the `cupla` porting steps mentioned above, touched most of our nine hundred device functions, forty kernels, amounting to two thousand lines of code, to provide the first Alpaka based prototype. Although this prototype did not utilize the *element* level, it was already executable on both a Power8 device using the OpenMP 2.0 back-end and on an NVIDIA device using the CUDA back-end. The number of threads in a block was left unchanged. Accordingly, the domain of a super cell is processed by a block consisting of 256 threads.

This block-size leads to inefficient communication between threads on the Power8 when the the element level is omitted, resulting in more frequent cache misses and a decrease in performance. Accordingly, the integration of the ele-

```

1 // CUDA Kernel
2 __global__ void kernel ( int * data )
3 {
4     int id = blockDim.x * blockIdx.x
5             + threadIdx.x;
6     data[ id ] = 42;
7 }

1 // Alpaka Kernel
2 struct void kernel {
3     template < typename Acc >
4     ALPAKA_FN_ACC void operator () (
5         Acc const & acc,
6         int * data
7     ) const
8     {
9         int id = blockDim.x * blockIdx.x * elemDim.x
10                + threadIdx.x * elemDim.x;
11         for( int elem = 0; elem < elemDim.x; ++elem)
12             data[ id + elem ] = 42
13     }
14 };

```

Fig. 1. CUDA and cupla kernels which initialize each element in the input array `data` by the value 42. The cupla kernel on the bottom was created through wrapping the CUDA kernel on the top within a C++ functor. Each thread of the cupla kernel processes multiple elements through looping over the dimensions of the additional element level. In the cupla kernel `blockDim`, `blockIdx`, `threadIdx`, and `elemDim` are pre-processor macros accessing the `acc` variable.

ment level enables for a work division of blocks with a single thread and multiple elements to calculate the entire domain of a super cell. This provides a more efficient mapping of Alpaka-threads to hardware threads and, therefore, an improved vectorization and cache utilization by the compiler. The integration of the element level required to loop over the fixed-size element index space for each sequential kernel part. These sequential parts were wrapped in lambda functions. Furthermore, single element variables were expanded to multidimensional fixed-size arrays. This change, on three thousand lines of code, took our developer about ten days.

To sum up, our developer modified about five thousand lines of code in a matter of two weeks, after which the entire forty thousand lines PIConGPU code could be compiled and run efficiently on CPU and GPU devices. It was not necessary to modify the core data structures or algorithms of PIConGPU. The element level has been added to enable a single thread to process the domain of a super cell. In the following section we will evaluate the performance of our Alpaka-based PIC simulation on both architectures.

Table 1. Compute nodes for evaluation (core counts in braces are HW threads).

Vendor	AMD	Intel	IBM	NVIDIA
Architecture	Interlagos [1]	Haswell [10]	Power8 [6]	Kepler [12]
Model	Opteron 6276	Xeon E5-2698v3	Power8 8247-42L	K80 GK210
Used devices per node	4	2	2	1
Cores per device	16	16 (32)	10 (80)	2496
Base clock frequency	2.3 GHz	2.3 GHz	2.1 GHz	0.56 GHz
Release date	Q4/2011	Q3/2014	Q1/2014	Q4/2014
Peak performance(sp)	960 GFLOPS	2354 GFLOPS	1120 GFLOPS	4350 GFLOPS
Peak performance(dp)	480 GFLOPS	1177 GFLOPS	560 GFLOPS	1450 GFLOPS

4 Evaluation

This section provides the evaluation of the PIConGPU code [18] that was ported to various compute architectures (see Table 1). We measured the runtime and performance of the memory-bound PIC algorithm as implemented in PIConGPU with a simulation of the Kelvin-Helmholtz instability [3] for one thousand time steps in double and single precision and compared these results between the various architectures. The simulation was parameterized with the Boris pusher, Esirkepov current solver, Yee field solver, trilinear interpolation in field gathering, three spatial dimensions (3D3V), 128 cells in each dimension, electron and ion species with each sixteen particles per cell, and quadratic-spline interpolation (TSC) [8]. On all CPU devices the OpenMP 2.0 back-end was used with a block consisting of a single thread with 256 elements. On NVIDIA GPUs the CUDA back-end is used with a block consisting of 256 threads with a single element. All GPU evaluations are compiled with `nvcc`¹ 7.0 and all CPU evaluations with `gcc`² 4.9.2.

Figure 2 displays the measured runtime and efficiency of the evaluated simulation. On the NVIDIA K80, the differences in runtime between the native and the ported PIC code are about one percent for single precision. For double precision, the Alpaka based code is even faster, because Alpaka emulates double *atomicAdd* using *atomicCAS* instead of the slower *atomicExch* used by the native PIConGPU implementation. Nevertheless, this small optimization could have been introduced easily into the native PIConGPU code to achieve the same

¹ `--use_fast_math --ftz=false -g0 -O3 -m64`

² `-g0 -O3 -m64 -funroll-loops -march=native --param max-unroll-times=512 -ffast-math`

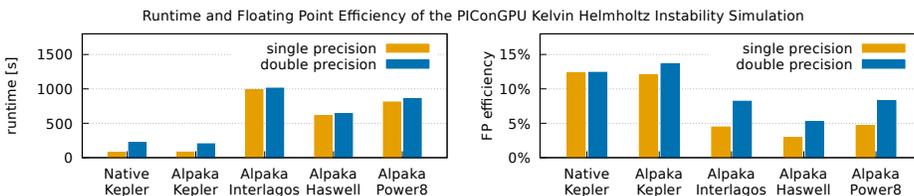


Fig. 2. As an example to evaluate a memory-bound PIC code, runtime and floating point efficiency of the PIConGPU Kelvin-Helmholtz instability simulation for single precision and for double precision was measured on various architectures (see Table 1).

runtime results. According to these measurements, Alpaka can keep its promise of zero-overhead abstraction on the same architecture even for rather complex applications such as PIConGPU. The runtime between GPU and CPU implementations differ in one order of magnitude for single precision. However, the results need to be evaluated in relation to the theoretical peak performance of the particular architecture. This metric is denoted as floating point efficiency in Figure 2. Regarding floating point efficiency, CPU and GPU vary by a factor of three to four on single precision and by a factor of two on double precision. Thus, Alpaka provides not just portability between GPU and CPU, but decent performance on both. All evaluated CPU architectures show similar runtime and efficiency characteristics. Nevertheless, the Intel architecture offers the lowest runtime and highest (theoretical) peak performance of all evaluated CPU devices. However, there still exists some potential to increase performance, as it only provides five percent floating point efficiency on double precision. While the IBM and AMD architectures fare slightly better with about eight percent double precision efficiency, there is still a lot of potential compared to the GPU efficiency. By refining the Alpaka back-ends and tuning the work division, this potential can be utilized to increase the performance of the CPU architectures even more.

5 Conclusion

We have presented the current progress in porting the particle-in-cell simulation PIConGPU onto the OpenPower platform through utilizing the CUDA-like Alpaka interface *cupla*. The core routines of the forty thousand lines mixed C++ and CUDA code have been ported from CUDA to Alpaka within two weeks. Through this abstraction, the ported PIConGPU implementation is executable on AMD, IBM, Intel, and NVIDIA architectures. The code was not just ported, but has been moved to a generic *single-source* multi-platform programming model. Thus, PIConGPU never needs to be ported again.

The native CUDA version and the Alpaka version show no significant differences in runtime or performance on the NVIDIA hardware, which demonstrates zero overhead abstraction capabilities of Alpaka. GPU and CPU devices differ in a factor of about two in efficiency on double precision, providing decent performance among the evaluated architectures.

Future work will focus on the evaluation of each kernel on CPU and GPU hardware separately. Based on these measurements, we want to provide a static mapping of kernels to heterogeneous hardware to achieve the best possible overall performance on the particular HPC system. Furthermore, we want to complete the porting of the remaining simulation plugins within PIConGPU and add a more fine-grain element level implementation.

The code is ready for the upcoming Power9 and NVIDIA Volta-based heterogeneous systems such as Summit [13] at the Oak Ridge National Laboratory. By using Alpaka we have the possibility to optimize and adapt our back-ends to these systems once they are fully specified and available for evaluation.

References

- [1] AMD. *AMD Opteron 6200 Series Processor Quick Reference Guide*. https://www.amd.com/Documents/Opteron_6000_QRG.pdf. [Online; accessed April 11, 2016].
- [2] Heiko Burau, René Widera, Wolfgang Hönig, Guido Juckeland, Alexander Debus, Thomas Kluge, Ulrich Schramm, Tomas E. Cowan, Roland Sauerbrey, and Michael Bussmann. “PICongPU: A fully relativistic particle-in-cell code for a GPU cluster”. In: *Plasma Science, IEEE Transactions on* 38.10 (2010), pp. 2831–2839.
- [3] Michael Bussmann, Heiko Burau, Thomas E. Cowan, Alexander Debus, Axel Huebl, Guido Juckeland, Thomas Kluge, Wolfgang E. Nagel, Richard Pausch, Felix Schmitt, Ulrich Schramm, Joseph. Schuchart, and René Widera. “Radiative signatures of the relativistic Kelvin-Helmholtz instability”. In: *Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis*. ACM. 2013, p. 5.
- [4] H.-K. Chung, M. H. Chen, and R. W. Lee. “Extension of atomic configuration sets of the Non-LTE model in the application to the $K\alpha$ diagnostics of hot dense matter”. In: *High Energy Density Physics* 3.1 (2007), pp. 57–64.
- [5] H Carter Edwards, Christian R Trott, and Daniel Sunderland. “Kokkos: Enabling manycore performance portability through polymorphic memory access patterns”. In: *Journal of Parallel and Distributed Computing* 74.12 (2014), pp. 3202–3216.
- [6] Eric J. Fluhr, Joshua Friedrich, Daniel Dreps, Victor Zyuban, Gregory Still, Christopher Gonzalez, Asha Hall, David Hogenmiller, Frank Malignoglio, Ryan Nett, Jose Paredes, Juergen Pille, Donald Plass, Ruchir Puri, Phillip Restle, David Shan, Kevin Stawiasz, Zeynep Toprak Deniz, Dieter Wendel, and Matt Ziegler. “5.1 POWER8 TM: A 12-core server-class processor in 22nm SOI with 7.6 Tb/s off-chip bandwidth”. In: *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*. IEEE. 2014, pp. 96–97.
- [7] Denis Foley. “NVLink, Pascal and Stacked Memory: Feeding the Appetite for Big Data”. In: *Nvidia.com* (2014).
- [8] Roger W Hockney and James W Eastwood. *Computer simulation using particles*. CRC Press, 1988.
- [9] R Hornung and J Keasler. “The RAJA portability layer: overview and status”. In: *Lawrence Livermore National Laboratory, Livermore, USA* (2014).
- [10] Intel. *Intel Xeon Processor E5-2698 v3 Specification*. http://ark.intel.com/de/products/81060/Intel-Xeon-Processor-E5-2698-v3-40M-Cache-2_30-GHz. [Online; accessed April 11, 2016].
- [11] Mauricio Faria de Oliveira. *NVIDIA CUDA on IBM POWER8: Technical overview, software installation, and application development*.
- [12] NVIDIA. *Tesla K80 GPU Accelerator Board Specification*. <http://images.nvidia.com/content/pdf/kepler/Tesla-K80-BoardSpec-07317-001-v05.pdf>. [Online; accessed April 11, 2016].

- [13] Oak Ridge National Laboratory. *Summit. Scale new heights. Discover new solutions. Oak Ridge National Laboratory's next High Performance Supercomputer*. <https://www.olcf.ornl.gov/summit/>. [Online; accessed April 10, 2016].
- [14] Oliver Kowalke. *boost.fiber*. <https://github.com/olk/boost-fiber>. [Online; accessed April 12, 2016].
- [15] OpenMP. *OpenMP application program interface version 4.0*. 2013.
- [16] René Widera. *cupla - C++ User interface for the Platform independent Library Alpaka*. <https://github.com/ComputationalRadiationPhysics/cupla>. [Online; accessed March 14, 2016].
- [17] John E. Stone, David Gohara, and Guochun Shi. “OpenCL: A parallel programming standard for heterogeneous computing systems”. In: *Computing in science & engineering* 12.1-3 (2010), pp. 66–73.
- [18] René Widera, Benjamin Worpitz, Erik Zenker, Axel Hübl, Guido Juckeland, Andreas Knüpfer, Wolfgang E. Nagel, and Michael Bussmann. *PI-ConGPU, Alpaka, and cupla software bundle for IWOPH 2016 submission*. May 2016. DOI: 10.5281/zenodo.53761. URL: <http://dx.doi.org/10.5281/zenodo.53761>.
- [19] Karl Zeil, Josefine Metzkes, Thomas Kluge, Michael Bussmann, Thomas E. Cowan, Stephan. D. Kraft, Roland Sauerbrey, and Ulrich Schramm. “Direct observation of prompt pre-thermal laser ion sheath acceleration”. In: *Nature communications* 3 (2012), p. 874.
- [20] Erik Zenker, Benjamin Worpitz, René Widera, Axel Huebl, Guido Juckeland, Andreas Knüpfer, Wolfgang E. Nagel, and Michael Bussmann. “Alpaka—An Abstraction Library for Parallel Kernel Acceleration”. In: *Accepted for publication on the IEEE International Parallel and Distributed Processing Symposium* (2016).