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Applied Reconfigurable Computing

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Preface

Reconfigurable computing technologies offer the promise of substantial performance gains over traditional architectures via customizing, even at runtime, the topology of the underlying architecture to match the specific needs of a given application. Contemporary adaptive systems allow for the definition of architectures with functional and storage units that match in function, bit-width, and control structures the specific needs of a given computation. They aim to exploit these novel and innovative resources to achieve the highest possible performance and energy efficiency.

Many are the challenges faced by reconfigurable computing in these days: design methods and tools, which include high-level languages and compilation, simulation and synthesis, estimation techniques, design space exploration, and run-time systems and virtualization; architectures, which may be self-adaptive and evolvable, heterogeneous, low-power, approximate, fine/coarse grained, embedded in an MPSOC and use an NOC, or even resilient and fault tolerant; applications that comprise security and cryptography, big data and HPC, embedded and DSP, robotics and automotive, mission critical, among many others; and trends in teaching, benchmarks, and other emerging technologies.

Over the past 12 years, the International Applied Reconfigurable Computing (ARC) Symposium series (www.arc-symposium.org) has provided a forum for dissemination and discussion of this transformative research area. The ARC symposium was first held in 2005 in Algarve, Portugal. The second edition took place in Delft, The Netherlands, in 2006, and was the first edition to have its proceedings published by Springer as a volume in its *Lecture Notes in Computer Science* series. Subsequent ARC yearly editions were held in Rio de Janeiro, Brazil (2007); London, UK (2008); Karlsruhe, Germany (2009); Bangkok, Thailand (2010); Belfast, UK (2011); Hong Kong, China (2012); Los Angeles, USA (2013); Algarve, Portugal (2014); Bochum, Germany (2015); Rio de Janeiro, Brazil (2016).

This LNCS volume includes the papers selected for the 13th edition of the symposium (ARC 2017), held in Delft, The Netherlands, during April 3–7, 2017. The symposium succeeded in attracting a significant number of high-quality contributions related to reconfigurable computing. A total of 49 papers were submitted to the symposium from 22 countries: Algeria (1), Brazil (5), Canada (1), China (9), Denmark (1), France (3), Germany (7), Greece (1), India (1), Iran(1), Italy(1), Japan (2), South Korea (1), Malaysia (1), The Netherlands (2), Pakistan (1), Poland (2), Singapore (2), Switzerland (1), Turkey (1), UK (4), and USA (1). All submissions were carefully evaluated by at least three members of the Program Committee. In all, 17 papers were accepted as full papers (acceptance rate of 34.7%) and 11 as short papers (global acceptance rate of 57.1%). The accepted papers composed a very interesting symposium program, which we consider to constitute a representative overview of ongoing research efforts in reconfigurable computing.

We would like to acknowledge the support of all the members of this year's Steering and Program Committees in reviewing papers, in helping with the paper selection, and in giving valuable suggestions. Special thanks also to the additional researchers who contributed to the reviewing process, to all the authors who submitted papers to the symposium, and to all the symposium attendees.

Last but not least, we are especially indebted to Juergen Becker from the University of Karlsruhe and to Alfred Hoffmann and Anna Kramer from Springer for their support and work in publishing this book as part of the LNCS series.

February 2017

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Invited Talks

Rethinking Memory System Design (and the Computing Platforms We Design Around It)

Onur Mutlu

ETH Zurich, Zurich, Switzerland

Abstract. The memory system is a fundamental performance and energy bottleneck in almost all computing systems. Recent system design, application, and technology trends that require more capacity, bandwidth, efficiency, and predictability out of the memory system make it an even more important system bottleneck. At the same time, DRAM and flash technologies are experiencing difficult technology scaling challenges that make the maintenance and enhancement of their capacity, energy efficiency, and reliability significantly more costly with conventional techniques. In fact, recent reliability issues with DRAM, such as the RowHammer problem, are already threatening system security and predictability. In this talk, we first discuss major challenges facing modern memory systems in the presence of greatly increasing demand for data and its fast analysis. We then examine some promising research and design directions to overcome these challenges and thus enable scalable memory systems for the future. We discuss three key solution directions: (1) enabling new memory architectures, functions, interfaces, and better integration of memory and the rest of the system, (2) designing a memory system that intelligently employs emerging non-volatile memory (NVM) technologies and coordinates memory and storage management, (3) reducing memory interference and providing predictable performance to applications sharing the memory system. If time permits, we will also touch upon our ongoing related work in combating scaling challenges of NAND flash memory. An accompanying paper, slightly outdated (circa 2015), can be found at http://people.inf.ethz.ch/omutlu/pub/memory-systems-research_superfri14.pdf.

Acceleration Through Hardware Multithreading

Walid Najjar

Department of Computer Science and Engineering,
University of California Riverside, Riverside, USA

Abstract. Long memory latencies, as measured in CPU clock cycles, is probably the most daunting challenge to modern computer architecture. In multicore designs, the long memory latency is mitigated with the use of massive cache hierarchies. This solution pre-supposes some forms of temporal or spatial localities. Irregular applications, by their very nature, suffer from poor data locality that results in high cache miss rates and long off-chip memory latency. Latency masking multithreading, where threads relinquish control after issuing a memory request, has been demonstrated as an effective approach to achieving a higher throughput. Multithreaded CPUs are designed for a fixed maximum number of threads tailored for an average application. FPGAs, however, can be customized to specific applications. Their massive parallelism is well-known, and ideally suited to dynamically manage hundreds, or thousands, of threads. Multithreading, in essence, trades off memory bandwidth for latency. In this talk I describe how latency masking multithreaded execution on FPGAs can achieve a higher throughput than CPUs and/or GPUs on two sets of applications: sparse linear algebra and database operations.

Enabling Software Engineers to Program Heterogeneous, Reconfigurable SoCs

Patrick Lysaght

Xilinx Research Labs, San Jose, USA

Abstract. In this talk, modern software trends will be explored with a focus on how we can enable software developers to exploit the benefits of reconfigurable hardware. This talk introduces PYNQ, a new open-source framework for designing with Xilinx Zynq devices, a class of All Programmable Systems on Chip (APSoCs) which integrates multiple processors and Field Programmable Gate Arrays (FPGAs) into single integrated circuits. The main goal of the framework is to make it easier for designers of embedded systems to use APSoCs in their applications. The APSoC is programmed in Python and the code is developed and tested directly on the embedded system. The programmable logic circuits are imported as hardware libraries and programmed through their APIs, in essentially the same way that software libraries are imported and programmed. The framework combines three main elements:

- The use of a high-level productivity language, Python in this case
- Python-callable hardware libraries based on FPGA overlays
- A web-based architecture incorporating the open-source Jupyter Notebook infrastructure served from Zynq's embedded processors

The result is a programming environment that is web-centric so it can be accessed from any browser on any computing platform or operating system. It enables software programmers to work at higher levels of design abstraction and to re-use both software and hardware libraries for reconfigurable computing. The framework is inherently extensible and integrates coherently with hardware-dependent code written in C and C++. The talk concludes with an outline of areas for continued development, and a call for community participation.

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