# Verification of Component Fault Trees using Error Effect Simulations

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Abstract. The growing complexity of safety-relevant systems causes an increasing effort for safety assurance. The reduction of development costs and time-to-market, while guaranteeing safe operation, is therefore a major challenge. In order to enable efficient safety assessment of complex architectures, we present an approach, which combines deductive safety analyses, in form of Component Fault Trees (CFTs), with an Error Effect Simulation (EES) for sanity checks. Both CFTs and the EES provide a modular, reusable and compositional safety analysis. The combination reduces the drawbacks of both analyses, such as the subjective failure propagation assumptions in the CFTs or the determination of relevant fault scenarios for the EES. Since both are applicable throughout the whole design process, they support continuous model refinement and the reuse of conducted safety analysis and simulation models. Hence, safety goal violations can be identified in early design stages and the reuse of conducted safety analyses reduces the overhead for safety assessment.

# 1 Introduction

The growing number and complexity of safety-relevant embedded systems poses new challenges, in many application domains such as the automotive domain with the rapidly evolving advance driver assistance systems. Along with the growing system complexity, also the need for safety assessment and its associated effort is drastically increasing. Safety assessment is a mandatory part in order to guarantee the high quality demands, imposed by the market. However, this is contrary to industry's aim to reduce costs and time-to-market.

In different application domains, safety standards, such as the IEC 61508 [10] or its automotive adaption ISO 26262 [11] define the safety assurance process. The goal of the safety assessment process is to identify all failures that cause hazardous situations and to demonstrate that their probabilities are sufficiently low. Traditionally, the analysis of systems in terms of safety consists of bottom-up safety analysis approaches, such as *Failure Mode and Effect Analysis (FMEA)*,

and top-down ones, such as *Fault Tree Analysis (FTA)*. Both provide structured procedure models to identify failure modes, failure causes and the effects on the system safety goals. The early identification of safety goal violations is crucial for a cost-efficient development process.

The quality of the safety assessment strongly depends on the correctness and completeness of the safety analysis model, describing the failure propagation and its transformation through the system. In current industrial practice, the quality of the safety analysis models in terms of completeness and correctness needs to be guaranteed manually by model reviews, which are very time-consuming tasks. Since such reviews are required after the initial construction of the safety analysis model as well as after each modification, the effort for maintaining its quality during the whole design time is significant. Applying a development strategy with frequent changes, such as agile methods, drastically increases this maintenance effort, endangering the success of the development.

Since system-level simulations enable the simultaneous analysis of software and digital/analog hardware, the application of simulations for safety evaluations attracted growing attention [2–4, 14–17]. However, the focus of most of these approaches is either the verification of fault tolerance mechanisms or the identification of failure modes as well as their effects. The determination of the analyzed fault space, as well as the integration in the still required safety assessment process is neglected. The main contribution of this paper is the synergistic combination of both methodologies. We present an approach for the verification of a failure propagation specification in form of a *Component Fault Tree (CFT)* methodology [12] with a *Error Effect Simulation (EES)* approach. Test cases are automatically generated from CFTs, which serve as input to inject faults into a system simulation. Additionally a test oracle, for failure effect detection, is created automatically. Thus, it is possible to discover gaps and errors in the failure propagation specification. This increases the quality while simultaneously reduces the effort for the manual safety model review drastically.

Since system simulations can be performed at different levels of granularity and CFT elements can be reused in different contexts, our approach is applicable throughout the design process. Hence, iterative and agile development strategies are supported by speeding up the analysis of the current system design abstraction. Thereby, only the refined parts of the system must be modified.

The paper is organized as follows: In Sect. 2 relevant related work is briefly summarized. The Sect. 3 presents the underlying method. The concept of CFTs is presented in Sect. 4. The EES infrastructure is presented in Sect. 5. The Sect. 6 outlines how test cases can be automatically generated from CFTs as input for the EES in order to review the safety analysis model. In Sect. 7 the benefits of our approach are demonstrated. The paper is concluded in Sect. 8.

#### 2 Related Work

As already mentioned, there exist manifold approaches that utilize simulationbased fault injection (SFI), such as [2–4, 14–17]. These approaches use system simulations combined with fault injection for enhancing safety analyses. They focus on the efficient execution of the fault injection and the determination of error effects. Randomly generated parameters are used in a large number of simulation runs. But in order to get meaningful results which can be used as evidence in a safety case, the number of test runs must be extremely high. And still these approaches cannot guarantee that all relevant faults are injected into the simulation. Additionally, previous approaches are missing a methodology to combine the presented techniques with established safety assessment processes which are still required for system qualification/certification. SFI mitigates the new challenges, but cannot replace safety assessments such as FTA or FMEA.

Such an FMEA integration is presented in [6]. It presents a simulationassisted FMEA by formalizing the FMEA structure and deriving a system simulation. With the help of such an approach, the fault catalogues used during FMEA are reused by the SFI. We utilize a similar approach for FTA, by mapping the FTA components to simulation components of a SFI. By provision of both a component-based FTA and a component-based SFI the concept of reusable databases is extended to reusable safety analysis artifacts.

The formalization of the FTA and the SFI structure are realized with the UML. Approaches such as [5,20] are also using the UML to support safety assessment. [5] provides a model-to-model transformation to map a UML specification to a executable model based on the *Action Language for Foundational UML*. However, the derivation or construction of FMEA tables are neglected.

In [13] Simulink-based simulation models are generated based on an EAST-ADL description of the system. Safety analysis is explicitly targeted by this approach, but it cannot be used to verify safety analysis. Similar to other SFI approaches, it is not described how input for the fault injection is generated.

### 3 Methodology

The goal of the safety assessment process is to identify all failures that cause hazardous situations and to demonstrate that their probabilities are sufficiently low. In the application domains of safety-relevant systems, the safety assurance process is defined by the means of safety standards (e.g. IEC 61508 [10]). Fig. 1 illustrates typical activities and their relation to the development process. Moreover, it outlines the used models and their interactions. As a first step, all relevant hazards of the system are identified and the associated risks are assessed during the so-called Hazard Analysis and Risk Assessment. Top-level safety requirements are the result of this step. Based on the system requirements the architecture of the system is designed in a model-based way using UML. Based on this system specification, the safety engineer is developing a safety analysis to identify failure modes, their causes, and effects with impact on the system safety. The results of the safety analysis as well as results of verification activities are used as evidences to evolve safety requirements to a safety case. Finally, the system safety is assessed based on the safety case and a certificate is issued in case of a positive assessment result.

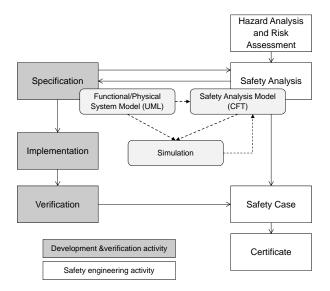


Fig. 1. Overview over the proposed methodology to verify safety analysis models

In our approach, we use the CFT methodology as a model- and componentbased approach for fault tree analyses to enable modular and compositional safety analysis. Thereby, fault tree elements are related to their development artifacts (defined in UML) and can be reused along with them. Based on the available system specification in UML a system level simulation can be generated automatically. Since safety artifacts are associated with design artifacts of the system architecture, a straightforward mapping between the entities in the generated system simulation and the safety analysis model is given. Hence, test cases with fault injection and test oracles are automatically generated from CFTs. This way it possible to check whether the specified failure propagation is correct, using the system-level simulation. This enhances the quality of the CFT-based safety analysis model in terms of correctness, since failure modes as well as failure mitigation mechanisms can be discovered which the safety engineer overlooked. Moreover, failure propagation paths, which are not yet know, e.g. caused by emergent behavior on system level, can be discovered.

### 4 Component Fault Trees

Component Fault Trees are Boolean models associated with system development elements such as components [8, 12, 22]. It has the same expressive power as classic fault trees, which are described in [19]. Like classic fault trees, CFTs are used to model failure behavior of safety-relevant systems. This failure behavior, including their appearance rate, is used to document the absence of unreasonable risk of the overall system. In addition, it can also be used to identify drawbacks of the design of a system. In CFT methodology, a separate CFT element is related to a component, e.g. defined in UML [7].

Let the System Sys consist of a set of components  $C = \{c_1, ..., c_n\}$ . Each component  $c_i \in C$  has a set of inports  $IN(c_i) = \{in_1, ..., in_p\}$  and a set of outports  $OUT(c_i) = \{out_1, ..., out_q\}$ . The information flow between the outport of a component  $c_i \in C$  and the inport of another component  $c_j \in C$  (with  $c_i \neq c_j$ ) is modelled by a set of connections  $CON = \{(out_x, in_y) | out_x \in OUT(c_i), in_y \in IN(c_j)\}$ .

If  $c_i \in C$  has a component fault tree element  $cft_i \in CFT$ , then it is  $C\tilde{F}T(c_i) = cft_i$  with  $cft_i \neq \emptyset$ . Thus, the CFT of the system Sys is defined by the set of CFT elements  $CFT = \{cft_1, ..., cft_n\}$ .

Failures that are visible at the outport of a component are modeled using Output Failure Modes  $OFM(out_l) = \{ofm_1, ..., ofm_t\}$  which are related to the specific outport  $out_l \in OUT(c_i)$ . To model how specific failures propagate from an inport of a component to the outport, Input Failure Modes  $IFM(in_k) = \{ifm_1, ..., ifm_s\}$  are used, which are related to an inport  $in_k \in IN(c_i)$ . The internal failure behavior that also influences the output failure modes is modeled using Boolean gates such as OR and AND as well as Basic Events. Basic Events  $B(cft_i) = \{b_1, ..., b_r\}$  represent failure modes that originate within a component. Each Basic Event can be assigned a failure rate, e.g. the Mean Time Between Failure (MTBF) or the Failure in Time (FIT). In case of an OR gate a failure propagates if at least one of the inputs is active, while an AND gate propagates failures only if all input failures are active.

A library, which contains CFT elements for all system components, eases the reusability of safety artifacts. Hence, it is possible to create different CFTs by just changing the assembly of the CFT elements. Every CFT can be transformed to a classic fault tree by removing the input and output failure mode elements.

### 5 Error Effect Simulation

The EES consists of a *Device Under Test (DUT)* and its test bench. The DUT models software, hardware and analog system parts. We use the IEEE standard SystemC [9] because of its support of various simulation domains and its comprehensive support of different abstraction levels. The EES uses an approach similar to [18]. It consists of a modular, parameterizable system simulation that is used to assess error effects. One simulation instance is assembled of parameterizable *Simulation Entities (SEs)*. To facilitate the analysis of different DUT characteristics, the framework uses dynamic configuration that is supplied during runtime. This covers the DUT architecture as well as the SEs parameterization.

The EES requires *fault injectors*, which cause a discrepancy within the DUT. We provide injection capability by replacing simulation primitives with an injectable container that encapsulates the original simulation primitive. This container provides an interface to change the value of the simulation primitive. The design of the injectors is particularly suited to support simulation models of different abstraction levels with their different modeling primitives. A centralized injection control module stimulates the safety case by controlling the injectors. The so-called Behavioral Threat Models (BTM) specifies the injected behavior. A BTM is based on Timed Automata (TA). A TA consists of a finite set of locations L, actions  $\Sigma$  and a set of clocks C, which can be reset individually. An edge  $(l_i, \sigma, g(C), r(C), l_j) \in E$  is a transition from location  $l_i$  to location  $l_j$ with an action  $\sigma \in \Sigma$ , a time dependent guard g(C) and a clock reset r(C). For fault modeling the TA approach is extended in a way that guard statement  $g(C, \mathbb{W}_s, \mathbb{W}_l, \mathbb{E})$  can additionally depend on the state of the simulation  $\mathbb{W}_s$ , the state of BTM local variables  $\mathbb{W}_l$  and a set of events  $\mathbb{E}$  that are used to synchronize multiple BTMs. Actions  $\sigma(\mathbb{W}_s, \mathbb{W}_l)$  are extended to modify the simulation state  $\mathbb{W}_s$  or local variables within the BTM  $\mathbb{W}_l$ . The centralized injection control module interprets a BTM dynamically and stimulates faults.

For failure detection, the virtual prototype is extended with *failure monitors*, which compare the behavior of one variable with a previous simulation run. Using an error free simulation run as reference enables the detection of failures that are caused by the fault injection. Ref. [1] presents a general failure mode characterization, which cover *content failures*, *early failures*, *late failures*, *halt failures* as well as *erratic failures*. The proposed failure monitors detect these standard failure modes by default. Besides the detection of these standard failure modes it is possible to specify queries that are checked both on the reference and error trace. A *Computation Tree Logic (CTL)* expression specifies the queries. This enables the detection of application specific failure modes.

A graphical specification of the EES based on the UML supports the user by conducting analyses. It reduces the manual overhead by code generation steps and increase the usability by a graphical user interface. The graphical specification consists of the specification of the SEs, their instantiation, parametrization and interconnection. Moreover, the placement of fault injectors, failure monitors and fault behavior is specified.

With these extensions of the system simulation the question still remains, at which location to inject faults (fault injector placement), how does the injected behavior look like (BTM specification) and where to detect deviations from the reference trace (monitor placement).

### 6 Verification of CFTs using Error Effect Simulation

In order to verify the failure behavior specified as CFT, test cases for the EES are generated automatically. A test case covers the fault specification and the fault injector placement. Additionally it includes a test oracle, which is realized by a failure monitor. The test cases are derived from the CFT. For this purposes, we define a so-called *scope* S of the CFT that involves only a certain amount of the components with  $S \subseteq CFT$ . Thus, it is possible to verify both the entire failure propagation model as well as only a part of it. A scope  $S \subseteq CFT$  provides a set of inputs and outputs. The inputs of the scope  $IN_S \subseteq \bigcup_{c_i \in S} IN(c_i)$  are used to enter a test scenario. The outputs  $OUT_S \subseteq \bigcup_{c_i \in S} OUT(c_i)$  are used to measure the results of a test scenario. The inner CFT logic can be simplified to a CFT element for the scope S, which only contains the gates and basic events, input

and output failure modes that are related to the scope (cf. Ref. [21]). Internal input and output failure modes are omitted. Hence, for a scope  $S \subseteq CFT$ , the CFT element related to S is  $CFT_S \subseteq CFT$ . It contains failure modes related to the inports and outports and have a connection outside of the scope. Let

$$IFM(S) = \{ in \mid \exists (a,b) \in CON, a \in OUT(A), A \notin S, \\ b \in IN(B), B \in S, in \in IFM(B) \}$$

be the input failure modes of the scope S and

$$OFM(S) = \{out \mid \exists (a,b) \in CON, a \in OUT(A), A \in S, b \in IN(B), B \notin S, ut \in OFM(A)\}$$

be the output failure modes of the scope S. Moreover, let

$$B(S) = \bigcup_{c_i \in S} B(c_i)$$

be the set of basic events of the scope S.

In order to determine a set of test cases, we apply the methodology of *Minimal* Cut Set Analysis (MCA). A MCA is a representation of a tree using a disjunction of conjunctive terms that cannot be reduced further [19]. For a scope S, let

$$mc_i(t) = x_1 \land \ldots \land x_n, t \in OFM(S), x_i \in IFM(S) \cup B(S)$$

be all cut sets that result in the occurrence of the output failure mode  $t \in OFM(S)$  of the scope  $S \subseteq CFT$ . Moreover, let

$$MCA(t) = mc_1(t) \lor \ldots \lor mc_m(t), t \in OFM(S)$$

be the minimal cut set analysis of the output failure mode t and scope  $S \subseteq CFT$ . Since in general multiple combinations of input data leads to different output data for the same test case, typical measures can be applied here to further reduce the set of test cases like equivalence class testing.

Thus, the results of the MCA are used to generate input for the fault injectors. For each input failure mode  $ifm_i$  a set of BTMs is generated  $BTM(ifm_i) = \{btm_{i,1} \dots btm_{i,m}\}$  to control the fault injector at the inports  $IN_S$  of the respective component. Similar for each Basic Events  $b_i$  a set of BTMs is generated  $BTM(b_i) = \{btm_{i,1} \dots btm_{i,n}\}$  to inject faults by the modification of the component state. In this work, we use sets of predefined BTMs that match the failure behavior of the input failure modes and Basic Events within the CFT. An approach with a BTM-library is used and the generation process parametrizes these predefined fault behaviors. The generated inputs stimulate the DUT and will lead to a discrepancy from the intended behavior. Since the output failure modes OFM(S) of S can be observed at the outports  $OUT_S$ , failure monitors are placed within the EES. These monitors detect general failure modes. With this the the CFT can be verified by the EES.

## 7 Case study

We illustrate the benefits of our approach using an automotive case study namely a coasting assistant. This assistant calculates driver hints such as acceleration or braking with regard to an energy efficient driving strategy. The system is designed for electric vehicles, where in case of a deceleration the driver has the choice of freewheeling or braking with recuperation. The coasting assistant displays the optimal driving choice w.r.t. energy efficiency in the Head-Unit. Therefore, the coasting assistant ECU uses maps annotated with speed limits but also a video-based speed limit detection to adjust to undocumented limits such as road works. This speed limit detection will be the focus of the case study.

### 7.1 Overview

The coasting assistant functionality is distributed over multiple Electronic Control Units (ECUs) which are interconnected by different communication channels. Fig. 2 shows the involved ECUs and communication channels. The camera ECU records the road in front of the vehicle and sends this image to a circle detection algorithm using the synchronous channel of a MOST bus. In the next processing step circles are detected and the containing image segments are forwarded to a speed limit classification. The image segments are forwarded via the dynamic segment of the FlexRay bus. Information about the estimated distance of the potential speed sign is sent with a separate CAN message to the coasting assistant ECU. The cropped circles are classified and the results are sent to the coasting assistant via CAN. The coasting assistant uses the received information on the next speed limit as well as the estimated distance and an internal look-up table to calculate an energy efficient driving strategy.

Focus of the safety analysis in early development stages is the actual functionality itself. The communication between simulation entities is abstracted by function calls. The logical system architecture, specified with the CFT architectural model, is shown in Fig. 3. The data exchange is modeled using ports.

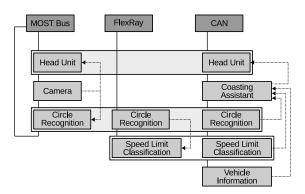


Fig. 2. Overview of the case study

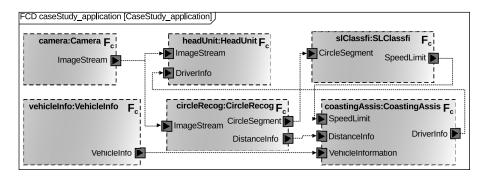


Fig. 3. Functional architecture of the exemplary system

### 7.2 CFT-based analysis

For each of the components within the system architecture a CFT element is specified. Fig. 4 (a) shows the CFT element describing the failure behavior of the camera ECU. The different internal failures are modeled by Basic Events. Each of them is associated with a specific failure rate. The CFT element of the camera specifies failure modes like a frozen image stream, a corruption of the image pixels, the omission of the complete images or a variation in the sampling time of the camera. These failure modes are propagated via the components' outports to other components. This way the failures originating from the camera induces the failure modes in the head unit and the Circle Detection ECU. Fig. 4 (b) shows the failure modes within the coasting assistant ECU. The input failure modes represent that a speed limit is reported too late that an erroneous speed limit is reported or that speed limit is missing. The output failure modes depend on the input failure modes and the Basic Events of the component. The output failure modes determine the input failure modes of the next component - in our case study the ones of the head unit.

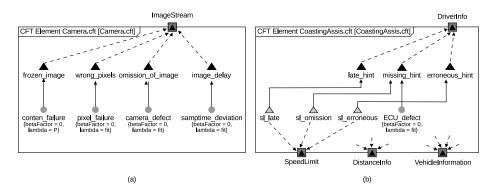


Fig. 4. Excerpt of failure modes within the camera (a) and coasting assistant (b)

With the specification of the CFT elements for all components of the system architecture it is possible to calculate the complete fault tree or different fault trees w.r.t. a restricted scope. Table 1 shows a few of the generated test cases with different scopes. One example fault tree path would be

Fault injection	Failure monitor
camera_defect	omission_of_image
content_failure	frozen_image
sl_omission OR di_omission OR	missing_hint
ECU_defect	
sl_errornous	erroneous_hint
camera.content_failure OR cam-	$coastingAssis.erroneous\_hint$
era.pixel_failure	
camera.content_failure OR cam-	HMI.image_content_failure
era.pixel_failure	
$camera.samptime\_deviation$	HMI.sl_late
	camera_defect content_failure sl_omission OR di_omission OR ECU_defect sl_errornous camera.content_failure OR cam- era.pixel_failure camera.content_failure OR cam- era.pixel_failure

Table 1. Excerpt of the generated test cases

that camera.content\_failure OR camera.pixel\_failure can cause the failure mode coastingAssis.erroneous\_hint, when the HMI is excluded from the analyzed scope.

### 7.3 Simulation-based verification

After generation of the relation between input failure modes and output failure modes, these relations are verified using simulations. The EES shows if the caused-by-relation specified in the safety analysis model is observed in the simulation. In case of OR-relations the simulation has to provoke an error effect if any of the faults is injected. In case of an AND-relation the error effect should only manifest if all input faults are injected simultaneous. For each component in the CFT a corresponding SE exists in the simulation. Fig. 5 shows the graphical specification of the simulation configuration. It contains the same components as the CFT system architecture and for each of the components a CFT element is specified. Model-to-model transformations enable the mapping of CFT elements to simulation components. The simulation specification contains additional information that is not specified within the CFT system architecture or the CFT, such as the SE parametrizations or the SEs of the test bench. Thus, it is no bijective transformation. In the context of this work the developer is supported by automated model-to-model transformations, but still manual extensions, e.g. to specify the component parametrization or to extend the configuration with sole simulation components, are required to create the simulation. This approach offers the benefit that the system architecture or the CFT is not polluted with information which is only required for the simulation.

The fault injection targets mainly the internal information of the components. The failure modes specified in the CFT element of the Camera (cf. Fig. 4) target

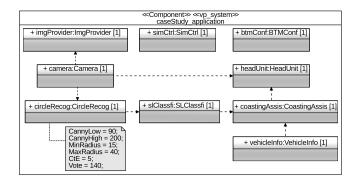


Fig. 5. Specification of the system simulation for the case study

the internal storage of the transmitted image. The failure mode frozen\_image is represented by altering the sampling time of the camera, the wrong\_pixels fault by altering the image payload. A camera defect (omission\_of\_image) is modeled by an infinite sampling time. If two failure modes are affecting the same injector, e.g. the camera defect and the frozen image, the user have to assure the interaction between the two failures modes is desired. The simulation contains therefore fault injectors that are associated with the payload array and with the sampling time variable. Fig. 6 (above) shows the BTMs to inject a pixel failure and Fig. 6 (below) shows the behavior of the content failure. It

```
<ESname> eInit <EStype> initial
1
   <ESname> eFree
2
3
   <ESname> eState
4
   <ETsrc> eInit <ETtgt> eFree
     <ETaction> ids = [id for id in range(719*200,719*210)]
\mathbf{5}
   <ETsrc> eFree <ETtgt> eState
6
      <ETguard> BTMclock('OKTime').read()==sc_time(23, sc_time_unit.SC_SEC)
7
      <ETaction> [VPvar('m_Camera.pixel')[id].force(0x00) for id in ids]
8
9
   <ETsrc> eState <ETtgt> eState
      <ETaction> [VPvar('m_Camera.pixel')[id].release() for id in ids];
10
                 [VPvar('m_Camera.pixel')[id].force(0x00) for id in ids]
11
```

Fig. 6. BTM for image corruption (above) and a freeze frame failure (below)

can be seen that both BTMs control the injector VPvar('m\_Camera.pixel'). In the context of the CFT the different failure modes determine the selection of the BTMs  $(BTM(ifm_i) \text{ or } BTM(bi))$ . In this case study, for each input failure



Fig. 7. Effect of different pixel corruption strategies

mode or Basic Event in the CFT a set of BTM are created. For instance, the BTM in Fig. 6 (below) is generated for the camera.content\_failure solely. For the camera.pixel\_failure different BTMs that stimulate different corruption patterns are created. Fig. 7 illustrates three effects of the generated BTMs. The picture on the left shows the pixel corruption limited to a horizontal line, the middle one to a vertical line and the picture on the right shows a random pixel corruption over the complete image.

Each output failure mode within the CFT is presented in the simulation by a monitor. In this case study a monitor is added at the received speed limit in the coasting assistant, corresponding to the output failure mode specified in the CFT element of the coasting assistant. Before each simulation with fault injection a reference trace is generated without fault injection. Based on this generated reference trace the monitors classify the current trace, caused by the fault injection.

In this example the traces indicate a late failure. The reference trace reports a speed limit at 28.8 seconds but the injection trace first at 29.1 seconds. This is based on the fact that the speed sign is recorded in sequence of images, while the vehicle drives towards the sign, and that the first classifications is prevented based on the pixel corruption within the image. In this fault scenario the horizontal line is injected, blocking the speed limits far away. This situation was overseen during the creation of the CFT. As mentioned earlier a camera.content\_failure OR camera.pixel\_failure can cause the failure mode coastingAssis.erroneous\_hint. The simulation has shown that this is a very unlikely case, because the classification will most likely return no classification at all instead of the wrong classification. Resulting in a late failure mode because a sequence of images is taken from the actual speed limit sign and most likely a subsequent image will be classified correctly. The nearer the speed limit the more robust is the classification against pixel errors. Subsequent to the EES the CFT, particularly the classification component, is adjusted in a way that the classification.erroneous\_circle\_recognition input failure additionally causes classification.speed-limit\_information-too-late output failures. This case is a very good example how the none-complete simulation approach and the deductive safety analysis in form of a CFT complement each other. A very large number of simulation runs would be necessary to reproduce the behavior of corrupted speed limit information within the coasting assistant based on a pixel corruption in the camera. Therefore, the safety analyst can specify this case manually in the fault tree after verifying the CFT using an EES. On the other hand when solely using the top-down safety analysis (in form of a CFT), the safety experts could have missed the propagation of a pixel corruption to a late speed limit failure mode.

Besides the verification of existing failure propagation paths within the CFT it is also possible to verify if failure propagation exists that are not represented in the CFT. Therefore, the input failure modes and Basic Events, respectively the generated fault behavior, are combined with different output failure modes, respectively their failure monitors. Thus, missing propagation paths within the CFT can be revealed using the EES. With increasing complexity of safety analysis models the effort to verify all combinations of fault injection and monitors is rapidly increasing. One benefit of our approach is that different failure monitors can be used within one simulation run in order to examine different failure propagation paths at once.

#### 7.4 Analyses refinement

In later stages of the design process the models will be refined. In this case study only the communication between the components is refined. In a first refinement step, the communication is mapped to abstract transaction models and in a second step to detailed bus models of CAN, FlexRay and MOST. With each more detailed abstraction level, new failure sources are added and the CFT is extended with CFT elements of the corresponding components. This will enable more detailed safety analyses of the system. On the other hand the already verified CFTs and simulation models of the application are reused with each refinement step. This is an example of the benefit of using a modular, compositional approach for the safety analysis and the simulation.

Another benefit is the reuse of components (CFT, EES) within a single system configuration. For example the models of the transaction-based communication are required at different locations of the system. Through a single CFT- and simulation-element it is possible to create multiple instances. This way the effort is reduced and the failures are automatically applied at different system parts.

#### 8 Summary

The presented approach enables the verification of failure propagation models in form of Component Fault Trees (CFT) by an Error Effect Simulations (EES). Automatic generation steps are provided to generate the injected fault behavior, required for the EES, as well as a test oracle to classify the monitored failure behavior. It is shown how the verification of the safety analysis model is applied during different phases of the development process. In particular, after each change of the system design, including modifications or refinements of the system architecture. Since the inputs of the fault injection as well as the test oracle are generated automatically, the repeated verification of the failure propagation model can be performed efficiently. Supporting a safety analysis technique, like CFT, with a non-complete simulationbased analysis reduces the weaknesses of both methodologies. The results of the CFT-based analysis are only as good as the system knowledge of the involved experts. Especially, the safety analysis model of large-scale, complex systems might be incomplete. The system simulation on the other hand offers a method to enable different stakeholders, in particular IP providers, to contribute their system knowledge. Such simulation models offer a good basis to support safety analysis, since they enable a quantitative assessment of failure mitigation mechanisms. On the other hand, only selective use cases are analyzed and the detailed assessment of failure rates can cause a huge simulation effort. By the automatic generation of fault injection input and test oracles for the simulation from the CFT these weaknesses are reduced. Hence, our approach enables the verification whether the specified failure propagation is defined correctly within a CFT-based safety analysis model. Moreover, additional failures on system level as well as additional failure mitigation mechanisms can be discovered. It is also possible to discover failure propagation paths, which are not yet know. Another benefit is that in most cases the simulation doesn't have to be executed with a random fault injection based on very small failure rates. Firm fault combinations are injected and the propagation is evaluated by the EES. The probabilistic analyses is then executed on the verified CFTs, reducing the simulation effort drastically.

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