Symbolic Parallelization of Nested Loop Programs

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Contents

Acronyms

ABS	Anti-lock Breaking System
AG	Address Generator
AST	Abstract Syntax Tree
CGRA	Coarse-Grained Reconfigurable Array
COTS	Commercial Off-The-Shelf
CPU	Central Processing Unit
CUDA	Compute Unified Device Architecture
DMR	Dual Modular Redundancy
DPLA	Dynamic Piecewise Linear Algorithm
ECC	Error-correcting Code
EDC	Egregious Data Corruptiony
EDL	Error Detection Latency
FCR	Fault Containment Region
FSM	Finite State Machine
FU	Functional Unit
GC	Global Controller
GPU	Graphics Processing Unit
HPC	High-Performance Computing
*i*Ctrl	Invasion Controller
i-let	Invasive-let
ILP	Integer Linear Program
IM	Invasion Manager
i-NoC	Invasive Network-on-Chip
LPGS	Locally Parallel Globally Sequential
LSGP	Locally Sequential Globally Parallel
MPSoC	Multi-Processor System-on-Chip
NMR	N-Modular Redundancy

PE	Processing Element
PFH	Probability of Failure per Hour
PGAS	Partitioned Global Address Space
PLA	Piecewise Linear Algorithm
SER	Soft Error Rate
SEU	Single-Event Upset
SIL	Safety Integrity Level
SoC	System-on-Chip
SPARC	Scalable Processor Architecture
TCPA	Tightly Coupled Processor Array
TMR	Triple Modular Redundancy
UDA	Uniform Dependence Algorithm
VLIW	Very Long Instruction Word

List of Symbols