

Computer Communications and Networks

Series editors

Jacek Rak, Department of Computer Communications, Faculty of Electronics, Telecommunications and Informatics, Gdansk University of Technology, Gdansk, Poland

A. J. Sammes, Cyber Security Centre, Faculty of Technology, De Montford University, Leicester, UK

The **Computer Communications and Networks** series is a range of textbooks, monographs and handbooks. It sets out to provide students, researchers, and non-specialists alike with a sure grounding in current knowledge, together with comprehensible access to the latest developments in computer communications and networking.

Emphasis is placed on clear and explanatory styles that support a tutorial approach, so that even the most complex of topics is presented in a lucid and intelligible manner.

More information about this series at <http://www.springer.com/series/4198>

Mohsen Jahanshahi · Fathollah Bistouni

Crossbar-Based Interconnection Networks

Blocking, Scalability, and Reliability



Springer

Mohsen Jahanshahi
Department of Computer Engineering,
Central Tehran Branch
Islamic Azad University
Tehran
Iran

Fathollah Bistouni
Department of Computer Engineering,
Central Tehran Branch
Islamic Azad University
Tehran
Iran

ISSN 1617-7975 ISSN 2197-8433 (electronic)
Computer Communications and Networks
ISBN 978-3-319-78472-4 ISBN 978-3-319-78473-1 (eBook)
<https://doi.org/10.1007/978-3-319-78473-1>

Library of Congress Control Number: 2018935863

© Springer International Publishing AG, part of Springer Nature 2018

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, express or implied, with respect to the material contained herein or for any errors or omissions that may have been made. The publisher remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Printed on acid-free paper

This Springer imprint is published by the registered company Springer International Publishing AG
part of Springer Nature

The registered company address is: Gwerbestrasse 11, 6330 Cham, Switzerland

Preface

Interconnection networks are used in multiprocessor systems in order to establish the connection between the various nodes such as processors and memory modules. Blocking problem has always been considered as one of the most challenging issues in these networks, which degrades network performance and consequently the performance of the whole system. In the meantime, the main option for dealing with this problem is the use of non-blocking crossbar networks. However, there are engineering and scaling difficulties to use these networks in large-scale systems; the number of pins on a VLSI chip cannot exceed a few hundreds, which restricts the size of the largest crossbar that should be integrated into a single VLSI chip. However, there is a reasonable solution to the exploitation of the crossbar network in large-scale systems. The solution is using small-size crossbar networks as building blocks for larger network sizes. So far, this idea has led to a variety of topologies designed to meet the problems of blocking and scalability. Therefore, having the knowledge of different types of these crossbar-based networks and their strengths and weaknesses is essential in the design and selection of efficient interconnection networks.

Based on the above discussions, the focus of this book is on the *Crossbar-Based Interconnection Networks* to provide different perspectives required to recognize these momentous networks. This book consists of the following chapters:

Chapter 1 (Introduction): This chapter contains some introductory information for understanding the role of interconnection networks in multiprocessor systems, blocking problem, crossbar network and scalability problem, and existing solutions to address the scalability and blocking problems.

Chapter 2 (Interconnection Networks): This chapter presents a classification of interconnection networks and then attempts to provide the necessary information to recognize any of the networks.

Chapter 3 (Blocking Problem): This chapter is focused on the problem of blocking and analysis of different existing solutions to solve the problems of blocking and scalability.

Chapter 4 (*Fault-Tolerant Multistage Interconnection Networks*): Use of fault-tolerant multistage interconnection networks is a scalable solution to the blocking problem reduction. Therefore, this chapter analyzes a variety of different approaches to improve fault tolerance on multistage interconnection networks.

Chapter 5 (*Scalable Crossbar Network*): This chapter discusses the scalable crossbar network, which is a non-blocking interconnection network and uses small-size crossbar switches as switching elements.

Tehran, Iran

Mohsen Jahanshahi
Fathollah Bistouni

Contents

1	Introduction	1
1.1	High Computational Power	1
1.2	Interconnection Networks	2
1.3	Blocking Problem	4
1.4	Crossbar Network and Scalability Problem.	4
1.5	Solutions	6
	References	7
2	Interconnection Networks	9
2.1	Introduction	9
2.2	Classification of Interconnection Networks	10
2.3	Bus-Based Interconnection Networks	10
2.3.1	Single-Bus Network	12
2.3.2	Multiple-Bus Networks	12
2.3.3	Reliability Analysis	16
2.4	Switch-Based Interconnection Networks.	21
2.4.1	Crossbar Network	22
2.4.2	Single-Stage Network	23
2.4.3	Multistage Networks	25
2.4.4	Blocking in Multistage Interconnection Networks	29
2.5	Static Interconnection Networks	32
2.5.1	Completely Connected Networks	32
2.5.2	Limited Connection Networks	33
2.5.3	Cube Networks	34
2.5.4	Mesh Networks	36
	References	37
3	Blocking Problem	41
3.1	Introduction	41
3.2	Related Works	42

3.2.1	Construction of Scalable Non-crossbar Networks by Small-Size Crossbars	43
3.2.2	Construction of Scalable Crossbar Topologies by Small-Size Crossbars	53
	References	55
4	Fault-Tolerant Multistage Interconnection Networks	57
4.1	Introduction	57
4.2	Performance Analysis of Increasing the Number of Stages in Terms of Reliability	58
4.2.1	Structure of the SEN, SEN+, and SEN+2	58
4.2.2	Terminal Reliability of SEN, SEN+, and SEN+2	59
4.2.3	Broadcast Reliability of SEN, SEN+, and SEN+2	64
4.2.4	Network Reliability of SEN, SEN+, and SEN+2	67
4.3	Designing a Multistage Interconnection Network with Fault-Tolerant Capability	71
4.3.1	Related Works	71
4.3.2	Pars Network Structure	73
4.3.3	Proposed Routing Scheme for Pars Network	78
4.3.4	Performance Analysis	81
4.4	Improving the Reliability of the Benes Network	105
4.4.1	Different Methods for Improving Reliability in Benes Network	106
4.4.2	Reliability Analysis of EBN, PBN, and RBN Networks	109
	References	133
5	Scalable Crossbar Network	137
5.1	Introduction	137
5.2	Scalable Crossbar Network (SCN) Structure	138
5.3	Routing Scheme in SCN	140
5.4	The Analysis of Performance	143
5.4.1	Mathematical Analysis	144
5.4.2	Numerical Results	150
	References	161
	Index	163