

Intrinsic Evolution of Analog Circuits on a Programmable Analog Multiplexer Array

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Abstract. This work discusses an Evolvable Hardware (EHW) platform for the intrinsic evolution of analog electronic circuits. The EHW analog platform, named PAMA-NG (Programmable Analog Multiplexer Array-Next Generation), is a reconfigurable platform that consists of integrated circuits whose internal connections can be programmed by Evolutionary Computation techniques, such as Genetic Algorithms (GAs), to synthesize circuits. The PAMA-NG is classified as Field Programmable Analog Array (FPAA). FPAAs are reconfigurable devices that will become the building blocks of a forthcoming class of hardware, with the important features of self-adaptation and self-repairing, through automatic reconfiguration. The PAMA-NG platform architectural details, concepts and characteristics are discussed. Two case studies, with promising results, are described: a logarithmic amplifier and an S membership function circuit of a fuzzy logic controller.

1 Introduction

This work focuses on evolutionary design of analog circuits on a platform named PAMA-NG (Programmable Analog Multiplexer Array – Next Generation). Evolutionary Computation is applied to carry out the process of automatic circuit synthesis through a set of search algorithms, called Evolutionary Algorithms (EAs), which borrow from biological evolution their main principles. This particular area of research, where Evolutionary Algorithms are applied to electronic circuit synthesis, receives the name of Evolvable Hardware (EHW)[1].

The PAMA-NG platform is based on PAMA (Programmable Analog Multiplexer Array)[2]. PAMA-NG is classified as an FPAA [2][3][4] and supplies an environment to evolve generic analog circuits based on discrete components, without the need of simulators, i.e. intrinsic evolution. PAMA is a flexible platform with respect to granularity: its building blocks can be chosen by the designer, from transistors to high level analog components, such as operational amplifiers. PAMA-NG introduces new important features, such as protection against configurations that may damage

electronic components and the possibility of analyzing circuits that have been evolved, since it provides access to individual circuit elements.

A traditional Genetic Algorithm (GA) [5] drives PAMA's intrinsic evolution. In the evolutionary process, a population of chromosomes is randomly generated to represent a pool of circuit architectures. The chromosomes (control bit strings) are uploaded to the reconfigurable hardware. Circuit responses are compared to specifications of a target response and individuals are ranked in accordance with how close they satisfy the specifications. A new iteration loop involves generation of a new population from the pool of the individuals in the previous generation. Some individuals are taken as they are and some are modified by genetic operators, such as crossover and mutation. The process is repeated for a number of generations, resulting in increasingly better individuals. This process ends after a given number of generations or when the obtained result is close enough to the target response. In practice, one or several solutions may be found among the individuals of the last generation.

This paper is divided into three additional sections. Section 2 describes how PAMA-NG: internal interfaces and data flow are shown and the Reconfigurable Circuit implementation and purpose are described. Section 3 presents two case studies and section 4 concludes the paper.

2 PAMA-NG

The PAMA-NG evolutionary platform is an analog platform based on analog multiplexers, which are responsible for the interconnections of the different discrete components that can be plugged into the board. Figure 1 depicts PAMA-NG block diagram.

The platform performs intrinsic evolution of analog electronic circuits through a traditional GA. The chromosome configures the connection of the discrete components and each gene drives the select input signals of a particular analog multiplexer. As shown in Figure 1, a multifunction I/O board connected to the PC bus is responsible for A/D conversion and for chromosome upload. An eight-channel D/A converter allows for the application of different input values to the circuits being evolved, in order to perform the input/output mapping for fitness evaluation.

2.1 Reconfigurable Circuit

The Analog Reconfigurable Circuit (ARC) is divided into three layers: discrete components, analog multiplexers and analog bus (Figure 1). The designer chooses the components, from low-level discrete ones such as transistors, resistors and capacitors, to higher level circuits, such as operational amplifiers and comparators, or even more complex building blocks, such as multipliers and root mean-square circuits.

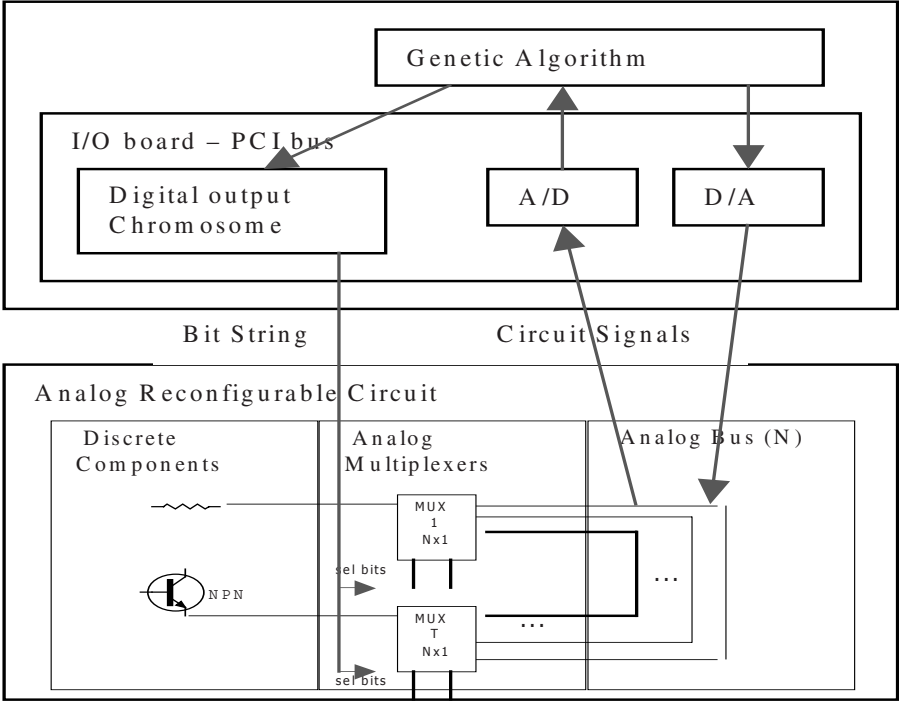


Fig. 1. The PAMA-NG platform block diagram

Each component terminal is connected to a specific line of an analog bus through an analog multiplexer. The chromosome bits, which are set by the GA running on the PC, select for each analog multiplexer a line of the analog bus to be connected to the component's terminal. Each line of the analog bus corresponds to one interconnection point of the circuit (node); some of them can be associated with external points, such as an input signal, power supply, ground and circuit output, while others can correspond to with internal points of interconnection.

The purpose of the ARC is to be generic, flexible and scalable. Discrete components can be of any type and in any number to fulfill application requirements. These components may be on sockets or on protoboard, making it easy to change them.

One ARC circuit module implements a 32 16-to-1 analog multiplexer. The low on-resistance (R_{on}) of 100 ohms of the analog multiplexers prevents the ARC from damage caused by potentially hazardous configurations during evolution. The search space associated to the platform is $16^{32} \sim 10^{38}$ (number of different possible solutions).

2.2 Important Issues

There are some important issues to discuss when analyzing an evolutionary platform, such as the circuit evaluation time, the platform's granularity and architecture and its protection against damaging configurations.

PAMA-NG presents a fast circuit evaluation time. Its multifunction I/O board starts the A/D conversion of the circuit's input and output signals immediately after the circuit's download to the platform. In tests, the period between two digital samples has been measured as 0.08ms.

The flexibility is another important feature. The optimal choice of the elementary block type and granularity is task dependent. PAMA-NG allows all discrete components to be selected by the designer, according to the application.

There are some other important characteristics that directly affect the evolution, such as the platform's protection against damaging configurations. In PAMA-NG, the parasitic resistances of the switches (R_{on}) provide this protection. Another desirable characteristic is that there are no architecture constraints, so that the evolution is allowed to exploit any interconnection pattern.

In view of the above, PAMA presents desirable characteristics when compared to other reconfigurable platforms designed to intrinsically evolve analog circuits [3][4]. Those characteristics have been contrasted in a previous work [6].

3 Case Studies

In the case studies, PAMA-NG is used to perform intrinsic evolution of analog circuits through a traditional GA with a chromosome length of 128 bits (32 mux times 4 select-inputs). In order to evolve the circuits, some steps have to be taken.

First, the discrete components have to be chosen. The platform has to be provided with a sufficient number of discrete components to be capable of achieving the desired circuit. The type of these components must be adequate. Since PAMA has originally a limited number of component terminals (32), its flexibility can be exploited to obtain higher level circuits, by using higher level building blocks as discrete components.

Next, the number of input and output signals must be assigned. The inputs and outputs of the circuit have to be connected to the multifunction I/O board.

Finally, a fitness measure has to be created. A precise function translates the output of the desired circuit. Experience has shown that the choice of an adequate fitness function plays a significant role in the evolution of an analog circuit.

The Genetic Algorithm used in the experiments has the following characteristics:

Binary Representation: 128 bits

Population Initialization: Random

Reproduction Technique: Steady State

Operators: One-point Crossover and Mutation

Fitness Technique: Exponential Normalization

In the fitness technique used – exponential normalization – probabilities of the ranked individuals are exponentially weighted [6] and are given by Equation (1).

$$p_i = \frac{c-1}{c^n-1} c^{n-i} \quad (1)$$

The closer c is to 1, the lower is the "exponentiality" of the selection method.

3.1 Logarithmic Amplifier

In a logarithmic amplifier the output is proportional to the logarithm of the input signal. In [7] the intrinsic evolution of a logarithmic amplifier with no gain has been reported. In that experiment the objective was to demonstrate the platform's flexibility with respect to granularity; coarse-grained components, such as operational amplifiers, were used. The discrete components were then chosen based on conventional configurations for logarithmic amplifiers and some connections were fixed.

Here a logarithmic amplifier with an amplification of two is presented. This evolution has no restrictions concerning the discrete components connections.

The following GA parameters are used:

Generations: 300

Population: 400

Crossover: 0.7

Mutation: 0.15

Steady State: 10

Exponential Normalization c parameter: 0.9

Evolution Time: 46 minutes

The discrete components are:

2 amplifiers from IC TL075 (supply voltages: +5V and -5V)

matched transistors from IC3086

1 PNP transistor

1 diode

1 zener 3.3V

resistors (1K, 22K, 47K, 3K3, 2K2, 330K, 100K)

Six of the 16 analog channels are fixed as external:

2 power supplies (+5V)

2 ground reference (0V)

input

output.

The other 10 channels (circuit nodes) are left as internal interconnection points of the circuit.

The input signal is a saw-tooth waveform of 100Hz with an amplitude range of 150mV to 500mV.

The fitness function used for evaluation of the configured circuits is:

$$\text{desired output} = -2 * \ln(V_{in}). \quad (2)$$

$$\text{Fitness} = (|\text{desired output} - \text{actual output}|)^5 \quad (3)$$

Figure 2 shows the schematic diagram of the best circuit evolved. About 200 discrete measurements were made to evaluate each circuit configured in PAMA-NG.

Figure 3 presents the input samples and the actual and desired outputs for the best circuit. This result shows that the evolved circuit performs well within expectations since only a small mapping error takes place.

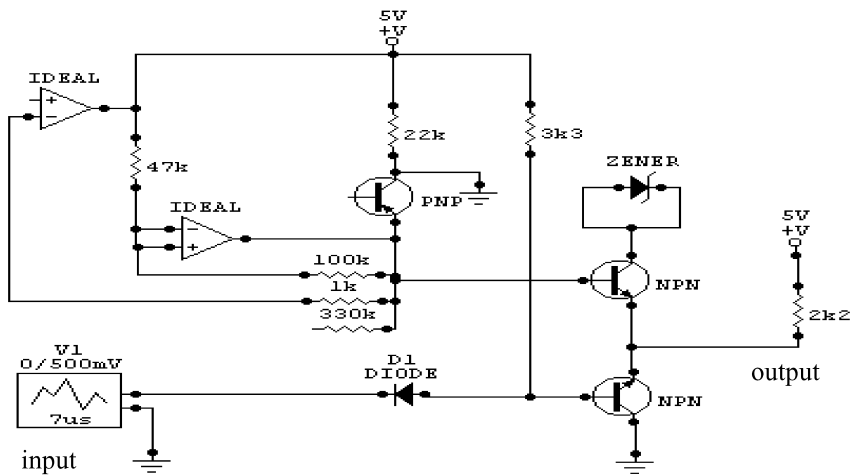


Fig. 2. Schematic of the best circuit evolved (without multiplexer's Ron)

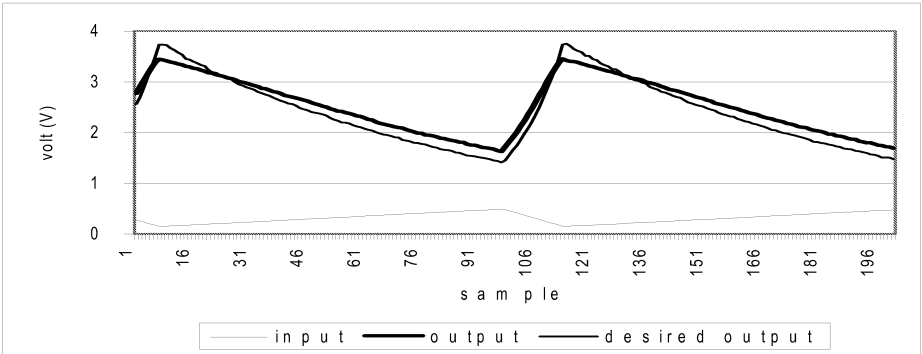


Fig. 3. Response of the best circuit evolved: a Logarithmic Amplifier with gain of two

3.2 S Membership Function Circuit

This experiment focuses on the development of a type *S* function – frequently used as a membership function in fuzzy inference systems – with amplitude of 3 volts and break points at 1 and 2 volts. The GA parameters are:

- Generations: 100
- Population: 400
- Crossover: 0.7
- Mutation: 0.1
- Steady State: 50
- Exponential Normalization *c* parameter : 0.9

The fitness function corresponds to the Mean Square Error of the difference between the desired output (*S* membership function) and the actual output. The transfer function and the schematic of the evolved circuit are illustrated in Figure 4 and Figure 5, respectively. Figure 4 shows the performance of the evolved circuit; it

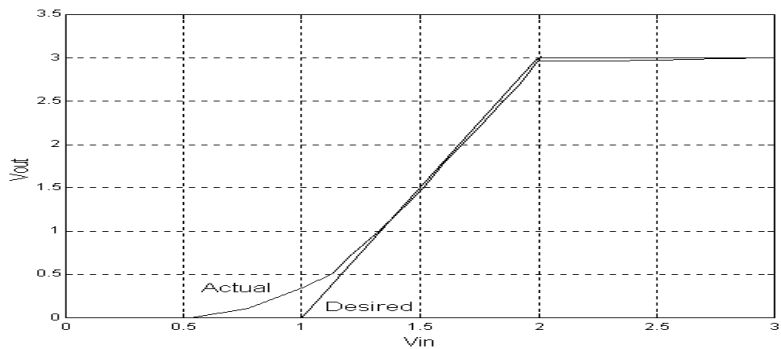


Fig. 4. Transfer function of type *S* membership function

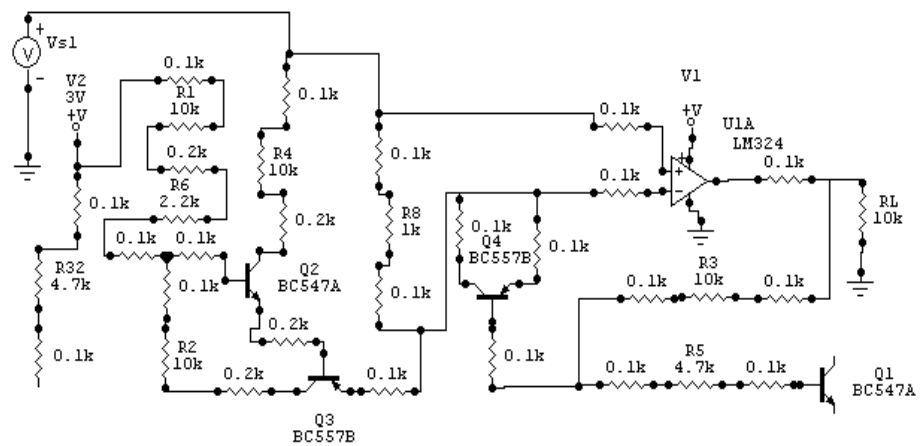


Fig. 5. Schematic of the evolved *S* membership function circuit

can be observed that only a small mapping error takes place at the break point of 1 volt. Figure 5 shows an unusual transistor configuration (Q4). This occurs quite often with EHW tools and demonstrates their ability to search for different circuit topologies

4 Conclusions

This work presented the PAMA-NG (Programmable Platform Multiplexer Array – Next Generation), a FPAA class platform that makes use of analog multiplexers, and some recent electronic designs carried out on it.

The PAMA-NG platform itself is being constantly updated. The latest version presents some advantages concerning the previous prototype platform which was first used to intrinsically evolve circuits [2]. The new ARC (Analog Reconfigurable Circuit) allows more component terminals (32 instead of 9), allowing the evolution of

a great number of circuits. In the new platform, the chromosome (configuration bits) is downloaded in parallel, in contrast with the serial interface used in previous versions. In PAMA-NG the converters were updated and the A/D conversion is performed by a multifunction I/O board connected to the PC bus. The circuit evaluation speed has increased considerably. The most recent enhancement is a D/A converter.

Further experiments shall consider the use of multi-objective criteria in circuit synthesis. The main difficulty to overcome is the access to different measures such as power dissipation and frequency responses. The synthesis of higher level circuits is also planned, particularly those related to analog fuzzy logic controllers [8]. The flexible PAMA-NG platform shall then be used to intrinsically evolve circuits based on coarse-grained building blocks. PAMA may also be used as a basic cell in a scalable and parallel system.

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