Challenges in Transmission Line Modeling at Multi-gigabit Data Rates

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Abstract. A signal trace on a PCB is modeled as a transmission line characterized by four parameters: R, L, C, and G, specified per unit length. A field solver is usually used to determine these frequency dependent parameters for a given trace geometry. This paper describes most recent trends in modeling PCB (Printed Circuit Board) interconnect traces in a context of current design requirements for multi-gigabit data interfaces.

1 Introduction: What Matters and Why?

No matter what signaling scheme is being designed — whether it's a common clock, source synchronous, or serial signaling — there are two main figures of merit: the noise margin and the timing margin.[1] It is the challenge of a signal integrity engineer to design the physical implementation of a bus to ensure that both noise and timing margins meet minimal requirements of the receiver.

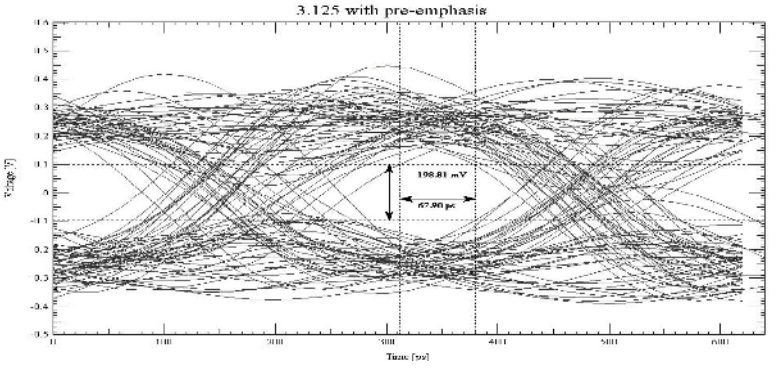

Fig. 1. Figures of merit: timing and noise margin

A receiver data sheet specifies the setup and hold times, as well as the switching threshold and the noise guard band around it. The signal shape at the receiver pad determines these margins in simulations. What is it that affects the signal shape as it arrives to the receiver's end of the trace? After leaving the driver pad, the signal propa-

[1] A system designer can define timing and noise margins in many different ways. Shown in Fig.1 is just one way of doing it.

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gates through the package; then it goes off on to the board where it spends most of the time flying on a trace – whether it's a top or bottom layer microstrip, or a stripline on one of the internal layers. Flying along the copper trace the signal gets attenuated, partly due to the losses in the copper trace and reference plane(s) and partly in the dielectric surrounding the trace. Various frequency components are attenuated to various degrees changing the shape of the arriving signal. Thus modeling the frequency dependent loss in traces becomes of great importance in predicting the signaling scheme performance. That's why so much effort has been spent industry wide on improving the PCB trace models and the algorithms making use of the models.

2 What Is a Trace Model?

From a system level viewpoint, a trace is a segment of an overall interconnect model, which also includes a driver, a receiver, their packages, possibly a connector or two, some vias... What is the trace model as shown in Fig.2? Typically a trace is viewed as a transmission line, and is characterized by the p.u.l. (per unit length) parameters R, L, C, and G.

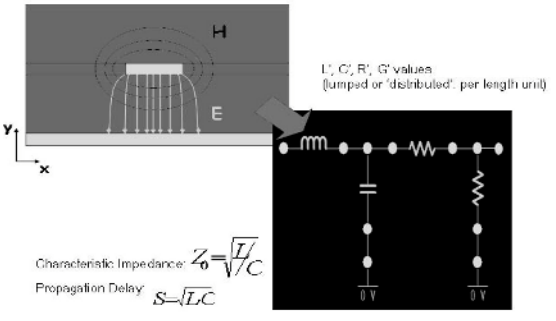

Fig. 2. Transition from physical trace geometry to an equivalent circuit model

Traces on PCBs have relatively low loss.[2] A trace without any loss works as an ideal delay element, and can be represented as a ladder of repeated sections, where each section is a series inductance L connected to a parallel capacitance C to ground. However, when losses become significant, they are accounted for by adding a series resistance R and a parallel conductance G to each section of the ladder model. The former, R, represents conductor loss, i.e. the loss due to the copper resistance, both in the trace and in the reference plane(s). The latter, G, represents the dielectric loss, i.e., loss due to some field energy drained into polarizing the dielectric around the trace, and, sometimes, a direct current leak through the dielectric. Each of these parameters is frequency dependent; it takes on a different value at different frequency. Therefore, one cannot accurately model a trace as a ladder with fixed values of R, L, C, and G. Such a ladder would *not* capture the frequency dependence of these parameters, and

[2] Low loss means R<<Z0.

therefore would *not* exhibit dispersive behavior one observes in reality.[3] Thus Fig.2 should by no means be construed as if a trace is modeled in any particular simulator as a ladder. (Most simulators do better than that.) The ladder representation is used here to merely explain the physical meaning of these parameters. To determine these four parameters at each frequency, a field solver (FS) is used. Below we describe what a FS can and should do.

3 What Are the Important Physical Effects?

There are several physical effects that should be taken into account by a field solver. They are: [4]

- Skin effect
- Proximity, or crowding effect
- Return path resistance
- Frequency dependent dielectric constant and dielectric loss in PCB materials.

Ultimately, we would like a field solver to capture these effects as accurately as possible. Any deviation of the model from the physical reality translates into errors in timing and noise margins as determined in simulations.

3.1 The Skin Effect

When a DC signal propagates through a PCB trace, or through any wire for that matter, the current flows so that it's evenly distributed through the conductor cross-section (see Fig.3). As the signal frequency rises, the magnetic field pushes out of the conductor while the current crowds out toward the wall of the conductor. At even higher frequencies, the current is flowing mainly within the thin layer under the conductor surface, or under the "skin" of the conductor. In the absence of other conductors in proximity, the current distributes itself evenly along the perimeter of the conductor cross-section. This in turn leads to frequency dependence of the inductance and resistance.

3.2 The Crowding Effect

The crowding or proximity effect manifests itself when another conductor is found near the conductor under consideration. In this case, through the distortion of the electromagnetic field, conductors sense each other's presence. This results in the high frequency current bunching up closer toward the side of the neighboring conductor.[5] If this other conductor is a reference plane in the PCB, then there is more current

[3] A more complex ladder model is possible, with many RLC elements in a section. See a paper at NESA, Inc. website. [1].

[4] R and L are affected by 3.1, 3.2, 3.3; G and C are affected by 3.4.

[5] See Eq.5.1 and Fig.5.3 in [2].

flowing along the side of the trace facing the reference plane. If this trace is routed as an asymmetrical stripline, the current tends to lean more toward the closer reference plane.

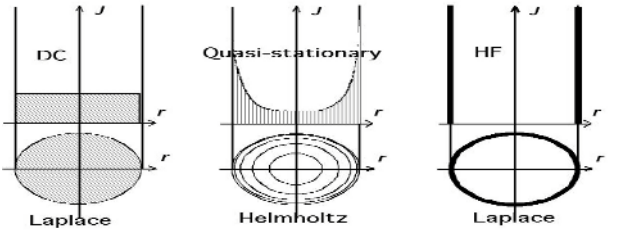

Fig. 3. Current density J as a function of frequency. Current spreads out toward the conductor surface as the frequency rises

3.3 The Return Path Resistance

It's not only the direct current in the trace, but also its return counterpart that faces some material resistance of copper. Previously, trace models in circuit simulators neglected this very real physical effect, treating the reference planes as ideal conductors. The return current density is fairly accurately described by the Lorentzian function. It concentrates more directly under the trace, and tapers off farther away from the trace.

3.4 The Frequency Dependent Dielectric Loss

There are two main mechanisms responsible for the dielectric loss in PCB materials. First, there is some, although very small, amount of direct current leakage through the dielectric even at zero frequency. Second, there is a polarization loss, which can be easily understood if the molecules of FR4, or other PCB materials, are viewed as dipoles. Water, for example, is a very prevalent molecule in FR4; it has a rather high dipole moment, and is responsible for the relatively high loss tangent of FR4 of about 0.02. When put in an alternating electric field, H_20 molecules tend to change their orientation following the electric field, just like a weathercock in a wind constantly changing its direction. It is the signal driver that causes the current to flow in the trace, and therefore causes the high frequency field to move down the trace along with the signal – as one happy cloud. The field, in turn, forces the molecules of the surrounding dielectric to oscillate.[6] While doing so the field loses some energy. Since the signal and the field "around it" are inseparable, the signal loses some of its strength too. The dipole molecules of the dielectric react differently to the external field at dif-

[6] This is exactly how a kitchen microwave works. It generates a narrow band MW field, which causes water molecules in food to oscillate. The kinetic energy of such rotational motion is, in fact, what we feel as "hot."

ferent frequencies. From DC to some high frequencies of about several hundred MHz, these molecules easily follow the external alternating field. However, at even higher frequencies, they find it harder and harder to respond to the external force. As the field frequency increases, the dipole molecules of the dielectric, first, lag behind the field, and then totally ignore it at very high frequencies. Via this mechanism the dielectric molecules drain the energy from the field – but drain it to various degrees at various frequencies. Since a digital signal comprises a bunch of various frequency components, each such signal component gets attenuated differently from others. With various frequency components being attenuated to a different degree, the signal shape changes in a rather convoluted manner. This is why it is very important to have accurate loss tangent data available for a field solver (see more on this issue in section 4 below).

4 How Are These Effects Accounted for in *R, L, C,* and *G* as Extracted by a Field Solver?

At frequencies where the skin depth becomes comparable to the trace's width, the skin effect sets in. The trace resistance bends up from its DC value at about the "knee frequency". For typical PCB dimensions, it happens around 100 kHz to 1 MHz range. Traditionally, SI simulators modeled this skin resistance as the square root of frequency. This is an approximation, however, that is accurate only for a perfectly round wire far away from a reference plane. A typical PCB trace cross section is far from being that. Presently, some circuit simulators take into account this real trace shape as well as the proximity of the reference plane(s) and other (adjacent) traces. This new level of FS sophistication does away with the traditional ω assumption, and results in a truer frequency dependent resistance R. It offers major improvements both around and above the knee frequencies, where, otherwise, estimated resistance may be off by as much as a factor of two. (see Fig.4). Parenthetically, let's mention another effect: the surface roughness of copper traces and planes. It certainly raises the trace resistance by some amount. The RMS roughness of "copper dandruff" can typically be between two and ten micron. In comparison, the skin depth of copper at one gigahertz is about two micron. Therefore, the current's higher frequency components comprising a digital signal do not just smoothly "flow" in the surface layer, but rather hop from peak to peak, thus facing much higher resistance. This issue has been dealt with in microwave design world, but has been mostly overlooked in high-speed digital designs. There is a conspicuous lack of data on this subject. Some engineers use fudge factor to account for this effect.

As far as inductance is concerned, it was typically modeled very accurately at frequencies well above the skin frequency, the higher the better. It was computed at infinite frequency (using BEM – Boundary Element Method), and assumed a constant across the entire frequency range: from DC to infinity. However, at frequencies below the knee, inductance is higher. It can be higher by up to 45% at DC than its value at high frequencies. (See Fig.5)

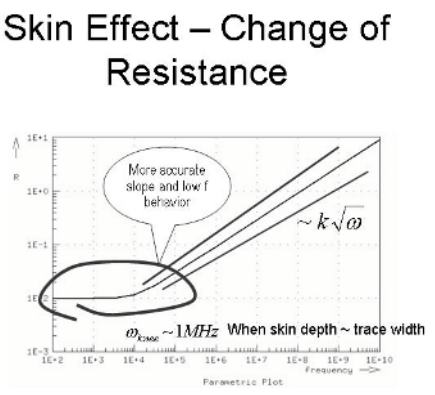

Fig. 4. Accurate field solver does away with traditional assumptions about the resistance's frequency dependence

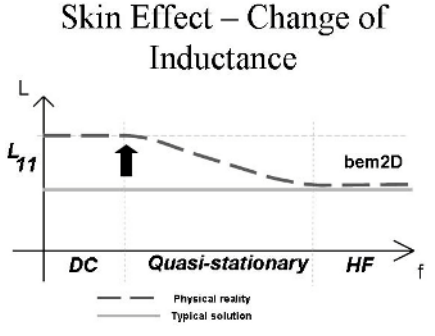

Fig. 5. Due to internal inductance, the DC value can be up to 45% higher than traditionally computed by BEM (at HF limit)

Such is the physical reality. Some circuit simulators successfully take this effect into account. These more accurate inductance values at low frequency result in more accurate modeling of signal shape at the receiving end. As pointed out above, all this translates into more accurate prediction of both the noise and timing margins. Mutual inductance follows the same trend as self-inductance. When modeling capacitance we usually assume capacitance to be independent of frequency. In reality, however, the real part of the dielectric constant is weakly dependent on frequency, and with it the capacitance. Its imaginary part, or the loss tangent, affects the conductance G

Conductance G, the last - but not least of the four p.u.l. parameters - actually becomes the dominant loss mechanism at frequencies above several hundred megahertz. Even "a slow" signal with a rise time of 0.5 ns has a (-3 dB) power density spectrum point at about 700 MHz. At this frequency the dielectric loss is comparable to the loss caused by the skin resistance. Thus including the conductance into the trace model

becomes a must. Conductance is comprised of two parts: the DC and the AC, as detailed in section 3.4 above. The DC component is negligible for all practical purposes, whereas the AC term is to be modeled as accurately as possible. This term is directly proportionate to the dielectric loss tangent. Traditionally, the latter was assumed a constant, and PCB manufacturers provided its value at a single frequency, typically 1 MHz. In that case, conductance rises linearly with frequency, and has no limit at higher frequencies. (top line on Fig.6). However, using this model will create an electrical short on any trace at sufficiently high frequencies.

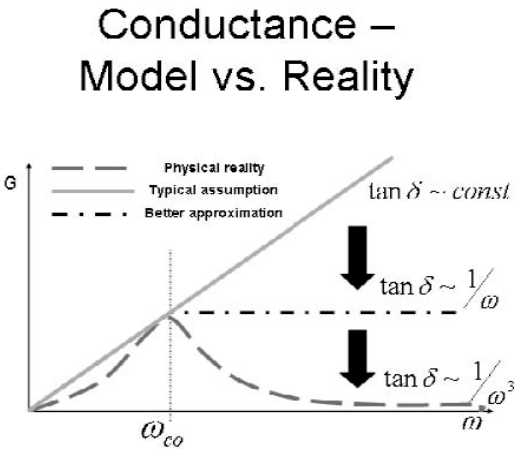

Fig. 6. The ever-growing level of sophistication in conductance modeling: evolutionary view

To counteract this non-physicality, some circuit simulators now clamp G at some frequency, thus again making an assumption about the frequency dependence of the loss tangent (as inverse frequency; see middle line on Fig.6). This is a definite improvement in accuracy. It is known, however, from the material modeling of dielectrics, that asymptotic behavior at very high frequencies should follow the inverse power of three. (Dashed line Fig.6) Signal integrity tools, however, are not in the business of doing molecular modeling of dielectric materials, and are anxiously waiting for the measured dielectric property data to become widely available. In the meantime, some tool vendors are preparing for the day this data becomes readily available by allowing the user to specify arbitrary frequency dependence for the conductance matrix. Thus the onus now is on the user to come up with such data, whether he does measurements in-house or relies on his fab house or any other third party.

5 Summary

In this article we have discussed why accurate modeling of a PCB trace is very important for high-speed design, especially at multi-gigabit data rates. We have identi-

fied what a PCB trace model is. We listed most significant physical phenomena and discussed how they affect the RLCG parameters. Describing each of these parameters, we gave a historical perspective, as well as outlined typical limitations that exist in some commercial Signal Integrity tools. Hopefully, this article will raise the level of awareness of both a high-speed system designer and EDA tool companies, and help them to be mindful of various aspects of modeling PCB and IC package traces.

References

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