Disjoint Region Partitioning for Probabilistic Switching Activity Estimation at Register Transfer Level

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Abstract. This paper presents a partition method for probabilistic switching activity estimation of combinational circuits described at register transfer level (RTL). Probabilistic estimation of switching activity requires large and complex models that could be unfeasible for large circuits; therefore, circuit partitioning becomes a necessary step to address the analysis. Nevertheless, partition methods imply approximations that produce inaccurate results. We present a partition method based on disjoint signals that minimizes the error and, in addition, it is easy to carry out. Results show important reductions on the binary decision diagrams (BDD) of the probabilistic model as well as low errors. Furthermore, the BDD reduction ratio shows a tendency to increase with large circuits; whilst error seems to decrease with the circuit size.

Keywords: Switching activity, CAD, RTL, BDD, activity estimation, digital circuit design, VHDL, circuit partition, power estimation.

1 Introduction

During the last decades, the complexity of digital circuits has experimented an extraordinary growth. Besides, the scaling technologies have confronted digital designers with new challenges, such as power consumption and reliability. In addition to these difficulties, time-to-market pressures are aggravated by shorter product cycles due to the rapid technology changes.

Therefore, new methodologies and tools are required to assist in digital circuit design. These methodologies and tools should facilitate a seamless design flow in which unnecessary design iterations are avoided. Frequently, despite the circuit functionality is correct, the non-fulfillment of other design issues impel to redesign it.

The ability to estimate the final circuit characteristics constitutes an important aspect of a methodology. Estimators, which anticipate these final characteristics, help designers to make early design decisions and avoid costly design iterations.

At the present time, power consumption is one of the most relevant issues to be considered in electronic design, both due to the proliferation of mobile devices and due to the excessive power consumption of high performance circuits, which require cooling

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systems that increment the final cost and reduce the reliability. Power consumption is considered one of the main challenges for the evolution of semiconductor industry [1].

Dynamic power consumption, caused by the switching activity of the circuit's internal signals, represents an important part of the total circuit power consumption. The objective of this work is the analysis of the circuit switching activity, which not only is an essential parameter of the dynamic power consumption, but also may contribute to other analyses such us testability, reliability and quality.

Switching activity estimation of circuit signals constitutes a difficult task. The problem has been addressed using two different approaches: dynamic and static techniques. Dynamic techniques simulate the circuit under a "typical" input vector sequence and afterwards, signal activity statistics are collected. The main disadvantages of dynamic techniques are the excessively large simulation times and the dependence of the results on the input sequence.

On the other hand, static techniques analyze the circuit and elaborate mathematical models that propagate signal probabilities and activities from the circuit inputs to the outputs. Static methods are much faster than dynamic but their main drawback is the complexity of the resultant model for large circuits. In these cases, simplifications, which may decrease the estimation results accuracy, have to be carried out. Static techniques are also known as probabilistic techniques because they usually resort to the theory of probability.

In this paper we present a partition method to address the probabilistic calculation of the switching activity of combinational circuits described at RTL. Once the circuit is partitioned, the signal activity is computed using Reduced Ordered Binary Decision Diagrams (ROBDD [2], just BDD henceforth). The proposed partition limits the BDD size allowing to analyze large circuits. The partition method is simple to carry out at RTL and, when the proposed guidelines are followed, the error remains low.

This paper is structured as follows: in the next section the previous work is exposed. Afterwards, the proposed partition method presented. Following, the experimental results are shown, considering both the benefits of the proposal and the error produced. In the last section, the conclusions are drawn.

2 Prior Work

Many proposals have contributed to the probabilistic analysis of digital circuits. Some of these works estimate the signal probability rather than the signal activity because signal probability is a useful characteristic for some kind of analysis such as testability analysis. These works have been included because signal probability is a previous step for switching activity calculation and, in some particular cases, signal activity can be calculated directly from signal probability. Nevertheless, signal activity computation entails more difficulties and produces an extraordinary growth of the probabilistic models.

One of the earliest works in this field was presented by Parker [3]. In this work, a polynomial representing each gate output probability was generated. Afterwards,

signal probabilities were calculated from inputs to outputs through these polynomials. Structural dependences were considered but, for large circuits, the method could be intractable. This method only calculated signal probability, but not switching activity.

The problem is that if structural dependences (due to reconvergent fanout) are not considered, probability and activity calculations may be erroneous. Figure 1 shows an example in which if probability is calculated using dependent signals the result is wrong. Thus, independent signals should be searched back in order to obtain correct results.

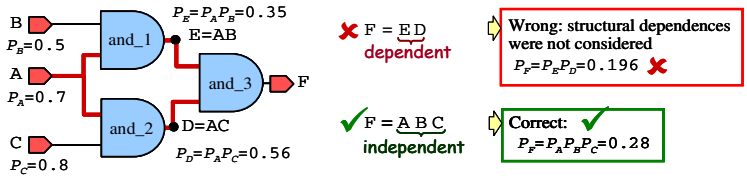

Fig. 1. Effect of structural dependences on probability computations

In order to reduce the complexity, Seth proposed to partition the circuit in *supergates* [4]. Each supergate only contained independent signals. Nevertheless, in large and highly reconvergent circuits, supergates could embrace large areas or they could even embrace the whole circuit. In these cases, this work proposed to limit the reconvergence area to a maximum depth from the supergate output.

Ghosh [5] proposed to calculate signal activity performing an XOR at the output function at two consecutive times: $a = P\ \{\ y^0 \oplus y^T\ \}$. Probabilities and activities were computed using BDDs, but for large circuits, the method was unfeasible due to the BDD sizes. Hence, approximate simulative techniques were proposed.

Schneider [6] introduced Markov chains, Shannon expansion and reconvergence analysis in order to handle temporal correlations and structural dependences. Computations were implemented using BDDs, whose sizes were also controlled by a maximum depth of the partitions. As a result, approximate values were also obtained.

Marculescu [7] handled input pairwise spatial correlations. BDDs were used to propagate switching activities and spatial correlations. For large circuits, an approximate approach was also proposed.

In order to reduce the size of circuit partitions, Agrawal [8] proposed to perform disjoint partitions. At gate level, mutually disjoint signals are not easy to find; therefore, an algorithm to locate them was developed. To determine whether signals are disjoint, a simulation-like procedure was used. Nevertheless, the method did not find all disjoint signals and symbolic analysis was required, resulting in higher time and memory complexities. Only probabilities were computed in this work, for which the results are exact. In figure 2 there is a circuit with disjoint signals. It can be observed that using disjoint signals, the probability equation results simpler. The result is the same as the one that is calculated by reconvergent regions (independent events). Note that if signals D and E of figure 2 were not mutually disjoint, the result would not be correct, as it happened in figure 1.

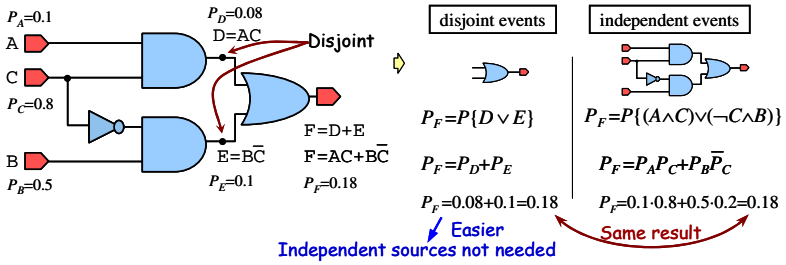

Fig. 2. Disjoint signals may simplify probability computations

Bhanja [9] used Bayesian networks to elaborate the probability model. Bayesian networks not only make explicit conditional dependences between nodes, but also they constitute an efficient computational mechanism to update probabilities. Large circuits had to be partitioned to avoid an excessive usage of computational and memory resources

In the field of testability analysis, Fernandes [10] proposed a probabilistic method to estimate controllability of sequential RTL circuits described in Verilog. The method approximately resolved the Champan-Kolmogorov equations that describe the steady state behavior of the circuit. It was the first static approach that calculated probabilities of RTL designs, due to fact that the field of the analysis is testability, switching activities were not computed.

Except for the work of Agrawal [8] (related to signal probability), all the contributions analyzed have proposed an approximate solution for large circuits. Otherwise, the probabilistic model would be totally impractical due to its size.

In what follows, we introduce a partition method based on disjoint signal detection at RTL. Contrary to what happens at gate level, in many cases, disjoint signal detection at RTL is straightforward. However, disjoint partitions produce approximate activity results, but not for signal probability. Therefore, rules that minimize the error will be presented.

3 Proposed Partition Method

We propose to perform a disjoint partition to reduce the complexity of the probabilistic model. Although disjoint partitions do not provoke inaccuracies for signal probabilities, the resulting activity is approximate. We have addressed this partition method in previous works [11], [12], but in this paper we propose an efficient disjoint partition in which errors are minimized.

This section first shows how disjoint regions are identified. Then, explains how to calculate the activity in disjoint regions and the error produced. Last, strategies to minimize the error are proposed.

3.1 Disjoint Regions Identification

Most of the proposals look for independent signals for circuit partitioning; hence, they perform reconvergent partitions. For large circuits, in which reconvergent partitions

still produce large regions, they propose to further divide the partitions at the cost of accuracy. Only Agrawal proposed [8] to look for disjoint signals to divide circuits in smaller disjoint regions. Since his proposal is restricted to gate level, the method to find disjoint signals is not straightforward.

In contrast, the identification of many disjoint signals is effortless at RTL. RTL conditional statements create disjoint signals and, as a result, they may be immediately detected. Generally, conditional statements represent multiplexers in which the condition selects what signal is assigned. Multiplexers generate mutually disjoint signals. Figure 3 shows the different representations of a multiplexer: in a hardware description language (VHDL), at RTL and at gate level.

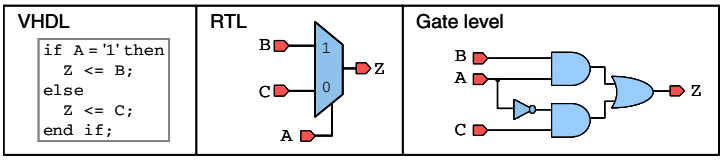

Fig. 3. Different representations of a multiplexer

As it can be seen in figure 3, identification of multiplexers is straightforward at RTL, either if described in a description language such as VHDL or using schematics. On the contrary, at gate level is not easy because gates may have different arrangements from the one of figure 3, especially in larger multiplexers.

3.2 Activity Calculation in Disjoint Regions

As it has been explained, disjoint partitioning is an effective practice to simplify signal probability computations. These partitions do not provoke any accuracy loss in signal probability computation; however, they produce inaccuracies in activity.

If disjoint partitions have been carried out, the activity equation for a multiplexer such as the one in figure 3 can be built applying the Shannon expansion [6] to the activity function and cofactoring the function with respect to the selection signal A:

$$a_Z = P(A_{1\to1})\cdot a(Z)_{A_{1\to1}} + P(A_{0\to0})\cdot a(Z)_{A_{0\to0}} + P(A_{0\to1})\cdot a(Z)_{A_{0\to1}} + P(A_{1\to0})\cdot a(Z)_{A_{1\to0}}. \quad (1)$$

Cofactors $a(Z)_{A_{0\to1}}$ and $a(Z)_{A_{1\to0}}$ depend on alternatives B and C, but not on selection signal A. Nevertheless, when signals B and C are not independent, these cofactors are inaccurate if they are calculated directly from alternatives B and C, but not from their independent sources. These two cofactors will be called activity cofactors. The equation of the cofactor $a(Z)_{A_{0\to1}}$ is:

$$a(Z)_{A_{0\to1}} = P\{(C^0=1)\wedge(B^T=0)\} + P\{(C^0=0)\wedge(B^T=1)\}\ . \quad (2)$$

If independent sources are not taken into account, probabilities can be decomposed. The resultant approximate equation is:

$$a(Z)_{A_{0\to1}} \approx P\{C^0=1\}\cdot P\{B^T=0\} + P\{C^0=0\}\cdot P\{B^T=1\}\ . \quad (3)$$

Considering the model as strict-sense stationary, the equation results:

$$a(Z)_{A_{0\to1}} \approx P_C \cdot \overline{P_B} + \overline{P_C} \cdot P_B . \tag{4}$$

Calculating the other cofactors and since $a_A = P(A_{0\to1}) + P(A_{1\to0}) = 2 \cdot P(A_{0\to1})$, equation 1 results in:

$$a_Z \approx P(A_{1\to1}) \cdot a_B + P(A_{0\to0}) \cdot a_C + a_A \cdot [P_C \cdot \overline{P_B} + \overline{P_C} \cdot P_B] . \tag{5}$$

The first two terms of equation 5 are accurate and the last term is approximate. Note the simplicity of the resulting formula, which only depends on the multiplexer inputs. Therefore, it is not necessary to look for independent signals and thus, the usage of large reconvergent regions is avoided.

3.3 Minimizing the Error Produced by Disjoint Regions

Since only the last term of equation 5 is approximate, the smaller the activity of the selection signal is, the lower the influence of the approximation will be. Besides, the activity calculation is approximate only when reconvergences affect the inputs of the multiplexer. Thus, the following conditions have been deduced to minimize the error:

1. The selection signal should be independent of the alternatives
2. The selection signal should have low activity
3. Reconvergent signals should have low temporal correlations
4. There should be a low rate of reconvergent sources for the alternatives

Next, the fundamentals of these conditions will be explained. It is not necessary to fulfil all the conditions but the first condition is considered indispensable. That is, the selection signal has to be independent of the alternatives.

When the first condition is met, only the activity cofactors (eq. 4) are approximate. Therefore, just the last term of equation 5 is approximate. The fulfillment of this condition justifies the second condition.

The second condition imposes a low activity on the selection signal. Due to the first condition, only the activity cofactors are approximate; therefore the lower the selection signal activity is, the smaller the influence of the activity cofactors on the activity equation will be (eqs. 1 and 5).

Since the simplifications carried out to obtain equation 5 are based on considering that the reconvergent signals are temporarily uncorrelated, the third condition states that the error drops when reconvergent signals have low temporal correlations.

The fourth condition indicates that should be a low rate of reconvergent signals influencing the alternatives. Therefore, the influence of the reconvergences would be low. This is because only the activities of the reconvergent signals are approximate.

These four conditions can be classified in structural conditions and extrinsic conditions. The first and the fourth conditions are structural because the fulfillment of these conditions depends on the circuit structure; therefore, they are invariant for a specific circuit. Conditions second and third depend on the probability and activity values of the signals. Thus, conditions vary with the external circumstances; hence, they have been denominated extrinsic conditions.

The fulfillment of these conditions should be analyzed during the circuit partitioning. The necessary information to evaluate both structural and extrinsic conditions can be obtained during the partition process. Circuits may be partitioned in very small disjoint regions. Nevertheless, since disjoint partitions produce inaccuracies, these partitions should not be applied exhaustively. *Exhaustive disjoint partitions* are those resulting from partitioning the circuit in the maximum number of disjoint partitions. This partitioning strategy is not convenient because errors rise and because having too many small regions do not produce any practical advantage.

On the contrary, circuits must be partitioned only in those nodes whereon the error is minimized due to the circuit structure and conditions. A few strategic disjoint partitions may extraordinarily reduce BDD sizes maintaining the error low. *Minimum disjoint partitions* are those partitions resulting from applying disjoint partitions exclusively in the nodes where:

- The resulting disjoint regions are significantly smaller than the original
- The resulting disjoint regions remain large but manageable
- The analysis of the proposed guidelines for the disjoint partition is favorable

4 Experimental Results

This section analyzes the effect of the proposed disjoint partitions on the BDD sizes and on the error. In order to carry out the analysis, an automated tool has been developed. This tools analyses VHDL circuits and obtains the activity and probability values of their output ports and internal signals. As the tool is a preliminary version, the VHDL circuits have to be manually adapted: they have to be flattened and vector signals have to be set as bit signals. As a consequence, a limited set of circuits have been analyzed. Besides, since our analysis is performed at RTL, it could not have been directly compared with other works, because they have been done at gate level. As a consequence, we were not be able to use the same benchmarks (ISCAS'85 [13]).

Four circuits have been analyzed, three ALUs and an adder/subtracter. The first circuit has been taken from [14] and the others have been taken from the ALU of the 8051 microcontroller [15]. Except for the first circuit, the circuits have been analyzed with different bus widths. Table 1 shows general characteristics of these circuits (bus width, number of gates of the synthesized circuit, number of input and output ports).

Table 1. Circuits taken for the experiments

no.	Name	Width	Gates	Inputs	Output	Source	Description	no.	Name	Width	Gates	Inputs	Output	Src.	Descrip.
1	alupeq	4	510	11	7	[14]	4-bit ALU	3	alu8051s	7	383	23	10	[15]	Simplif. 8051 ALU
2	addsub	7	70	16	10	[15]	Adder/ subtracter			8	415	25	11		
		8	72	18	11					9	450	28	13		
		9	87	20	13					10	487	30	14		
		10	101	22	14					11	517	32	15		
		11	108	24	15					12	557	34	16		
		12	117	26	16			4	alu8051	6	520	27	9	[15]	8051 ALU
		13	125	28	18					7	571	30	10		
		14	139	30	19					8	629	33	11		
		15	146	32	20					9	685	37	13		
		16	152	34	21					10	759	40	14		

When the proposed guidelines for the partition are followed, smaller BDDs are obtained, especially for the activity BDDs (*a*BDDs [16]). For each circuit, figure 4 shows the number of *a*BDD nodes ratio between the analysis with no disjoint partition (exact-RTL) and with it. It can be observed from figure 4 that the larger the bus width is the higher the ratio is. The smallest ratio is for circuit "alupeq", which is only 1.5. Nevertheless, this circuit is small; hence, it is not really necessary to partition it.

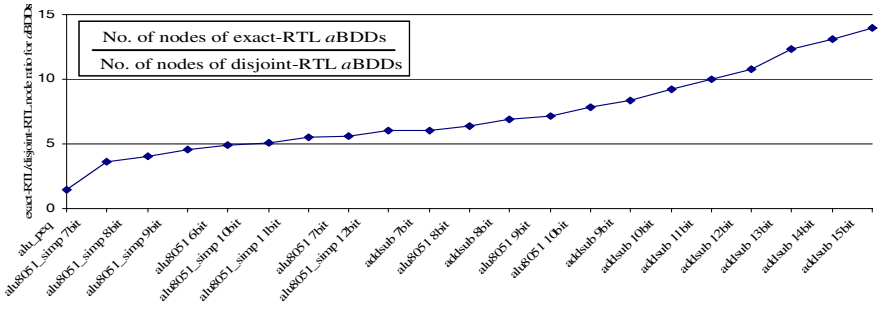

Fig. 4. Ratio of exact-RTL *a*BDD nodes to disjoint-RTL *a*BDD nodes

The circuit's largest BDD is critical because it could hinder the analysis due to an excessive memory demand. Table 2 shows the evolution of the largest *a*BDD with the operand's bus width. Disjoint partitions maintain the worst case *a*BDD in constant size; whereas exact-RTL *a*BDDs depend linearly on the bus width. Thus, using disjoint partitions, any of the circuits could be analyzed regardless of the bus width.

Table 2. Largest *a*BDD for 8-bit and n-bit bus width with and without disjoint partition

Circuit	exact-RTL		disjoint-RTL	
	worst case *a*BDD (8 bits)	worst case *a*BDD (*n* bits)	worst case *a*BDD (8 bits)	worst case *a*BDD (*n* bits)
addsub	479	$74 \cdot n - 113$	13	13
alu8051s	3215	$423 \cdot n - 169$	370	370
alu8051	10807	$1467 \cdot n - 929$	912	912

All these circuits have been synthesized into logic gates. The resulting gate-level BDDs were larger than the disjoint-RTL ones because no disjoint partition could be easily performed. But they were even larger than the exact-RTL ones due to a better BDD variable ordering achieved at RTL [12].

Error Analysis. Although disjoint partitions provoke inaccuracies; if the proposed guidelines are followed the error is minimized. The BDD of table 2 and figure 4 could be smaller if an *exhaustive partition* would be performed; however, in order to minimize the error, it is advisable to make *minimum disjoint partitions* and avoid exhaustive partitions.

Since errors not only depend on the model but also on the input sequence, they cannot be characterized by just a number obtained at specific input conditions. There are infinite combinations of input probabilities and activities which produce different errors. Generally, other works have assigned certain probability and activity values to

the inputs. We have performed a wider analysis in which the values of a probability-activity mesh have been assigned to the inputs. We have assigned 31 different probability values and 64 activity values. Hence, there are 1024 probability-activity pairs and thus, we have performed 1024 activity estimations for every circuit. Errors have been obtained comparing with simulation. As an example, figure 5 shows the error distribution of the highest error outputs of circuits "alupeq" and "alu8051s".

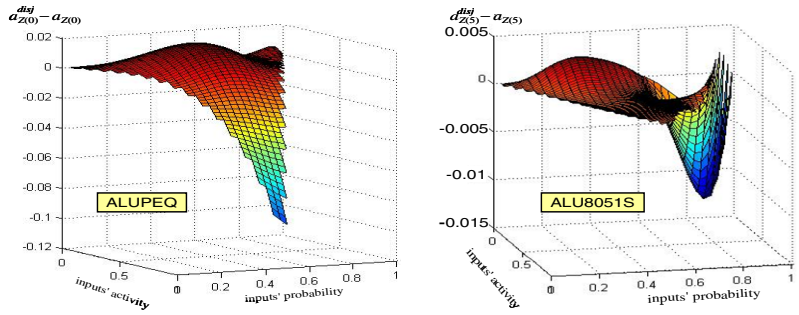

Fig. 5. Error distribution of signal $Z(0)$ of circuit "alupeq" and signal $Z(5)$ of circuit "alu8051s" for all the range of possible probabilities and activities of the inputs

The statistics of the error distributions have been extracted in table 3. The maximum error ($|e_{max}|$) is in absolute value. Notice that the smaller the exact-RTL *a*BDD is, the higher the error is. Circuits "alupeq" and "addsub" have the highest errors and have the smaller exact-RTL *a*BDDs; whilst circuit "alu8051s", having an larger exact-RTL *a*BDD, has lower errors. The largest circuit ("alu8051") has negligible errors, even for its maximum error. Therefore, it is better to perform the partitions on large circuits, for which more interesting BDD reductions are achieved and the error is minimized. Although the same benchmark could not be used, our errors are similar or smaller than other proposals [9], [7], [6]. Even though we have considered wider input conditions and we only have accounted the outputs for the mean error (which generally have larger errors than the internal nodes).

Table 3. *a*BDD reduction and error statistics when partitioning the circuit in disjoint regions

Circuit		Worst case *a*BDD		Error statistics		
No.	name	exact-RTL	disjoint-RTL	μ	σ	$\lvert e_{max} \rvert$
1	alupeq	438	85	0.0080	0.0143	0.109
2	addsub	479	13	0.0011	0.0049	0.125
3	alu8051s	3215	370	0.0011	0.0019	0.012
4	alu8051	10807	912	0.00056	0.00088	0.0068

5 Conclusions

A partition method to estimate the switching activity of RTL combinational circuits has been presented. The method performs the partition on disjoint signals, which are easy to find at RTL. In order to minimize the error, guidelines to perform the partition

have been proposed. The results show an important node reduction in BDDs as well as low errors. In addition, results show that the larger the circuit is, the greater the BDD reductions are and the lower the errors are. Furthermore, when the disjoint partition is performed, the largest BDD remains constant independent on the operand's bus width. Hence, there will not be memory limitation for the computations when disjoint partition are performed. The proposed estimation method has been implemented in a preliminary automated tool.

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