Analog Circuits and Systems Optimization Based on Evolutionary Computation Techniques

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Manuel F.M. Barros
To Fatuxa, Catarina, Lucas and Joaquim

Jorge M.C. Guilherme
To Paula, Patricia and Inês

Nuno C. G. Horta
To Carla, João and Tiago

Preface

The microelectronics market, with special emphasis to the production of complex mixed-signal systems-on-chip (SoC), is driven by three main dynamics, time-to-market, productivity and managing complexity. Pushed by the progress in nanometer technology, the design teams are facing a curve of complexity that grows exponentially, thereby slowing down the productivity design rate. Analog design automation tools are not developing at the same pace of technology, once custom design, characterized by decisions taken at each step of the analog design flow, relies most of the time on designer knowledge and expertise. Actually, the use of design management platforms, like the Cadences Virtuoso platform, with a set of integrated CAD tools and database facilities to deal with the design transformations from the system level to the physical implementation, can significantly speed-up the design process and enhance the productivity of analog/mixed-signal integrated circuit (IC) design teams. These design management platforms are a valuable help in analog IC design but they are still far behind the development stage of design automation tools already available for digital design. Therefore, the development of new CAD tools and design methodologies for analog and mixed-signal ICs is essential to increase the designer's productivity and reduce design productivitygap.

The work presented in this book describes a new design automation approach to the problem of sizing analog ICs. The developed design optimization tool, GENOM, is based on a modified genetic algorithm (GA) kernel and incorporates heuristic knowledge on the control mechanism allowing a significant reduction on the required number of generations and, therefore, iterations to reach the optimal solution. However, the optimization process, employing a simulation-based approach with a kernel based on stochastic optimization techniques is clearly a computational intensive task typified by high dimension search spaces and high cost function evaluations. A step forward to enhance the efficiency of the implemented optimization tool corresponds to the introduction of behavior modeling techniques. The model introduced in this paper follows a supervised learning strategy based on support vector machines (SVM) which, together with an evolutionary strategy, is used to create feasibility models in order to efficiently prune the design search space during the optimization process, thus, reducing the overall number of required evaluations.

The book is organized in seven chapters. The first one, the introduction, presents the motivation and outlines the original goals for this research work.

Chapter 1 provides an overview of the thesis motivations, research goals and main contributions.

Chapter 2 presents a state-of-the-art review in analog IC design automation field by analyzing and comparing methods, strategies and tools presented in literature, including some commercial tools.

Chapter 3 starts with an overview on computation techniques to solve nonlinear optimization problems with focus on evolutionary optimization algorithms. Then, it introduces a new optimization kernel based on genetic algorithms applied to analog circuit optimization. It includes a detailed description of the fitness function, the genetic operators and design methodology in order to obtain an efficient and robust analog circuit design.

Chapter 4 explores the main learning techniques used to manage large amount of information, to discover complex relationships among various factors and extract meaningful knowledge to improve the efficiency and quality of decision-making. In particular, it discusses the use and the integration of a learning model based in support vector machine (SVM) in order to improve the evolutionary optimization strategy for analog circuit design applications introduced in chapter 3.

Chapter 5 describes the analog design environment and architecture of GENOM optimization tool. It discusses the methodology, representation and architecture issues, giving details of the analog IC design representation, interfaces between the synthesizer and evaluation algorithms, and software architecture. The main options taken in this work approach will be described and justified.

Chapter 6 presents several synthesis experiments, demonstrating the capabilities of the system and providing some insight into factors that affect the synthesis process. The suite of test circuits is taken from standard text books and technical papers. The first section describes the performance metrics, the algorithm optimization strategy and input data of each the experiment. The resulting performances computed automatically by the optimization tool during the evolutionary process are delivered to the user in the form of output reports or by dynamic graphics or reports. Apart from accuracy, mean and standard deviation of execution time and evaluation cycles are also presented. Additionally, information regarding the circuit, such as circuit sizing, corner information and performance are also specified.

Finally, chapter 7 presents the conclusions and the research contributions of the thesis and the improvements that are possible to GENOM.

Manuel F.M. Barros
Jorge M.C. Guilherme
Nuno C.G. Horta

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List of Abbreviations

AI	Artificial Intelligence
AMD	Advanced Micro Devices
AMS	Austrian Micro Systems
ADC	Analog-to-Digital Converter
ADSL	Asymmetrical Digital Subscriber Line
AIDA	Analog Integrated Circuit Design Automation platform
ASIC	Application Specific Integrated Circuits
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CAD	Computer Aided Design
CMFB	Common Mode Feedback Amplifier
CMOS	Complementary Metal Oxide Semiconductor
CMR	Common-Mode Range
CMRR	Common-Mode Rejection Ratio
DA	Design Automation
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
EDA	Electronic Design Automation
EP	Evolutionary Programming
EA	Evolutionary Algorithms
GA	Genetic Algorithms
GBW	Gain-Bandwidth Product
GP	Geometrical Programming
MOO	Multi-Objective Optimization
NMOS	N-channel MOSFET
NN	Neural Networks
OPAMPS	Operational amplifiers
OR	Output Range
OTA	Operational Transconductance Amplifier
PMOS	P-channel MOSFET
PSRR	Power Supply Rejection Ratio
SNR	Signal-to-Noise Ratio
GUI	Graphical User Interface
IC	Integrated Circuit
IP	Intellectual Property
OR	Output Range

RF	Radio Frequency
SA	Simulated Annealing
SoC	System-on-Chip
SNR	Signal-to-Noise-Ratio
SVM	Support Vector Machines
SPICE	Simulated Program with Integrated Circuits Emphasis
VLSI	Very Large Scale Integration
THD	Total Harmonic Distortion
UGBW	Unity-Gain Bandwidth
VHDL	Very High Speed Integrated Circuits Hardware Description Language
VHDL-AMS	Analog Mixed Signal VHDL