Wireless Multimedia Sensor Networks on Reconfigurable Hardware

Li-minn Ang • Kah Phooi Seng • Li Wern Chew Lee Seng Yeong • Wai Chong Chia

# Wireless Multimedia Sensor Networks on Reconfigurable Hardware

Information Reduction Techniques



Li-minn Ang Kah Phooi Seng School of Engineering Edith Cowan University Joondalup, Western Australia Australia

Li Wern Chew Intel Architecture Group Intel Corporation Penang, Malaysia Lee Seng Yeong Wai Chong Chia Dept. of Computer Science and Networked Systems Sunway University Selangor, Malaysia

ISBN 978-3-642-38202-4 ISBN 978-3-642-38203-1 (eBook) DOI 10.1007/978-3-642-38203-1 Springer Heidelberg New York Dordrecht London

Library of Congress Control Number: 2013950611

#### © Springer-Verlag Berlin Heidelberg 2013

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed. Exempted from this legal reservation are brief excerpts in connection with reviews or scholarly analysis or material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work. Duplication of this publication or parts thereof is permitted only under the provisions of the Copyright Law of the Publisher's location, in its current version, and permission for use must always be obtained from Springer. Permissions for use may be obtained through RightsLink at the Copyright Clearance Center. Violations are liable to prosecution under the respective Copyright Law.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

While the advice and information in this book are believed to be true and accurate at the date of publication, neither the authors nor the editors nor the publisher can accept any legal responsibility for any errors or omissions that may be made. The publisher makes no warranty, express or implied, with respect to the material contained herein.

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

To Grace Ang Yi-en, our blessed daughter for all the joy you bring. —Li-minn Ang and Kah Phooi Seng To my parents for your unconditional love and never ending support. —Li Wern Chew To my parents and loved ones for your uncoasing support and love

unceasing support and love. -Lee Seng Yeong

To my parents, thank you for all your unconditional support. –Wai Chong Chia

#### Acknowledgements

We would like to express our deepest appreciation to all the people who contributed to the work presented in this book. We would like to thank our former Ph.D. student Christopher Ngau Wing Hong, in particular for his help on some of the work described in Chaps. 4 and 5.

Li-minn Ang and Kah Phooi Seng gratefully acknowledge support from the Centre for Communications Engineering Research at Edith Cowan University, Australia. Lee Seng Yeong and Wai Chong Chia gratefully acknowledge support from the School of Computer and Networked Systems at Sunway University, Malaysia. Li Wern Chew gratefully acknowledges support from the Intel Architecture Group at Intel, Malaysia. We gratefully acknowledge our Springer editor Ronan Nugent and the publication team for their diligent efforts and support towards the publication of this book. The support of the Malaysian eScience Fund research grants (01-02-12-SF0054, 01-02-16-SF0026) is gratefully acknowledged.

#### Contents

1	Intro	duction	1
	1.1	Overview	1
	1.2	Book Organisation	3
2	Wire	eless Multimedia Sensor Network Technology	5
	2.1	Introduction	5
	2.2	WMSN Network Technology	6
		2.2.1 Structure of a WMSN Network	7
		2.2.2 WMSN Network Architecture	9
	2.3	WMSN Node Technology	13
		2.3.1 Structure of a WMSN Node	13
		2.3.2 Sensing Unit	14
		2.3.3 Processor Unit	19
		2.3.4 Communication Unit	23
		2.3.5 Power Unit	27
		2.3.6 Frame Memory	31
		2.3.7 Localisation Unit	31
	2.4	Information Processing in WMSN	32
		2.4.1 Multi-Camera Network Models	32
		2.4.2 Collaborative Object Detection, Tracking	
		and Recognition	33
		2.4.3 Information Reduction in WMSN	35
	2.5	Applications of WMSNs	37
	2.6	Chapter Summary	38
3	Hard	lware Technology and Programming Languages	
	for R	Reconfigurable Devices	39
	3.1	Introduction	39
	3.2	Hardware Technology for Reconfigurable Hardware	40
		3.2.1 System-Level Architectures	41
		3.2.2 Reconfigurable-Level Models	43

		3.2.3	Functional Block Architectures	46
		3.2.4	Soft-Core Microprocessor Architectures	52
	3.3	Progra	amming Languages for Reconfigurable Devices	53
		3.3.1	Hardware Description Languages (HDLs)	54
		3.3.2	HDL Design Flow	54
		3.3.3	HDL Abstraction Models	56
		3.3.4	Advantages of HDLs	57
		3.3.5	Examples of HDLs	58
	3.4	Chapt	er Summary	68
4	<b>FPG</b>	A Wire	less Multimedia Sensor Node Hardware Platforms	69
	4.1	Introd	uction	69
	4.2	WMS	N Hardware Platforms	71
		4.2.1	Low-Cost WMSN Platform Using Celoxica RC10	72
		4.2.2	Medium-Cost WMSN Platform Using Celoxica	
			RC203E	73
		4.2.3	Digi XBee ZB Zigbee Wireless Module	74
		4.2.4	Platform Architecture	75
		4.2.5	Memory Architecture	75
	4.3	WMS	N Processor Architecture	77
		4.3.1	Structure of a MIPS Microprocessor and Customisations	77
		4.3.2	Strip-Based MIPS Processor Architecture	80
	4.4	Discre	ete Wavelet Transform and Handel-C Implementation	90
		4.4.1	Lifting-Based DWT	91
		4.4.2	Hardware Architecture for DWT	94
		4.4.3	Stage 0: Data Copy	94
		4.4.4	Stage 1: Discrete Wavelet Transform	94
	4.5	Hardv	vare Platform Implementations	102
	4.6	Chapt	er Summary	102
5	Singl	e-View	Information Reduction Techniques for WMSN	
	Using	g Event	Detection	105
	5.1	Introd	uction	105
	5.2	Comp	utational Visual Attention and Models	108
		5.2.1	High-Level and Low-Level Features	108
		5.2.2	Bottom-Up and Top-Down Approaches	108
		5.2.3	Centre-Surround Process	109
		5.2.4	Saliency Map	110
		5.2.5	Visual Attention Models	111
	5.3	Low-O	Complexity and Low-Memory VA Model	122
		5.3.1	Integer-Based MSF Model for Hardware	
			Implementation	123
		5.3.2	Lowering Memory Requirements Through	
			Strip-Based Processing	125
	5.4	Hardv	vare Implementation on the WMSN Platform	129
		5.4.1	Stages 0 and 1: Data Copy and DWT	129
		5.4.2	Stage 2: Feature Emphasis	129

		5.4.3 Stage 3: Feature Combination	135
		5.4.4 Stage 4: Upsampling and Across Level Combination	136
		5.4.5 Stage 5: Salient Pixel Computation	145
		5.4.6 Stage 6: Information Reduction Using Salient Patches	146
	5.5	Hardware Setup and Results	152
	5.6	Chapter Summary	156
6	Singl	e-View Information Reduction Techniques for WMSN	
	Using	g Event Compression	159
	6.1	Introduction	159
	6.2	Visual Compression and Models	161
		6.2.1 Spatial and Temporal Redundancy	161
		6.2.2 Lossy and Lossless Compression	162
		6.2.3 Evaluation of Image Quality	162
		6.2.4 Image Compression Models	163
	6.3	SPIHT Coding with Improvements	176
		6.3.1 Low-Memory Implementation of SPIHT Coding	177
		6.3.2 Modified SPIHT Algorithm	184
		6.3.3 Listless SPIHT-ZTR Coding	190
	6.4	Hardware Implementation on the WMSN Platform	193
		6.4.1 Stages 0 and 1: Data Copy and DWT	195
		6.4.2 Stage 2: Upward Scanning Significance Data Collection	196
		6.4.3 Stage 3: Downward Scanning Listless	
		SPIHT-ZTR Coding	198
	6.5	Hardware Setup and Results	198
	6.6	Chapter Summary	206
7	Mult	iple-View Information Reduction Techniques	
	for W	WMSN Using Image Stitching	207
	7.1	Introduction	207
	7.2	Joint-Sources Compression	208
		7.2.1 Slepian–Wolf and Wyner–Ziv Theorems	210
		7.2.2 Collaborative Correspondence Analysis	213
		7.2.3 Comparison of Joint-Sources Compression	214
	7.3	Feature Extraction	215
		7.3.1 Harris Corner Detector	215
		7.3.2 Harris–Laplace Detector	216
		7.3.3 Laplacian-of-Gaussian (LoG) Detector	216
		7.3.4 Features from Accelerated Segment Test (FAST)	
		Detector	217
		7.3.5 Scale Invariant Feature Transform (SIFT)	217
		7.3.6 Comparison of Feature Extraction Methods	218
	7.4	Overview of Image Stitching	219
		7.4.1 Feature Points Descriptor and Image Matching	220
		7.4.2 Transformation Parameters and Image Stitching	221
		7.4.3 Post-Processing	222

	7.5	Analysis of Feature Extraction Methods on Subsampled Images	223
		7.5.1 Minimum Resolution of Subsampled Images	223
		7.5.2 Number of Feature Points	224
	7.6	Proposed Framework	226
		7.6.1 Stage 1: Send Images to Aggregation Node	228
		7.6.2 Stage 2: Correspondence Analysis and Image Stitching	229
		7.6.3 Stage 3: Generate Data for Visual Nodes	229
		7.6.4 Stage 4: Discard the Overlapping Regions	233
		7.6.5 One-Pass Downward Scanning SPIHT Coding	233
	7.7	Simulation Results	239
		7.7.1 Relationship Between Overlapping Regions	
		and Number of Output Bits	240
	7.8	Hardware Implementation	241
	7.9	Experimental Results	243
	7.10	Chapter Summary	247
Α	Appe	ndix	249
Re	ferenc	es	271
Ine	Index		

# List of Figures

Fig. 2.1	Typical WMSN layout	7
Fig. 2.2	General structure of a WMSN	8
Fig. 2.3	Multi-hop homogeneous flat network architecture	10
Fig. 2.4	Hierarchical single-tier single-hop network architecture	11
Fig. 2.5	Hierarchical single-tier multi-hop network architecture	11
Fig. 2.6	Hierarchical multi-tier multi-hop architecture	11
Fig. 2.7	State diagram for Waspmote operational modes	13
Fig. 2.8	Components of a typical WSN node	14
Fig. 2.9	A typical CMOS sensor arrangement (Bayer pattern filter)	16
Fig. 2.10	Front-illuminated vs. back-illuminated CMOS sensor	17
Fig. 2.11	The ECM microphone (foil type or diaphragm type)	
	(a) Photo of ECM. (b) Cross-section of ECM	18
Fig. 2.12	Processor unit	19
Fig. 2.13	Different memory types	21
Fig. 2.14	A six-transistor CMOS SRAM	22
Fig. 2.15	Communication types	24
Fig. 2.16	ZigBee layers and specifications	26
Fig. 2.17	ZigBee network topologies	30
Fig. 2.18	Position calculation using angle-of-arrival	32
Fig. 2.19	Multi-camera network models	33
Fig. 2.20	General model for background subtraction	34
Fig. 3.1	WSN reconfigurable configurations	41
Fig. 3.2	Reconfigurable configuration for embedded processor.	42
Fig. 3.3	Single-context reconfigurable model.	44
Fig. 3.4	Multi-context reconfigurable model.	44
Fig. 3.5	Partial reconfigurable model.	45
Fig. 3.6	Pipeline reconfiguration model	45
Fig. 3.7	Overview of a FPGA architecture.	47
Fig. 3.8	Xilinx Spartan-3 architecture.	47
Fig. 3.9	Arrangement of Slices with the CLB	48

Fig. 3.10	Xilinx Spartan-3 slice structure.	49
Fig. 3.11	Altera Stratix II FPGA architecture.	50
Fig. 3.12	Altera Stratix II ALM structure.	51
Fig. 3.13	Functional block architecture for ALU array	51
Fig. 3.14	Functional block architecture for processor array	52
Fig. 3.15	Xilinx MicroBlaze soft-core processor architecture.	53
Fig. 3.16	General design flow using hardware description language	55
Fig. 3.17	Abstraction levels of a hardware description language	56
Fig. 3.18	Sequential and parallelism in Handel-C.	66
Fig. 3.19	C-to-FPGA design flow	67
Fig. 4.1	Overview of the Celoxica RC10 FPGA board	72
Fig. 4.2	Overview of the Celoxica RC203E FPGA board	73
Fig. 4.3	Overview of the Digi Xbee ZigBee mesh	
C	development kit	74
Fig. 4.4	Hardware platform architecture for the RC10 WMSN	75
Fig. 4.5	Illustration of the STRIP RAM with its partitions	76
Fig. 4.6	Simplified architecture for a standard five-stage	
	pipelined MIPS processor	77
Fig. 4.7	Datapath design for strip-based MIPS processor	83
Fig. 4.8	IF datapath for strip-based MIPS processor	84
Fig. 4.9	ID datapath for strip-based MIPS processor	85
Fig. 4.10	Address branching unit in the ID stage	86
Fig. 4.11	EXMEM datapath for strip-based MIPS processor	88
Fig. 4.12	WB datapath for strip-based MIPS processor	89
Fig. 4.13	Hardware architecture for the lifting-based 5/3 DWT	92
Fig. 4.14	Symmetric extension through reflection for row	
	filtering and column filtering	97
Fig. 4.15	Arrangements of DWT coefficients	
	in the STRIP_RAM—1D DWT. (a) 2-D DWT	
	arrangement (level 3). (b) Desired 1-D DWT	
	arrangement in STRIP_RAM	100
Fig. 4.16	Arrangements of DWT coefficients	
	in the STRIP_RAM—lifting DWT. (c1) Lifting-based	
	DWT filter output (level 1). $(c2)$ 1-D DWT	
	arrangement (level 1). (d1) Lifting-based DWT filter	
	output (level 2). ( <b>d2</b> ) 1-D DWT arrangement (level 2).	
	(e1) Lifting-based DWT filter output (level 3). (e2) 1-D	
	DWT arrangement (level 3)	101
Fig. 5.1	Examples of visual salience caused by low-level	
	features	109
Fig. 5.2	Centre-surround process using the sliding window	
	method	110
Fig. 5.3	Input image for VA processing and its saliency map	111

Fig. 5.4	Visual comparison of saliency maps for VA models	
	using simple scene images	119
Fig. 5.5	Visual comparison of saliency maps for VA models	
	using complex scene images	121
Fig. 5.6	An overview of the integer-based MSF	123
Fig. 5.7	Diamond-structured filter used in the CS process	
-	of the MSF 5/3 VA model	125
Fig. 5.8	Strip-based processing approach applied to VA model	126
Fig. 5.9	Visual comparison of saliency maps for various strip sizes	128
Fig. 5.10	Computing the CS filter start address	135
Fig. 5.11	Feature combination of orientation sub-band maps	138
Fig. 5.12	Four neighbourhood averaging in the upsampling method	139
Fig. 5.13	Obtaining image patches from the captured image	146
Fig. 5.14	Overview of information reduction using salient patches	150
Fig. 5.15	Hardware setup for VA implementation	154
Fig. 5.16	Data reduced images that are captured, processed	
•	and transmitted by the WMSN	155
$\mathbf{E} = \mathbf{C} 1$		161
Fig. $0.1$	Two of finance compression process	101
Fig. $0.2$	Pagaling IPEC Compression and Decompression	105
Fig. $0.5$	Baseline JPEG—Compression and Decompression	104
F1g. 0.4	when the structure and parent-children dependencies of	166
Eig 65	Sub-Dands III EZW couling	167
Fig. 0.3	Prior chart lof EZW couling	167
Fig. $0.0$	IDEC 2000 compression	100
Fig. 0.7	FEC 2000 compression	171
Fig. 0.0	SDECV goding methodology	172
Fig. $0.9$	Broass of pyramidal anding (a) Original image	175
Fig. 0.10	Lenna (b) Gaussian pyramid image (c) Gaussian	
	interpolation image (d) Lonlogion pyramid image	174
Eig 6 11	Drogoes for segmentation based adding	174
Fig. $0.11$	SDILT adding in STDID DUEEED	170
Fig. $0.12$	New spatial orientation tree structures	1/0
Fig. $0.15$	SOT Degree 1.2 and 3	100
Fig. $0.14$	Two combinations in modified SDIHT algorithm	104
Fig. $0.15$	Listless modified SDIHT for strin based	105
Fig. 0.10	implementation sorting and refinement	101
Fig. 6.17	Listless modified SDIHT for strip based	191
Fig. 0.17	implementation Combi 1	102
Fig = 6.18	Listless modified SDIHT for strip based	192
Fig. 0.18	implementation Combi 2	103
Fig. 6.10	Hardware architecture of the proposed strip based	193
1 1g. 0.19	image coder	10/
Fig. 6.20	Architecture for SPIHT-7TR encoder module	105
1 1g. 0.20		175

Fig. 6.21	Wavelet coefficients arrangement in STRIP_BUFFER	195
Fig. 6.22	Significant coefficient at each bit-plane	
	in the STRIP_BUFFER	196
Fig. 6.23	Visual compression experimental setup	202
Fig. 6.24	Visual compression back-end processing	203
Fig. 6.25	Results of visual compression (outdoor)	204
Fig. 6.26	Results of visual compression (indoor)	205
Fig. 7.1	The effect of applying image stitching to images	
	captured by two image sensors	209
Fig. 7.2	(a) The encoding of $X$ with $Y$ present at both encoder	
	and decoder. (b) The encoding of $X$ with $Y$ only	
	present at the decoder	211
Fig. 7.3	Three-bit input can form eight codewords, and these	
	eight codewords can be separated into four different	
	cosets	211
Fig. 7.4	DCT step sizes	213
Fig. 7.5	Multiview visual node setup	214
Fig. 7.6	The Gaussian scale-space representation	216
Fig. 7.7	The Difference-of-Gaussian (DoG)	217
Fig. 7.8	The computation process of the DoG adopted in SIFT	218
Fig. 7.9	SIFT candidate point and its neighbours	218
Fig. 7.10	Image stitching steps	220
Fig. 7.11	RANSAC line estimation	222
Fig. 7.12	Number of feature points extracted from Image	
	A and B of Set 1–4	227
Fig. 7.13	Four stage WMSN information reduction	228
Fig. 7.14	Distribution of wavelet coefficients at different	
	decomposition levels	229
Fig. 7.15	Identification of overlapping regions	230
Fig. 7.16	Efficiency of SPHIT coding—effects of high-frequency	
	components	232
Fig. 7.17	Binary map and tree pruning data	233
Fig. 7.18	Single-pass downward scanning SPHIT coding flowchart	236
Fig. 7.19	Single-pass SPHIT subroutines	237
Fig. 7.20	Single-pass SPHIT subroutines—DESC significance	
	determination	238
Fig. 7.21	Single-pass SPHIT subroutines—GDESC significance	
	determination	239
Fig. 7.22	Modified MIPS with tree pruning	242
Fig. 7.23	Hardware experiment setup	244
Fig. 7.24	Sample hardware stitching result	245
Fig. 7.25	Sample binary maps for stitching	246
Fig. 7.26	Result of number of mapping and refinement bits	
	received from two visual nodes	247

### List of Tables

Table 2.1	Comparison of mote platforms	12
Table 2.2	Operational modes for Waspmote	13
Table 2.3	SHT1x, 2x and 7x series of humidity sensors from Sensirion	15
Table 2.4	Comparison of NAND and NOR flash memory	
	operating specifications	23
Table 2.5	Comparison of RF communication standards	24
Table 2.6	ZigBee PHY layer IEEE 802.15.4 specifications,	
	2003–2012	28
Table 2.7	ZigBee and 802.15.4 network node types	30
Table 3.1	Resource differences between Spartan-3 FPGA	
	and Spartan-6 FPGA	49
Table 3.2	Comparison of Xilinx MicroBlaze and Altera Nios II	
	soft-core processors	54
Table 3.3	VHDL built-in data operators	59
Table 3.4	Verilog built-in data operators	60
Table 3.5	Comparison of SystemC and SpecC in terms	
	of design modelling	63
Table 3.6	Handel-C data types	64
Table 3.7	Handel-C operators	65
Table 4.1	The structure of the MIPS instruction code	
	in R-format, I-format and J-format	78
Table 4.2	Extended instruction set for strip-based MIPS processor	81
Table 4.3	Extended instruction set for strip-based MIPS processor	81
Table 4.4	Machine code for R-format instructions	82
Table 4.5	Machine code for I-format instructions	82
Table 4.6	List of instruction opcodes and their control signals	90
Table 4.7	Description and function of major control signals	90
Table 4.8	New address calculations of DWT coefficients	
	to be rearranged in STRIP_RAM	102

Table 4.9	Hardware platform summary for Celoxica RC10 WMSN hardware platform	103
Table 5.1	Memory requirements against the number of strips for the MSF 5/3 implementation	127
Table 5.2	Number of MIPS instructions and clock cycles for visual attention data reduction	156
Table 6.1	Prediction functions in lossless JPEG	164
Table 6.2	Tree structure	179
Table 6.3	Parent-children relationship of the original	
	and the proposed new spatial orientation tree (SOT)	
	structures for a three-scale SOT decomposition.	
	Parent node is at coordinate $(i, j)$ and its first	101
Tabla 6 1	descendant node is at coordinate $(x, y)$	181
Table 6.5	The perceptage (%) of occurrence of possible	165
	outcomes of the $SIG(k, l)$ and $DESC(k, l)$	
	bits for various standard greyscale test images	
	of size $512 \times 512$ pixels under Combination 1,	
	DESC(i, j) = 1 and $GDESC(i, j) = 1$ . Node $(i, j)$	
	is the root node and $(k, l)$ is the offspring of $(i, j)$	186
Table 6.6	The percentage (%) of occurrence of possible	
	outcomes of the ABCD for various standard	
	greyscale test images of size $512 \times 512$ pixels under Combination 2. DESC( <i>i</i> , <i>i</i> ) = 1 and	
	GDESC(i, j) = 0 ABCD refers to the significance	
	of the four offspring of node $(i, j)$	187
Table 6.7	Performance of modified SPHIT (Deg-0)	190
Table 7.1	Comparison of different approaches used for feature	
	extraction	219
Table 7.2	Object transformations and their parameters	221
Table 7.3	Stitching test sets	224
Table 7.4	Definition of stitching quality	225
Table 7.5	The evaluation results of using the subsampled	226
$T_{a}$ bla 7 6	Images for stitching	226
14010 7.0	the proposed framework to the first frame of video	
	sequence "Ballroom" and "Vassar"	240
Table 7.7	The percentage of overlap (%) and the reduction	
	in number of bits that are required to transmit	
	the non-overlapping region	241
Table 7.8	New address calculation rules	242
Table 7.9	Number of MIPS instructions used to process	
	the image data	243

xviii

Table 7.10	Total number of clock cycles required to encode	
	all the 16 strips of an image frame	243
Table 7.11	Resources utilisation of the soft-core processor	244
Table 7.12	Battery lifespan	246

## Acronyms

AIM	Attention based on information maximization
CS	Center surround
DWT	Discrete wavelet transform
EX	Instruction execution
EXMEM	Instruction execution and memory access
FOV	Field of view
FPGA	Field-programmable gate array
ID	Instruction decode
IF	Instruction fetch
MCH	Multimedia cluster head
MEM	Instruction memory access
MIPS	Microprocessor without interlocked pipeline stages
MSB	Most-significant bit
MSF	Medium spatial frequencies
NCC	Normalized cross-correlation
RAM	Random-access memory
RANSAC	Random sample consensus
SAD	Sum of absolute difference
SIFT	Shift invariant feature transform
SIG	Significant
SOT	Spatial orientation tree
SPIHT	Set partitioning in hierarchical trees
SSD	Sum of square difference
SW	Slepian–Wolf
VA	Visual attention
WB	Instruction write back
WBSME	Wavelet-based saliency map estimator
WMN	Wireless multimedia node
WMSN	Wireless multimedia sensor network
WSN	Wireless sensor network
WZ	Wyner-Ziv