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Digital Signal Processing with Field Programmable Gate Arrays

Fourth Edition

 Springer

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CD-ROM material found at <https://extras.springer.com/2014/978-3-642-45308-3/>.

ISSN 1860-4862 ISSN 1860-4870 (electronic)
ISBN 978-3-642-45308-3 ISBN 978-3-642-45309-0 (eBook)
DOI 10.1007/978-3-642-45309-0
Springer Heidelberg New York Dordrecht London

Library of Congress Control Number: 2014939295

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To

Anke, Lisa, and my Parents

Preface to First Edition

Field-programmable gate arrays (FPGAs) are on the verge of revolutionizing digital signal processing in the manner that programmable digital signal processors (PDSPs) did nearly two decades ago. Many front-end digital signal processing (DSP) algorithms, such as FFTs, FIR or IIR filters, to name just a few, previously built with ASICs or PDSPs, are now most often replaced by FPGAs. Modern FPGA families provide DSP arithmetic support with fast-carry chains (Xilinx Virtex, Altera FLEX) that are used to implement multiply-accumulates (MACs) at high speed, with low overhead and low costs [1]. Previous FPGA families have most often targeted TTL “glue logic” and did not have the high gate count needed for DSP functions. The efficient implementation of these front-end algorithms is the main goal of this book.

At the beginning of the twenty-first century we find that the two programmable logic device (PLD) market leaders (Altera and Xilinx) both report revenues greater than US\$1 billion. FPGAs have enjoyed steady growth of more than 20% in the last decade, outperforming ASICs and PDSPs by 10%. This comes from the fact that FPGAs have many features in common with ASICs, such as reduction in size, weight, and power dissipation, higher throughput, better security against unauthorized copies, reduced device and inventory cost, and reduced board test costs, and claim advantages over ASICs, such as a reduction in development time (rapid prototyping), in-circuit reprogrammability, lower NRE costs, resulting in more economical designs for solutions requiring less than 1000 units. Compared with PDSPs, FPGA design typically exploits parallelism, e.g., implementing multiple multiply-accumulate calls efficiently, e.g., zero product-terms are removed, and pipelining, i.e., each LE has a register, therefore pipelining requires no additional resources.

Another trend in the DSP hardware design world is the migration from graphical design entries to hardware description language (HDL). Although many DSP algorithms can be described with “signal flow graphs,” it has been found that “code reuse” is much higher with HDL-based entries than with graphical design entries. There is a high demand for HDL design engineers and we already find undergraduate classes about logic design with HDLs [2]. Unfortunately *two* HDL languages are popular today. The US west coast and

Asia area prefer Verilog, while US east coast and Europe more frequently use VHDL. For DSP with FPGAs both languages seem to be well suited, although some VHDL examples are a little easier to read because of the supported signed arithmetic and multiply/divide operations in the IEEE VHDL 1076-1987 and 1076-1993 standards. The gap is expected to disappear after approval of the Verilog IEEE standard 1364-1999, as it also includes signed arithmetic. Other constraints may include personal preferences, EDA library and tool availability, data types, readability, capability, and language extensions using PLIs, as well as commercial, business, and marketing issues, to name just a few [3]. Tool providers acknowledge today that both languages have to be supported and this book covers examples in both design languages.

We are now also in the fortunate situation that “baseline” HDL compilers are available from different sources at essentially no cost for educational use. We take advantage of this fact in this book. It includes a CD-ROM with Altera’s newest **MaxPlusII** software, which provides a complete set of design tools, from a content-sensitive editor, compiler, and simulator, to a bitstream generator. All examples presented are written in VHDL and Verilog and should be easily adapted to other propriety design-entry systems. Xilinx’s “Foundation Series,” ModelTech’s ModelSim compiler, and Synopsys FC2 or FPGA Compiler should work without any changes in the VHDL or Verilog code.

The book is structured as follows. The first chapter starts with a snapshot of today’s FPGA technology, and the devices and tools used to design state-of-the-art DSP systems. It also includes a detailed case study of a frequency synthesizer, including compilation steps, simulation, performance evaluation, power estimation, and floor planning. This case study is the basis for more than 30 other design examples in subsequent chapters. The second chapter focuses on the computer arithmetic aspects, which include possible number representations for DSP FPGA algorithms as well as implementation of basic building blocks, such as adders, multipliers, or sum-of-product computations. At the end of the chapter we discuss two very useful computer arithmetic concepts for FPGAs: distributed arithmetic (DA) and the CORDIC algorithm. Chapters 3 and 4 deal with theory and implementation of FIR and IIR filters. We will review how to determine filter coefficients and discuss possible implementations optimized for size or speed. Chapter 5 covers many concepts used in multirate digital signal processing systems, such as decimation, interpolation, and filter banks. At the end of Chap. 5 we discuss the various possibilities for implementing wavelet processors with two-channel filter banks. In Chap. 6, implementation of the most important DFT and FFT algorithms is discussed. These include Rader, chirp- z , and Goertzel DFT algorithms, as well as Cooley–Tuckey, Good–Thomas, and Winograd FFT algorithms. In Chap. 7 we discuss more specialized algorithms, which seem to have great potential for improved FPGA implementation when compared with PDSPs. These algorithms include number theoretic transforms, algorithms for cryp-

tography and errorcorrection, and communication system implementations. The appendix includes an overview of the VHDL and Verilog languages, the examples in Verilog HDL, and a short introduction to the utility programs included on the CD-ROM.

Acknowledgements. This book is based on an FPGA communications system design class I taught for four years at the Darmstadt University of Technology; my previous (German) books [4,5]; and more than 60 Masters thesis projects I have supervised in the last 10 years at Darmstadt University of Technology and the University of Florida at Gainesville. I wish to thank all my colleagues who helped me with critical discussions in the lab and at conferences. Special thanks to: M. Acheroy, D. Achilles, F. Bock, C. Burrus, D. Chester, D. Childers, J. Conway, R. Crochiere, K. Damm, B. Delgutte, A. Dempster, C. Dick, P. Duhamel, A. Drolshagen, W. Endres, H. Eveking, S. Foo, R. Games, A. Garcia, O. Ghitza, B. Harvey, W. Hilberg, W. Jenkins, A. Laine, R. Laur, J. Mangen, J. Massey, J. McClellan, F. Ohl, S. Orr, R. Perry, J. Ramirez, H. Scheich, H. Scheid, M. Schroeder, D. Schulz, F. Simons, M. Soderstrand, S. Stearns, P. Vaidyanathan, M. Vetterli, H. Walter, and J. Wietzke.

I would like to thank my students for the innumerable hours they have spent implementing my FPGA design ideas. Special thanks to: D. Abdolrahimi, E. Allmann, B. Annamaier, R. Bach, C. Brandt, M. Brauner, R. Bug, J. Burros, M. Burschel, H. Diehl, V. Dierkes, A. Dietrich, S. Dworak, W. Fieber, J. Guyot, T. Hattermann, T. Häuser, H. Hausmann, D. Herold, T. Heute, J. Hill, A. Hundt, R. Huthmann, T. Irmeler, M. Katzenberger, S. Kenne, S. Kerkmann, V. Kleipa, M. Koch, T. Krüger, H. Leitel, J. Maier, A. Noll, T. Podzimek, W. Praefcke, R. Resch, M. Rösch, C. Scheerer, R. Schimpf, B. Schlanske, J. Schleichert, H. Schmitt, P. Schreiner, T. Schubert, D. Schulz, A. Schuppert, O. Six, O. Spiess, O. Tamm, W. Trautmann, S. Ullrich, R. Watzel, H. Wech, S. Wolf, T. Wolf, and F. Zahn.

For the English revision I wish to thank my wife Dr. Anke Meyer-Bäse, Dr. J. Harris, Dr. Fred Taylor from the University of Florida at Gainesville, and Paul DeGroot from Springer.

For financial support I would like to thank the DAAD, DFG, the European Space Agency, and the Max Kade Foundation.

If you find any errata or have any suggestions to improve this book, please contact me at Uwe.Meyer-Baese@ieee.org or through my publisher.

Tallahassee, May 2001

Uwe Meyer-Bäse

Preface to Second Edition

A new edition of a book is always a good opportunity to keep up with the latest developments in the field and to correct some errors in previous editions. To do so, I have done the following for this second edition:

- Set up a web page for the book at the following URL:
www.eng.fsu.edu/~umb
The site has additional information on DSP with FPGAs, useful links, and additional support for your designs, such as code generators and extra documentation.
- Corrected the mistakes from the first edition. The errata for the first edition can be downloaded from the book web page.
- A total of approximately 100 pages have been added to the new edition. The major new topics are:
 - The design of serial and array dividers
 - The description of a complete floating-point library
 - A new Chap. 8 on adaptive filter design
- Altera's current student version has been updated from 9.23 to 10.2 and all design examples, size and performance measurements, i.e., many tables and plots have been compiled for the EPF10K70RC240-4 device that is on Altera's university board UP2. Altera's UP1 board with the EPF10K20RC240-4 has been discontinued.
- A solution manual for the first edition (with more than 65 exercises and over 33 additional design examples) is available from Amazon. Some additional (over 25) new homework exercises are included in the second edition.

Acknowledgements. I would like to thank my colleagues and students for the feedback to the first edition. It helped me to improve the book. Special thanks to: P. Ashenden, P. Athanas, D. Belc, H. Butterweck, S. Connors, G. Coutu, P. Costa, J. Hamblen, M. Horne, D. Hyde, W. Li, S. Lowe, H. Natarajan, S. Rao, M. Rupp, T. Sexton, D. Sunkara, P. Tomaszewicz, F. Verahrami, and Y. Yunhua.

From Altera, I would like to thank B. Esposito, J. Hanson, R. Maroccia, T. Mossadak, and A. Acevedo (now with Xilinx) for software and hardware support and the permission to include datasheets and MaxPlus II on the CD of this book.

From my publisher (Springer-Verlag) I would like to thank P. Jantzen, F. Holzwarth, and Dr. Merkle for their continuous support and help over recent years.

I feel excited that the first edition was a big success and sold out quickly. I hope you will find this new edition even more useful. I would also be grateful, if you have any suggestions for how to improve the book, if you would e-mail me at Uwe.Meyer-Baese@ieee.org or contact me through my publisher.

Tallahassee, October 2003

Uwe Meyer-Bäse

Preface to Third Edition

Since FPGAs are still a rapidly evolving field, I am very pleased that my publisher Springer Verlag gave me the opportunity to include new developments in the FPGA field in this third edition. A total of over 150 pages of new ideas and current design methods have been added. You should find the following innovations in this third edition:

- 1) Many FPGAs now include embedded 18×18 -bit multipliers and it is therefore recommended to use these devices for DSP-centered applications since an embedded multiplier will save many LEs. The Cyclone II EP2C35F672C6 device for instance, used in all the examples in this edition, has 35 18×18 -bit multipliers.
- 2) MaxPlus II software is no longer updated and new devices such as the Stratix or Cyclone are only supported in Quartus II. All old and new examples in the book are now compiled with Quartus 6.0 for the Cyclone II EP2C35F672C6 device. Starting with Quartus II 6.0 integers are by default initialized with the smallest negative number (similar to with the ModelSim simulator) rather than zero and the verbatim 2/e examples will therefore not work with Quartus II 6.0. Tcl scripts are provided that allow the evaluation of all examples with other devices too. Since downloading Quartus II can take a long time the book CD includes the web version 6.0 used in the book.
- 3) The new device features now also allow designs that use many MAC calls. We have included a new section (2.9) on MAC-based function approximation for trigonometric, exponential, logarithmic, and square root.
- 4) To shorten the time to market further FPGA vendors offer intellectual property (IP) cores that can be easily included in the design project. We explain the use of IP blocks for NCOs, FIR filters, and FFTs.
- 5) Arbitrary sampling rate change is a frequent problem in multirate systems and we describe in Sect. 5.6 several options including B-spline, MOMS, and Farrow-type converter designs.
- 6) FPGA-based microprocessors have become an important IP block for FPGA vendors. Although they do not have the high performance of a custom algorithm design, the software implementation of an algorithm with a μ P usually needs much less resources. A complete new chapter (9) covers many aspects from software tool to hard- and softcore μ Ps. A

complete example processor with an assembler and C compiler is developed.

- 7) A total of 107 additional problems have been added and a solution manual will be available later from www.amazon.com at a not-for-profit price.
- 8) Finally a special thank you goes to Harvey Hamel who discovered many errors that have been summarized in the errata for 2/e that is posted at the book homepage

Acknowledgements. Again many colleagues and students have helped me with related discussions and feedback to the second edition, which helped me to improve the book. Special thanks to:

P. Athanas, M. Bolic, C. Bentancourth, A. Canosa, S. Canosa, C. Chang, J. Chen, T. Chen, J. Choi, A. Comba, S. Connors, J. Coutu, A. Dempster, A. Elwakil, T. Felderhoff, O. Gustafsson, J. Hallman, H. Hamel, S. Hashim, A. Hoover, M. Karlsson, K. Khanachandani, E. Kim, S. Kulkarni, K. Lenk, E. Manolakos, F. Mirzapour, S. Mitra, W. Moreno, D. Murphy, T. Meißner, K. Nayak, H. Ningxin, F. von Münchow-Pohl, H. Quach, S. Rao, S. Stepanov, C. Suslowicz, M. Unser, J. Vega-Pineda, T. Zeh, E. Zurek

I am particular thankful to P. Thévenaz from EPFL for help with the newest developments in arbitrary sampling rate changers.

My colleagues from the ISS at RHTH Aachen I would like to thank for their time and efforts to teach me LISA during my Humboldt award sponsored summer research stay in Germany. Special thanks go to H. Meyr, G. Ascheid, R. Leupers, D. Kammler, and M. Witte.

From Altera, I would like to thank B. Esposito, R. Maroccia, and M. Phipps for software and hardware support and permission to include datasheets and Quartus II software on the CD of this book. From Xilinx I like to thank for software and hardware support of my NSF CCLI project J. Weintraub, A. Acevedo, A. Vera, M. Pattichis, C. Sepulveda, and C. Dick.

From my publisher (Springer-Verlag) I would like to thank Dr. Baumann, Dr. Merkle, M. Hanich, and C. Wolf for the opportunity to produce an even more useful third edition.

I would be very grateful if you have any suggestions for how to improve the book and would appreciate an e-mail to Uwe.Meyer-Baese@ieee.org or through my publisher.

Tallahassee, May 2007

Uwe Meyer-Bäse

Preface to Fourth Edition

In recent years FPGAs have increased in complexity so that we can now build large DSP systems with a single FPGA. Modern devices now have hundreds of embedded multipliers and large on-chip memories. Since the previous books were written mainly to optimize the size of the design, system design questions now become more important. A good study of such issues can be carried out with larger tasks such as PCA or ICA algorithms, image and video processing systems, or a new 256-point FFT design discussed in this edition. A total of over 150 pages – including 11 new system designs ideas – have been added to this new edition, some requiring more than 100 embedded multipliers. You should find the following innovations in this fourth edition:

- 1) Simulation in HDL in the book is now done with the powerful MODEL-SIM simulator for Altera devices and the ISIM simulator for the Xilinx designs.
- 2) For the system designs many test bench data are now provided using MATLAB or SIMULINK.
- 3) System level designs using the VHDL-2008 new fixed-point and floating-point IEEE libraries are introduced.
- 4) All-pass IIR filter designs in direct form, BiQuads, lattices, and wave digital filters are compared.
- 5) Independent component analysis (ICA) and principle component analysis (PCA) algorithms are implemented.
- 6) Speech and audio compression methods from A-law, ADPCM to MP3 are discussed and implemented in HDL.
- 7) Image processing algorithms for edge detection and median filtering using HDL and embedded microprocessors are discussed.
- 8) Video processing for motion compensation using microprocessors with custom instructions are discussed.
- 9) Plans exist to provide design examples for the SIMULINK toolbox from Altera and Xilinx as well as support for Xilinx ISE and ISIM simulation later as additional CDs available through www.amazon.com.
- 10) Updates and bug fix report will be posted at the author's webpage, that is, at the time of writing, at www.eng.fsu.edu/~umb

Acknowledgements. Again many colleagues helped me with related discussions and feedback to the third edition, which helped me to improve the book. Special thanks to:

R. Adhami, M. Abd-El-Hameed, C. Allen, S. Amalkar, A. Andrawis, G. Ascheid, P. Athanas, S. Badave, R. Badeau, S. Bald, A. Bardakcioglu, P. Bendixen, C. Betancourth, R. Bhakthavatchalu, G. Birkelbach, T. Borsodi, F. Casado, E. Castillo, O. Calvo, P. Cayuela, A. Celebi, C.-H. Chang, A. Chanerley, K. Chapman, I. Chiorescu, G. Connelly, S. Connors, J. Coutu, S. Cox, S. David, R. Deka, A. Dempster, J. Domingo, A. Elias, F. Engel, R. van Engelen, H. Fan, S. Foo, T. Fox, M. Frank, J. Gallagher, A. Garcia, M. Gerhardt, A. Ghalame, G. Glandon, S. Grunwald, A. Guerrero, W. Guolin, O. Gustafsson, H. Hamel, S. Hashim, S. Hedayat, D. Hodali, S. Hong, K. Huang, F. Iqbal, R. Jadhav, D. Jiang, D. Kammmler, K. Karuri, T. Knudsen, M. Koepnick, F. Koushanfar, M. Kumm, M. Krishna, H. LeFevre, R. Leupers, S. Liljeqvist, A. Littek, A. Lloris, M. Luqman, V. Madan, M. Manikandan, J. Mark, B. McKenzie, H. Meyr, P. Mishra, A. Mitra, I. Miu, J. Moorhead, S. Moradi, F. Munsche, Z. Navabi, L. Oniciuc, B. Parhami, S. Park, L. Parrilla, V. Pedroni, R. Pereira, R. Perry, A. Pierce, F. Poderico, G. Prinz, D. Raic, N. Rafla, S. Rao, N. Relia, F. Rice, D. Romero, D. Sarma, P. Sephra, W. Sheng, T. Taguchi, N. Trong, C. Unterrieder, G. Wall, G. Wang, Y. Wang, R. Wei, S. Weihua, J. Wu, J. Xu, O. Zavala-Romero, P. Zipf, D. Zhang, L. Zhang, M. Zhang,

Special thanks also to the students from my Spring EEL5722 DSP with FPGAs class. Thanks to Nick Stroupe for the DWT de-noising project work, Ye Yang for the LPC project work, Soumak Mookherjee for the 256-point FFT project, Naren Nagaraj for the all-pass filter project work, Venkata Pothavajhala for the BiQuad floating-point design, Haojun Yang for the lattice filter design project, and Crispin Odom for her ICA project and MS thesis work.

I am particular thankful to Guillermo Botella and Diego González from the University of Madrid for help with the image and video processing chapter.

Special thank also to David Bishop and Huibert Lincklaen Arriens for permission to include their libraries on the book CD.

From Altera, I would like to thank Ben Esposito, M. Phipps, Ralene Maroccia, Blair Fort, and Stephen Brown for software and hardware support. From Xilinx support I would like to thank A. Vera, M. Pattichis, Craig Kief, and Parimal Patel.

From my publisher (Springer-Verlag) I would like to thank Dr. Baumann, for his patience and the opportunity to update the book.

I would be very grateful if you have any suggestions on how to improve the book and would appreciate e-mail to Uwe.Meyer-Baese@ieee.org or through my publisher.

Tallahassee, January 2014

Uwe Meyer-Bäse

Contents

| | |
|---|------|
| Preface to First Edition | VII |
| Preface to Second Edition | XI |
| Preface to Third Edition | XIII |
| Preface to Fourth Edition | XV |
| 1. Introduction | 1 |
| 1.1 Overview of Digital Signal Processing (DSP) | 1 |
| 1.2 FPGA Technology | 3 |
| 1.2.1 Classification by Granularity | 3 |
| 1.2.2 Classification by Technology | 6 |
| 1.2.3 Benchmark for FPLs | 7 |
| 1.3 DSP Technology Requirements | 12 |
| 1.3.1 FPGA and Programmable Signal Processors | 14 |
| 1.4 Design Implementation | 15 |
| 1.4.1 FPGA Structure | 20 |
| 1.4.2 The Altera EP4CE115F29C7 | 23 |
| 1.4.3 Case Study: Frequency Synthesizer | 32 |
| 1.4.4 Design with Intellectual Property Cores | 40 |
| Exercises | 47 |
| 2. Computer Arithmetic | 57 |
| 2.1 Introduction | 57 |
| 2.2 Number Representation | 58 |
| 2.2.1 Fixed-Point Numbers | 58 |
| 2.2.2 Unconventional Fixed-Point Numbers | 61 |
| 2.2.3 Floating-Point Numbers | 75 |
| 2.3 Binary Adders | 79 |
| 2.3.1 Pipelined Adders | 81 |
| 2.3.2 Modulo Adders | 85 |
| 2.4 Binary Multipliers | 86 |
| 2.4.1 Multiplier Blocks | 89 |

| | | |
|-----------|--|------------|
| 2.5 | Binary Dividers | 93 |
| 2.5.1 | Linear Convergence Division Algorithms | 95 |
| 2.5.2 | Fast Divider Design..... | 100 |
| 2.5.3 | Array Divider | 105 |
| 2.6 | Fixed-Point Arithmetic Implementation | 106 |
| 2.7 | Floating-Point Arithmetic Implementation | 109 |
| 2.7.1 | Fixed-Point to Floating-Point Format Conversion..... | 110 |
| 2.7.2 | Floating-Point to Fixed-Point Format Conversion..... | 111 |
| 2.7.3 | Floating-Point Multiplication | 112 |
| 2.7.4 | Floating-Point Addition | 113 |
| 2.7.5 | Floating-Point Division | 115 |
| 2.7.6 | Floating-Point Reciprocal | 116 |
| 2.7.7 | Floating-Point Operation Synthesis | 118 |
| 2.7.8 | Floating-Point Synthesis Results | 122 |
| 2.8 | Multiply-Accumulator (MAC) and Sum of Product (SOP) .. | 124 |
| 2.8.1 | Distributed Arithmetic Fundamentals | 125 |
| 2.8.2 | Signed DA Systems | 129 |
| 2.8.3 | Modified DA Solutions | 130 |
| 2.9 | Computation of Special Functions Using CORDIC | 131 |
| 2.9.1 | CORDIC Architectures | 135 |
| 2.10 | Computation of Special Functions using MAC Calls..... | 141 |
| 2.10.1 | Chebyshev Approximations | 142 |
| 2.10.2 | Trigonometric Function Approximation | 143 |
| 2.10.3 | Exponential and Logarithmic Function Approximation | 152 |
| 2.10.4 | Square Root Function Approximation | 159 |
| 2.10 | Fast Magnitude Approximation | 165 |
| | Exercises | 168 |
| 3. | Finite Impulse Response (FIR) Digital Filters | 179 |
| 3.1 | Digital Filters | 179 |
| 3.2 | FIR Theory | 180 |
| 3.2.1 | FIR Filter with Transposed Structure | 181 |
| 3.2.2 | Symmetry in FIR Filters | 184 |
| 3.2.3 | Linear-phase FIR Filters | 185 |
| 3.3 | Designing FIR Filters | 187 |
| 3.3.1 | Direct Window Design Method..... | 187 |
| 3.3.2 | Equiripple Design Method | 190 |
| 3.4 | Constant Coefficient FIR Design | 192 |
| 3.4.1 | Direct FIR Design | 192 |
| 3.4.2 | FIR Filter with Transposed Structure | 196 |
| 3.4.3 | FIR Filters Using Distributed Arithmetic..... | 204 |
| 3.4.4 | IP Core FIR Filter Design | 215 |
| 3.4.5 | Comparison of DA- and RAG-Based FIR Filters | 217 |
| | Exercises | 219 |

| | |
|---|-----|
| 4. Infinite Impulse Response (IIR) Digital Filters | 225 |
| 4.1 IIR Theory | 228 |
| 4.2 IIR Coefficient Computation | 231 |
| 4.2.1 Summary of Important IIR Design Attributes | 233 |
| 4.3 IIR Filter Implementation | 234 |
| 4.3.1 Finite Wordlength Effects | 238 |
| 4.3.2 Optimization of the Filter Gain Factor | 239 |
| 4.4 Fast IIR Filter | 240 |
| 4.4.1 Time-domain Interleaving | 241 |
| 4.4.2 Clustered and Scattered Look-Ahead Pipelining | 243 |
| 4.4.3 IIR Decimator Design | 246 |
| 4.4.4 Parallel Processing | 246 |
| 4.4.5 IIR Design Using RNS | 250 |
| 4.5 Narrow Band IIR Filter | 250 |
| 4.5.1 Narrow Band Design Example | 251 |
| 4.5.2 Cascade Second Order Systems Narrow Band Filter Design | 259 |
| 4.5.3 Parallel Second Order Systems Narrow Band Filter Design | 263 |
| 4.5.4 Lattice Design of Narrow Band IIR Filter | 271 |
| 4.5.5 Wave Digital Filter Design of Narrow Band IIR Filter | 280 |
| 4.6 All-Pass Filter Design of Narrow Band IIR Filter | 287 |
| 4.6.1 All-Pass Wave Digital Filter Design of Narrow Band IIR Filter | 289 |
| 4.6.2 All-Pass Lattice Design of Narrow Band IIR Filter | 293 |
| 4.6.3 All-Pass Direct Form Design of Narrow Band Filter | 294 |
| 4.6.4 All-Pass Cascade BiQuad of Narrow Band Filter | 295 |
| 4.6.5 All-Pass Parallel BiQuad of Narrow Band Filter | 295 |
| Exercises | 299 |
| 5. Multirate Signal Processing | 305 |
| 5.1 Decimation and Interpolation | 305 |
| 5.1.1 Noble Identities | 306 |
| 5.1.2 Sampling Rate Conversion by Rational Factor | 308 |
| 5.2 Polyphase Decomposition | 309 |
| 5.2.1 Recursive IIR Decimator | 314 |
| 5.2.2 Fast-running FIR Filter | 315 |
| 5.3 Hogenauer CIC Filters | 317 |
| 5.3.1 Single-Stage CIC Case Study | 317 |
| 5.3.2 Multistage CIC Filter Theory | 320 |
| 5.3.3 Amplitude and Aliasing Distortion | 325 |
| 5.3.4 Hogenauer Pruning Theory | 328 |
| 5.3.5 CIC RNS Design | 333 |
| 5.3.6 CIC Compensation Filter Design | 334 |
| 5.4 Multistage Decimator | 337 |

| | | |
|-----------|---|------------|
| 5.4.1 | Multistage Decimator Design Using Goodman–Carey Half-Band Filters | 338 |
| 5.5 | Frequency-Sampling Filters as Bandpass Decimators | 341 |
| 5.6 | Design of Arbitrary Sampling Rate Converters | 345 |
| 5.6.1 | Fractional Delay Rate Change | 349 |
| 5.6.2 | Polynomial Fractional Delay Design | 356 |
| 5.6.3 | B-Spline-Based Fractional Rate Changer | 362 |
| 5.6.4 | MOMS Fractional Rate Changer | 366 |
| 5.7 | Filter Banks | 374 |
| 5.7.1 | Uniform DFT Filter Bank | 375 |
| 5.7.2 | Two-channel Filter Banks | 379 |
| 5.8 | Wavelets | 395 |
| 5.8.1 | The Discrete Wavelet Transformation | 398 |
| 5.8.2 | Discrete Wavelet Transformation Applications | 402 |
| | Exercises | 411 |
| 6. | Fourier Transforms | 417 |
| 6.1 | The Discrete Fourier Transform Algorithms | 418 |
| 6.1.1 | Fourier Transform Approximations Using the DFT ... | 418 |
| 6.1.2 | Properties of the DFT | 420 |
| 6.1.3 | The Goertzel Algorithm | 423 |
| 6.1.4 | The Bluestein Chirp- z Transform | 424 |
| 6.1.5 | The Rader Algorithm | 427 |
| 6.1.6 | The Winograd DFT Algorithm | 434 |
| 6.2 | The Fast Fourier Transform (FFT) Algorithms | 436 |
| 6.2.1 | The Cooley–Tukey FFT Algorithm | 437 |
| 6.2.2 | The Good–Thomas FFT Algorithm | 449 |
| 6.2.3 | The Winograd FFT Algorithm | 451 |
| 6.2.4 | Comparison of DFT and FFT Algorithms | 455 |
| 6.2.5 | IP Core FFT Design | 456 |
| 6.3 | Fourier-Related Transforms | 461 |
| 6.3.1 | Computing the DCT Using the DFT | 462 |
| 6.3.2 | Fast Direct DCT Implementation | 463 |
| | Exercises | 465 |
| 7. | Communication Systems | 475 |
| 7.1 | Error Control and Cryptography | 475 |
| 7.1.1 | Basic Concepts from Coding Theory | 476 |
| 7.1.2 | Block Codes | 482 |
| 7.1.3 | Convolutional Codes | 485 |
| 7.1.4 | Cryptography Algorithms for FPGAs | 494 |
| 7.2 | Modulation and Demodulation | 509 |
| 7.2.1 | Basic Modulation Concepts | 510 |
| 7.2.2 | Incoherent Demodulation | 515 |
| 7.2.3 | Coherent Demodulation | 521 |

| | |
|--|------------|
| Exercises | 529 |
| 8. Adaptive Systems | 533 |
| 8.1 Application of Adaptive Systems | 534 |
| 8.1.1 Interference Cancellation | 534 |
| 8.1.2 Prediction | 535 |
| 8.1.3 Inverse Modeling | 535 |
| 8.1.4 System Identification | 536 |
| 8.2 Optimum Estimation Techniques | 537 |
| 8.2.1 The Optimum Wiener Estimation | 540 |
| 8.3 The Widrow–Hoff Least Mean Square Algorithm | 544 |
| 8.3.1 Learning Curves | 551 |
| 8.3.2 Normalized LMS (NLMS) | 554 |
| 8.4 Transform Domain LMS Algorithms | 555 |
| 8.4.1 Fast-Convolution Techniques | 556 |
| 8.4.2 Using Orthogonal Transforms | 557 |
| 8.5 Implementation of the LMS Algorithm | 561 |
| 8.5.1 Quantization Effects | 561 |
| 8.5.2 FPGA Design of the LMS Algorithm | 561 |
| 8.5.3 Pipelined LMS Filters | 565 |
| 8.5.4 Transposed Form LMS Filter | 567 |
| 8.5.5 Design of DLMS Algorithms | 568 |
| 8.5.6 LMS Designs using SIGNUM Function | 572 |
| 8.6 Recursive Least Square Algorithms | 575 |
| 8.6.1 RLS with Finite Memory | 578 |
| 8.6.2 Fast RLS Kalman Implementation | 581 |
| 8.6.3 The Fast a Posteriori Kalman RLS Algorithm | 586 |
| 8.7 Comparison of LMS and RLS Parameters | 587 |
| 8.8 Principle Component Analysis (PCA) | 589 |
| 8.8.1 Principle Component Analysis Computation | 591 |
| 8.8.2 Implementation of Sanger’s GHA PCA | 595 |
| 8.9 Independent Component Analysis (ICA) | 601 |
| 8.9.1 Whitening and Orthogonalization | 603 |
| 8.9.2 Independent Component Analysis Algorithm | 604 |
| 8.9.3 Implementation of the EASI ICA Algorithm | 605 |
| 8.9.4 Alternative BSS Algorithms | 610 |
| 8.10 Coding of Speech and Audio Signals | 612 |
| 8.10.1 A- and μ -Law Coding | 612 |
| 8.10.2 Linear and Adaptive PCM Coding | 617 |
| 8.10.3 Coding by Modeling: The LPC-10e Method | 623 |
| 8.10.4 MPEG Audio Coding Methods | 624 |
| Exercises | 626 |

| | |
|---|-----|
| 9. Microprocessor Design | 631 |
| 9.1 History of Microprocessors | 631 |
| 9.1.1 Brief History of General-Purpose Microprocessors | 632 |
| 9.1.2 Brief History of RISC Microprocessors | 634 |
| 9.1.3 Brief History of PDSPs | 635 |
| 9.2 Instruction Set Design | 638 |
| 9.2.1 Addressing Modes | 638 |
| 9.2.2 Data Flow: Zero-, One-, Two- or Three-Address Design | 646 |
| 9.2.3 Register File and Memory Architecture | 652 |
| 9.2.4 Operation Support | 656 |
| 9.2.5 Next Operation Location | 659 |
| 9.3 Software Tools | 660 |
| 9.3.1 Lexical Analysis | 661 |
| 9.3.2 Parser Development | 672 |
| 9.4 FPGA Microprocessor Cores | 682 |
| 9.4.1 Hardcore Microprocessors | 683 |
| 9.4.2 Softcore Microprocessors | 689 |
| 9.5 Case Studies | 700 |
| 9.5.1 T-RISC Stack Microprocessors | 700 |
| 9.5.2 LISA Wavelet Processor Design | 706 |
| 9.5.3 Nios Custom Instruction Design | 721 |
| Exercises | 728 |
| 10. Image and Video Processing | 739 |
| 10.1 Overview on Image and Video Processing | 740 |
| 10.1.1 Image Format | 741 |
| 10.1.2 Basic Image Processing Operation | 746 |
| 10.2 Case Study 1: Edge Detection in HDL | 748 |
| 10.2.1 2D HDL Filter Design | 751 |
| 10.2.2 Imaging System Design | 753 |
| 10.2.3 Putting the VGA Edge Detection System Together | 757 |
| 10.3 Case Study 2: Median Filter Using an Image Processing Li- | |
| brary | 769 |
| 10.3.1 The Median Filter | 770 |
| 10.3.2 Median Filter in HDL | 772 |
| 10.3.3 Nios Median Filtering Image Processing System | 775 |
| 10.3.4 Median Filter in SW | 777 |
| 10.4 Motion Detection | 782 |
| 10.4.1 Motion Detection | 782 |
| 10.4.2 ME Co-processor Design | 785 |
| 10.4.3 Video Compression Standards | 788 |
| Exercises | 791 |
| Correction to: Digital Signal Processing with Field Programmable | |
| Gate Arrays | C1 |

| | |
|--|-----|
| Appendix A. Verilog Code of Design Examples | 795 |
| Appendix B. Design Examples Synthesis Results | 879 |
| Appendix C. VHDL and Verilog Coding Keywords | 883 |
| Appendix D. CD-ROM Content | 885 |
| Appendix E. Glossary | 895 |
| References | 903 |
| Index | 923 |