

Robustness against Power is PSpace-complete

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Abstract. Power is a RISC architecture developed by IBM, Freescale, and several other companies and implemented in a series of POWER processors. The architecture features a relaxed memory model providing very weak guarantees with respect to the ordering and atomicity of memory accesses.

Due to these weaknesses, some programs that are correct under sequential consistency (SC) show undesirable effects when run under Power. We call these programs not robust against the Power memory model. Formally, a program is robust if every computation under Power has the same data and control dependencies as some SC computation.

Our contribution is a decision procedure for robustness of concurrent programs against the Power memory model. It is based on three ideas. First, we reformulate robustness in terms of the acyclicity of a happens-before relation. Second, we prove that among the computations with cyclic happens-before relation there is one in a certain normal form. Finally, we reduce the existence of such a normal-form computation to a language emptiness problem. Altogether, this yields a PSPACE algorithm for checking robustness against Power. We complement it by a matching lower bound to show PSPACE-completeness.

1 Introduction

To execute code as fast as possible, modern processors reorder operations. For example, Intel x86/x86-64 and SPARC processors implement the Total Store Ordering (TSO) memory model [13] which allows write buffering: store operations in each thread can be queued and get executed on memory later. Processors can also execute independent instructions out of program order as soon as the input data and computational units are available for them. This is an inherent feature of the POWER and ARM microprocessors [12]. Moreover, Power and ARM memory models, unlike TSO, do not guarantee store atomicity: one write can become visible to different threads at different times. They only ensure that all threads see stores to the same memory location in the same order; stores to different memory locations can be seen in different order by different threads.

All these optimizations are usually designed so that a single-threaded program has the illusion that its instructions are executed in program order. The picture changes in the presence of concurrency. Concurrent programs are often assumed to have sequentially consistent (SC) semantics [10]: each thread executes its operations in program order, stores become visible immediately to all threads. Concurrent programs may observe a difference from SC when run on

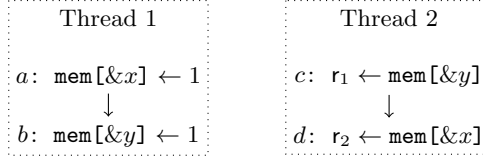


Fig. 1. Message Passing (MP) program [14]. By $\&x$ and $\&y$ we denote the addresses of the variables x and y . Initially, $x = y = 0$. The first thread writes a message into x and sets flag variable y , signifying that the message is written. The second thread reads the flag and, if it is set, expects to see the message written to x by the first thread.

a modern processor with a weak memory model. To see this, consider the MP program in Figure 1. SC and TSO forbid the situation where $r_1 > r_2$ upon termination of both threads. However, this is possible on Power: instruction c can read the value written by b , whereas d reads the initial value.

We call a program *not robust* against Power [15,6,7,2,5,8,4] if it exhibits non-SC behaviors when executed under the Power memory model. More formally, a program is robust if all its Power computations have the same data and control dependencies as the computations under SC. That is, for every Power computation there is a sequentially consistent computation which executes the same instructions, all loads read from the same stores in both computations, and stores to the same address happen in the same order. Robust programs produce the same results on Power and SC architectures, which means verification results for SC remain valid for the weak memory model.

We present an algorithm for deciding robustness against Power. This is the first decidability result for this architecture and, more generally, the first decidability result for a non-store atomic memory model. We obtain the algorithm in the following steps. First, we reformulate robustness in terms of acyclicity of a happens-before relation, using the result by Shasha and Snir [15]. Second, we show that among the computations with cyclic happens-before there is always one in a certain normal form. Next, we prove that the set of all normal-form computations can be generated by a multiheaded automaton — an automaton model developed recently in the context of robustness [8]. Finally, to check cyclicity of the happens-before relation we intersect this automaton with regular languages. The program is robust iff the intersection is empty. This reduces robustness to language emptiness for multiheaded automata. The algorithm works in space polynomial in the size of the program. We obtain a matching lower bound by a reduction of SC-reachability to robustness, similar to [5].

Related work The happens-before relation was formulated by Lamport [9]. Shasha and Snir [15] have shown that a computation violates sequential consistency iff it has a cyclic happens-before relation. Burckhardt and Musuvathi [6] proposed the first algorithm for detecting non-robustness against TSO based on monitoring SC computations. Burnim et al. [7] pointed out a mistake in the definition of TSO used in [6] and described monitoring algorithms for the TSO

and PSO memory models. Alglave and Maranget [2] presented a tool to statically over-approximate happens-before cycles in programs written in x86 and Power assembly, and to insert synchronization primitives (memory fences and syncs) as required for robustness (called stability in their work). Bouajjani et al. [5] obtained the first decidability result for robustness: robustness against TSO is PSPACE-complete for finite-state programs. In [4] they presented a reduction of robustness against TSO to SC reachability for general programs and an algorithm for optimal fence insertion.

The Power architecture has attracted considerable recent attention. Alglave et al. [3] give an overview of the numerous publications devoted to defining its semantics. We highlight two Power models: the operational model by Sarkar et al. [14] and the axiomatic one by Mador-Haim et al. [11]. These models were extensively tested against the architecture and were proven to be equivalent [11]. Nevertheless, the operational model is known to forbid certain behaviors that are possible on real hardware¹ and in the axiomatic model² [3]. Fortunately, there is a suggested fix: in Section 4.5 of [14] one should read *from a coherence-order-earlier write* instead of *from a different write* (two occurrences). Then, the operational model is believed to strictly and tightly over-approximate Power [1]. In the present paper we stick to the corrected operational model from [14].

Finally, we would like to note that ARM has a memory model very similar to that of Power. The differences and similarities are highlighted by Maranget et al. in [12,3]. This fact promises a relatively easy transfer of the proof techniques used in the present paper to the ARM memory model.

2 Programming Model

We define programs and their semantics in terms of automata. An *automaton* is a tuple $A = (S, \Sigma, \Delta, s_0, F)$, where S is a set of states, Σ is an alphabet, $\Delta \subseteq S \times (\Sigma \cup \{\varepsilon\}) \times S$ is a set of transitions, $s_0 \in S$ is an initial state, and $F \subseteq S$ is a set of final states. We call the automaton *finite* if S and Σ are finite. We write $s_1 \xrightarrow{a} s_2$ if $t = (s_1, a, s_2) \in \Delta$ and denote $\text{src}(t) := s_1$, $\text{dst}(t) := s_2$, $\text{lab}(t) = a$. The *language* of the automaton is $\mathcal{L}(A) := \{\sigma \in \Sigma^* \mid s_0 \xrightarrow{\sigma} s \text{ for some } s \in F\}$. For a sequence $\sigma = a_1 \dots a_n \in \Sigma^*$ we define $|\sigma| := n$, $\sigma[i] := a_i$, $\text{first}(\sigma) := a_1$, and $\text{last}(\sigma) := a_n$. We use \cdot for concatenation, \downarrow for projection, and ε for the empty sequence. Given $\alpha \in \Sigma^*$ and $a, b \in \alpha$, we write $a <_\alpha b$ if $\alpha = \alpha_1 \cdot a \cdot \alpha_2 \cdot b \cdot \alpha_3$. Given a function $f: X \rightarrow Y$, $x' \in X$, and $y' \in Y$, we define $f' = f[x' \leftarrow y']$ by $f'(x) := f(x)$ for $x \in X \setminus \{x'\}$ and $f'(x') := y'$.

A program is a finite sequence of threads: $\mathcal{P} = \mathcal{T}_1 \dots \mathcal{T}_n$. A *thread* is an automaton $\mathcal{T}_{\text{tid}} = (Q_{\text{tid}}, \text{CMD}, \mathcal{I}_{\text{tid}}, q_{0_{\text{tid}}}, Q_{\text{tid}})$ with a finite set of control states Q_{tid} , all of them being final, initial state $q_{0_{\text{tid}}}$, and a set of transitions \mathcal{I}_{tid} called *instructions* and labeled with *commands* CMD defined below. Each thread has an id from $\text{TID} := [1..|\mathcal{P}|]$.

¹ <http://diy.inria.fr/cats/pldi-power/#lessvs>

² <http://diy.inria.fr/cats/cav-power/>

Let $\text{DOM} = \text{ADDR}$ be a finite domain of values and addresses containing the value 0. Let REG be a finite set of registers that take values from DOM . The set of commands CMD includes loads, stores, local assignments, and conditionals (**assume**):

$$\begin{aligned} \langle \text{cmd} \rangle ::= & \langle \text{reg} \rangle \leftarrow \text{mem}[\langle \text{expr} \rangle] \mid \text{mem}[\langle \text{expr} \rangle] \leftarrow \langle \text{expr} \rangle \\ & \mid \langle \text{reg} \rangle \leftarrow \langle \text{expr} \rangle \mid \text{assume}(\langle \text{expr} \rangle) \end{aligned}$$

The set of expressions EXPR is defined over constants from DOM , registers from REG , and (unspecified) functions FUN over $\text{DOM} \cup \{\perp\}$. We assume that these functions return \perp iff any of the arguments is \perp .

2.1 Power Semantics

We briefly recall the corrected model from [14]. The state of a running program consists of the runtime states of threads and the state of a storage subsystem.

The runtime state of a thread includes information about the instructions being executed by the thread. In order to start executing an instruction, the thread must *fetch* it. The thread can fetch any instruction whose source control state is equal to the destination state of the last fetched instruction. Then, the thread must perform any computation required by the semantics of this instruction. For example, for a load the thread must compute the address being accessed, then read the value at this address, and place it into the target register. The last step of executing an instruction is *committing* it. Committing an instruction requires committing all its *dependencies*. For example, before committing a load the thread must commit all its *address dependencies* — the instructions which define the values of registers used in the address expression — and *control dependencies* — the program-order-earlier (fetched earlier than the load) conditional instructions. Moreover, all loads and stores accessing the same address must be committed in the order in which they were fetched.

The storage subsystem keeps track, for each address, of the global ordering of stores to this address — the *coherence order* — and the last store to this address *propagated* to each thread. When a thread commits a store, this store is assigned a position in the coherence order which we identify by a rational number — the *coherence key*. We choose rational numbers (rather than naturals) to be able to insert a store between any two stores in the coherence order. The key must be greater than the coherence key of the last store to the same address propagated to this thread. The committed store is immediately propagated to its own thread. At some point later this store can be propagated to any other thread, as long as it is coherence-order-later (has a greater coherence key) than the last store to the same address propagated to that thread. When a thread loads a value from a certain address, it gets the value written by the last store to this address propagated to this thread. A thread can also forward the value being written by a not yet committed store to a later load reading the same address. This situation is called an *early read*.

An important property of Power is that it maintains the illusion of sequential consistency for single-threaded programs. This means that reorderings on

the thread level must not lead to situations when, e.g., a program-order-later load reads a coherence-order-earlier store than the one read by a program-order-earlier load from the same address. In [14] these restrictions are enforced by the mechanism of restarting operations. We put these conditions into the requirements on final states of the running program instead.

To keep the paper readable, we omit the descriptions of Power synchronization instructions: `sync`, `lwsync`, `isync`. All constructions in the paper can be consistently extended to support them with the final result continuing to hold.

Formally, we define the semantics of program \mathcal{P} on Power by a *Power automaton* $Z(\mathcal{P}) := (S_Z, E, \Delta_Z, s_{0Z}, F_Z)$. Here, E is a set of labels called *events* that we define together with the transitions.

State space A state of the Power automaton is a pair $s_Z = (\text{ts}, s_Y) \in S_Z$ with runtime thread states $\text{ts}: \text{TID} \rightarrow S_X$ and storage subsystem state $s_Y \in S_Y$.

A runtime thread state $s_X = (\text{fetched}, \text{committed}, \text{loaded}) \in S_X$ includes a finite sequence of fetched instructions $\text{fetched} \in \mathcal{I}^*$, a set of indices of committed instructions $\text{committed} \subseteq [1..|\text{fetched}|]$, and a function giving the store read by a load $\text{loaded}: [1..|\text{fetched}|] \rightarrow \{\perp\} \cup \{\text{init}_a \mid a \in \text{ADDR}\} \cup \text{TID} \times \mathbb{N}$. We use init_a to denote the initial store of value 0 to address a . The initial state of a running thread is $s_{0X} := (\varepsilon, \emptyset, \lambda i. \perp)$.

A state of the storage subsystem $s_Y = (\text{co}, \text{prop}) \in S_Y$ includes a mapping from a store instruction (its thread id and index in the list of fetched instructions) to its position in the coherence order $\text{co}: (\text{TID} \times \mathbb{N} \cup \{\text{init}_a \mid a \in \text{ADDR}\}) \rightarrow \mathbb{Q}$, and a mapping from a thread id and an address to the last store to this address propagated to this thread $\text{prop}: \text{TID} \times \text{ADDR} \rightarrow \{\text{init}_a \mid a \in \text{ADDR}\} \cup \text{TID} \times \mathbb{N}$. The initial state of the storage subsystem is $s_{0Y} := (\lambda \text{tid}. \lambda i. 0, \lambda \text{tid}. \lambda a. \text{init}_a)$.

The initial state of automaton $Z(\mathcal{P})$ is $s_{0Z} := (\lambda \text{tid}. s_{0X}, s_{0Y})$.

Transition relation Fix a state $s_Z = (\text{ts}, s_Y)$ with $s_Y = (\text{co}, \text{prop})$ and a thread id $\text{tid} \in \text{TID}$ with runtime state $\text{ts}(\text{tid}) = (\text{fetched}, \text{committed}, \text{loaded})$.

Let $\text{eval}(\text{tid}, i, e)$ return the value in DOM of expression e in the i 'th fetched instruction of thread tid , or \perp when the value is undefined. Formally $\text{eval}(\text{tid}, i, e) := v$, where v is computed as follows. If $e \in \text{DOM}$, then $v := e$. If $e = f(e_1 \dots e_n)$, then $v := f(\text{eval}(\text{tid}, i, e_1) \dots \text{eval}(\text{tid}, i, e_n))$. Otherwise, $e = r \in \text{REG}$. Let $i' \in [1..i-1]$ be the greatest index, such that $\text{fetched}[i']$ is a local assignment or a load to r . If there is no such index, we define $v := 0$. If $\text{lab}(\text{fetched}[i']) = r \leftarrow e_v$, then $v := \text{eval}(\text{tid}, i', e_v)$. If $\text{lab}(\text{fetched}[i']) = r \leftarrow \text{mem}[e_a]$, then $v := \perp$ if $\text{loaded}[i'] = \perp$, $v := 0$ if $\text{loaded}[i'] = \text{init}_*$, and $v := \text{val}(\text{loaded}[i'])$ otherwise (see the definition of val below).

The expression $\text{addr}(\text{tid}, i)$ returns the value of the address argument of the i 'th fetched instruction of thread tid and is defined as follows. We use the special value \top if the instruction has no such argument. If $\text{lab}(\text{fetched}[i]) = r \leftarrow \text{mem}[e_a]$ or $\text{lab}(\text{fetched}[i]) = e_a \leftarrow \text{mem}[e_v]$, then $\text{addr}(\text{tid}, i) := \text{eval}(\text{tid}, i, e_a)$. Otherwise, $\text{addr}(\text{tid}, i) := \top$.

Similarly, the expression $\text{val}(\text{tid}, i)$ returns the value of the value argument of the i 'th fetched instruction of thread tid and is defined as follows. If $\text{lab}(\text{fetched}[i]) = \text{mem}[e_a] \leftarrow e_v$, $\text{lab}(\text{fetched}[i]) = r \leftarrow e_v$, or $\text{lab}(\text{fetched}[i]) = \text{assume}(e_v)$, then $\text{val}(\text{tid}, i) = \text{eval}(\text{tid}, i, e_v)$. Otherwise, $\text{val}(\text{tid}, i) := \top$.

The expressions $\text{addrdep}(\text{tid}, i)$, $\text{datadep}(\text{tid}, i)$, $\text{ctrldep}(\text{tid}, i)$ denote the sets of indices of instructions in thread tid being respectively address, data, and control dependencies of the i 'th instruction. The first two can be formally defined in a recursive manner, similar to eval . Also, $\text{ctrldep}(\text{tid}, i) := \{i' \in [1..i-1] \mid \text{lab}(\text{fetched}[i']) = \text{assume}(e_v)\}$.

Let $\mathcal{T}_{\text{tid}} = (Q_{\text{tid}}, \text{CMD}, \mathcal{I}_{\text{tid}}, q_{0\text{tid}}, Q_{\text{tid}}) \in \mathcal{P}$. The transition relation Δ_Z is the smallest relation defined by the rules below:

POW-FETCH Consider $\text{instr} \in \mathcal{I}_{\text{tid}}$ with $\text{src}(\text{instr}) = \text{dst}(\text{last}(\text{fetched}))$ or $\text{src}(\text{instr}) = q_{0\text{tid}}$ if $\text{fetched} = \varepsilon$, then:

$$(\text{ts}, s_Y) \xrightarrow{(\text{fetch}, \text{tid}, \text{instr})} (\text{ts}[\text{tid} \leftarrow (\text{fetched} \cdot \text{instr}, \text{committed}, \text{loaded})], s_Y).$$

POW-LOAD If $\text{fetched}[i]$ is a load, $\text{loaded}[i] = \perp$, $a = \text{addr}(\text{tid}, i) \neq \perp$, then:

$$(\text{ts}, s_Y) \xrightarrow{(\text{load}, \text{tid}, i, a)} (\text{ts}[\text{tid} \leftarrow (\text{fetched}, \text{committed}, \text{loaded}[i \leftarrow \text{prop}(\text{tid}, a)])], s_Y).$$

POW-EARLY Let $\text{fetched}[i]$ be a load, $\text{loaded}[i] = \perp$, and $a = \text{addr}(\text{tid}, i) \neq \perp$.

Let $i' \in [1..i-1]$ be the greatest index such that $\text{fetched}[i']$ is a store with $a' = \text{addr}(\text{tid}, i') \in \{a, \perp\}$. If $a' \neq \perp$, $\text{val}(\text{tid}, i') \neq \perp$, $i' \notin \text{committed}$, then:

$$(\text{ts}, s_Y) \xrightarrow{(\text{load}, \text{tid}, i, a)} (\text{ts}[\text{tid} \leftarrow (\text{fetched}, \text{committed}, \text{loaded}[i \leftarrow (\text{tid}, i')])], s_Y).$$

POW-COMMIT Consider $i \in [1..|\text{fetched}|] \setminus \text{committed}$ where $\text{fetched}[i]$ is not a store. Assume $\text{addrdep}(\text{tid}, i) \cup \text{datadep}(\text{tid}, i) \cup \text{ctrldep}(\text{tid}, i) \subseteq \text{committed}$. Assume $a = \text{addr}(\text{tid}, i) \neq \perp$ and $v = \text{val}(\text{tid}, i) \neq \perp$. If $a \neq \top$, assume $\{i' \in [1..i-1] \mid \text{addr}(\text{tid}, i') \in \{a, \perp\}\} \subseteq \text{committed}$. In case $\text{fetched}[i]$ is a load, assume $\text{loaded}[i] \neq \perp$. In case $\text{fetched}[i]$ is an $\text{assume}()$, assume $v \neq 0$. Then:

$$(\text{ts}, s_Y) \xrightarrow{(\text{commit}, \text{tid}, i)} (\text{ts}[\text{tid} \leftarrow (\text{fetched}, \text{committed} \cup \{i\}, \text{loaded})], s_Y).$$

POW-STORE Assume all the preconditions from the previous rule hold, but $\text{fetched}[i]$ is a store. Choose a coherence key $k \in \mathbb{Q}$ such that there is no $\text{tid}' \in \text{TID}$, $i' \in \mathbb{N}$ for which $\text{co}(\text{tid}', i') = k$. Then:

$$(\text{ts}, s_Y) \xrightarrow{(\text{commit}, \text{tid}, i, k, a)} (\text{ts}[\text{tid} \leftarrow (\text{fetched}, \text{committed} \cup \{i\}, \text{loaded})], s'_Y),$$

where $s'_Y := (\text{co}[(\text{tid}, i) \leftarrow k], \text{prop})$.

Additionally, this transition is immediately followed by a POW-PROP transition propagating the store to the thread where it was committed.

POW-PROP Consider $\text{tid}' \in \text{TID}$, $i' \in \mathbb{N}$ with $\text{co}(\text{tid}', i') \neq \perp$. Let $a = \text{addr}(\text{tid}', i')$. Assume $\text{co}(\text{prop}(\text{tid}, a)) < \text{co}(\text{tid}', i')$. Then:

$$(\text{ts}, s_Y) \xrightarrow{(\text{prop}, \text{tid}, \text{tid}', i', a)} (\text{ts}, (\text{co}, \text{prop}[(\text{tid}, a) \leftarrow (\text{tid}', i')])).$$

Final states The set of final states $F_Z \subseteq S_Z$ consists of all states $s_Z = (\text{ts}, (\text{co}, \text{prop})) \in S_Z$, such that for each $\text{tid} \in \text{TID}$, $\text{ts}[\text{tid}] = (\text{fetched}, \text{committed}, \text{loaded})$ the following holds:

FIN-COMM All instructions are committed: $\text{committed} = [1..|\text{fetched}|]$.

FIN-LD Loads agree with the coherence order. Let $\text{fetched}[i]$ be a load, and $\text{fetched}[i']$ be an earlier load to the same address: $i' < i$, $\text{addr}(\text{tid}, i) = \text{addr}(\text{tid}, i')$. Then $\text{co}(\text{loaded}[i']) \leq \text{co}(\text{loaded}[i])$.

FIN-LD-ST Loads and stores in the same thread agree with the coherence order. Let $\text{fetched}[i]$ be a load, let $\text{fetched}[i']$ be an earlier store to the same address: $i' < i$, $\text{addr}(\text{tid}, i) = \text{addr}(\text{tid}, i')$. Then $\text{co}(\text{tid}, i') \leq \text{co}(\text{loaded}[i])$.

The set of all *Power computations of program \mathcal{P}* is $\mathbf{C}_{\text{power}}(\mathcal{P}) := \mathcal{L}(Z(\mathcal{P}))$. The set of all *SC computations of the program* $\mathbf{C}_{\text{sc}}(\mathcal{P}) \subseteq \mathbf{C}_{\text{power}}(\mathcal{P})$ includes only those computations where each instruction is executed atomically, and stores are immediately propagated to all threads.

Example 1. $\sigma_{\text{MP}} = \text{fetch}(a) \cdot \text{commit}(a) \cdot \text{prop}(a, 1) \cdot \text{fetch}(b) \cdot \text{commit}(b) \cdot \text{prop}(b, 1) \cdot \text{prop}(b, 2) \cdot \text{fetch}(c) \cdot \text{fetch}(d) \cdot \text{load}(c) \cdot \text{load}(d) \cdot \text{commit}(d) \cdot \text{commit}(c)$ is a feasible Power computation of the program MP (Figure 1):

- $\text{fetch}(a) := (\text{fetch}, 1, a)$ — thread 1 fetches store instruction a .
- $\text{commit}(a) := (\text{commit}, 1, 1, 1, \&x)$ — thread 1 commits a with $k = 1$.
- $\text{prop}(a, 1) := (\text{prop}, 1, 1, 1, \&x)$ — a is propagated to its own thread.
- $\text{fetch}(b) := (\text{fetch}, 1, b)$ — thread 1 fetches store instruction b .
- $\text{commit}(b) := (\text{commit}, 1, 2, 2, \&y)$ — thread 1 commits b with $k = 2$.
- $\text{prop}(b, 1) := (\text{prop}, 1, 1, 2, \&x)$ — the store is propagated to its thread.
- $\text{prop}(b, 2) := (\text{prop}, 2, 1, 2, \&x)$ — the store is propagated to thread 2.
- $\text{fetch}(c) := (\text{fetch}, 2, c)$ — thread 2 fetches load c .
- $\text{fetch}(d) := (\text{fetch}, 2, c)$ — thread 2 fetches load d .
- $\text{load}(c) := (\text{load}, 2, 1, \&y)$ — thread 2 reads value 1 written by b to y , because b was propagated to thread 2.
- $\text{load}(d) := (\text{load}, 2, 2, \&x)$ — thread 2 reads the initial value 0 of x , because a was not propagated to thread 2.
- $\text{commit}(d) := (\text{commit}, 2, 2)$ — thread 2 commits load d .
- $\text{commit}(c) := (\text{commit}, 2, 1)$ — thread 2 commits load c .

In the end, FIN-COMM holds as all fetched instructions are indeed committed, and FIN-LD and FIN-LD-ST trivially hold, as none of the threads has two instructions accessing the same address.

Lemma 1. Assume $s_{0Z} \xrightarrow{\sigma} s_Z \in F_Z$. Then s_Z is uniquely determined.

Proof. Given a state and an event e , there is at most one transition from this state labeled by e . This is clear for non-load events. For load events, this follows from Lemma 4 and Lemma 5: if a load event was produced by a load from memory transition, then condition (3) from Lemma 5 holds, then condition (1) from Lemma 4 cannot hold for any store, therefore, the load event cannot be produced by an early read transition. \square

Lemma 2. Let $s_{0Z} \xrightarrow{\sigma} (ts, s_Y) \xrightarrow{e} (ts', s'_Y)$. Let $(\text{fetched}, \text{committed}, \text{loaded}) = ts(\text{tid})$, $(\text{fetched}', \text{committed}', \text{loaded}') = ts'(\text{tid})$ for some $\text{tid} \in TID$. If $\text{loaded}[i] \neq \perp$, then $\text{loaded}'[i] = \text{loaded}[i]$.

Proof. Follows from the $\text{loaded}[i] = \perp$ requirement in POW-LOAD and POW-EARLY transitions. \square

Lemma 3. Let $s_{0Z} \xrightarrow{\sigma} s_Z \xrightarrow{e} s_{Z'}$. Assume $\text{eval}(\text{tid}, i, e) = v \neq \perp$ in s_Z . Then $\text{eval}(\text{tid}, i, e) = v$ in $s_{Z'}$.

Proof. By definition of eval , Lemma 2, and the fact that functions in FUN are deterministic. \square

Lemma 4. Consider a computation $\sigma \in C_{\text{power}}(\mathcal{P})$. Then a load (tid, i) reads a value from a store (tid, i') via an early read (POW-EARLY) transition iff (1) $\sigma = \sigma_1 \cdot (\text{load}, \text{tid}, i, a) \cdot \sigma_2 \cdot (\text{commit}, \text{tid}, i', *, a) \cdot \sigma_3$, $i' \in [1..i-1]$ and (2) σ_3 does not contain events matching $(\text{commit}, \text{tid}, [i' + 1..i-1], *, a)$.

Proof. From left to right. Assume the load (tid, i) reads the store (tid, i') via an early read transition. Then (tid, i) must be the latest store to the same address in thread tid and must not be committed before load (i.e. committed after it), therefore (1) holds. If (2) does not hold, then (tid, i') is not the latest store to address a in thread tid before the load event, since stores to the same address are committed in the order of fetching. Contradiction.

From right to left. Let $s_{0Z} \xrightarrow{\sigma_1} s_Z = (ts, s_Y)$. Consider $ts(\text{tid}) = (\text{fetched}, \text{committed}, \text{loaded})$. Let $i'' < i$ be the greatest index, such that $\text{fetched}[i'']$ is a store, $\text{addr}(i'') \in \{a, \perp\}$.

Assume $i' < i''$. If $\text{addr}(i'') = a$, we get a contradiction to (2), since stores to the same address are committed in the order of fetching. If $\text{addr}(i'') = \perp$, then an early read is not possible in state s_Z , and the load reads from the latest propagated store (POW-LOAD), which is coherence-order-before the store (tid, i') , which is program-order-before (tid, i) . This situation is forbidden by FIN-LD-ST.

By Lemma 3, $\text{addr}(\text{tid}, i') \in \{a, \perp\}$, therefore, $i'' = i'$. Assume $\text{addr}(\text{tid}, i') = \perp$ or $\text{val}(\text{tid}, i') = \perp$. Then, again, a load from the latest propagated store takes place, which is impossible (see above). Therefore, $\text{addr}(\text{tid}, i') = a$ and $\text{val}(\text{tid}, i') \neq \perp$.

Obviously, $i' \notin \text{committed}$ holds, as each fetched instruction is committed only once, and (tid, i') is committed after the load takes place, see (1). All in all, all requirements for the early read from (tid, i') are met, therefore, an early read transition from state s_Z is possible. As shown above, a load from memory transition from the same state leads to $\sigma \notin C_{\text{power}}(\mathcal{P})$, therefore, (tid, i) reads from the store (tid, i') via an early read transition. \square

Lemma 5. Consider a computation $\sigma \in C_{\text{power}}(\mathcal{P})$. Then a load (tid, i) reads a value from a store (tid', i') via a load from memory (POW-LOAD) transition iff (1) $\sigma = \sigma_1 \cdot (\text{prop}, \text{tid}, \text{tid}', i', a) \cdot \sigma_2 \cdot (\text{load}, \text{tid}, i, a) \cdot \sigma_3$, (2) σ_2 does not contain events matching $(\text{prop}, \text{tid}, *, *, a)$, and (3) σ_3 does not contains events matching $(\text{commit}, \text{tid}, [1..i-1], *, a)$.

Proof. From left to right. Assume the load (tid, i) reads the store (tid', i') via a load from memory transition. Then, the load has read from the latest store to address \mathbf{a} propagated to thread tid , i.e., (1) and (2) hold. Assume (3) does not hold — σ_3 contains a commit $(\text{commit}, \text{tid}, i'', *, \mathbf{a})$ and $i'' < i$. Then, (tid, i) reads from the store (tid', i') , which is coherence-order-before the store (tid, i'') , which is program-order-before (tid, i) . This situation is forbidden by FIN-LD-ST.

From right to left. By (1), (3), and Lemma 4, the load event was not generated by an early read transition. Therefore, the event was generated by a load from memory transition, and the load has taken the value from the latest propagated store to address \mathbf{a} , which is, by (1) and (2), (tid', i') . \square

3 Robustness

Intuitively, a *trace* $T(\sigma)$ abstracts a program computation σ to the dataflow and control-flow relations between instructions. Formally, the trace of σ is a directed graph $T(\sigma) := (V, \rightarrow_{po}, \rightarrow_{co}, \rightarrow_{src}, \rightarrow_{cf})$ with nodes V and four kinds of arcs. The nodes are instructions together with their thread identifiers and serial numbers (in order to distinguish instructions executed in different threads and the same instruction executed multiple times in the same thread): $V \subseteq (\{\text{init}_a \mid a \in \text{ADDR}\} \cup \bigcup_{\text{tid} \in \text{TID}} \{\text{tid}\}) \times \mathbb{N} \times \mathcal{I}_{\text{tid}}$. The *program order* \rightarrow_{po} is the order in which instructions were fetched in each thread. The *coherence order* \rightarrow_{co} gives the global ordering of writes to each address. The *source order* \rightarrow_{src} shows the store from which a load took its value. The *conflict order* \rightarrow_{cf} shows, for a load, the stores to the same address following the store the load took its value from. We define the *happens-before* relation as $\rightarrow_{hb} := \rightarrow_{po} \cup \rightarrow_{co} \cup \rightarrow_{src} \cup \rightarrow_{cf}$.

Formally, consider a computation $\sigma \in \mathcal{C}_{\text{power}}(\mathcal{P})$. Let $s_{0Z} \xrightarrow{\sigma} s_Z$ with $s_Z = (\text{ts}, (\text{co}, \text{prop}))$. By Lemma 1, s_Z is uniquely determined. The trace $T(\sigma) := (V, \rightarrow_{po}, \rightarrow_{co}, \rightarrow_{src}, \rightarrow_{cf})$ is defined as follows. Assuming $\text{tid} \in \text{TID}$, $\text{ts}(\text{tid}) = (\text{fetched}, \text{committed}, \text{loaded})$, $i \in [1..|\text{fetched}|]$, and similarly for tid' , we have:

$$\begin{aligned}
V &:= \{(\text{tid}, i, \text{fetched}[i]) \mid \text{tid} \in \text{TID}, i \in \mathbb{N}\}, \\
\rightarrow_{po} &:= \{((\text{tid}, i, \text{fetched}[i]), (\text{tid}, i+1, \text{fetched}[i+1])) \mid \\
&\quad i \in [1..|\text{fetched}| - 1]\}, \\
\rightarrow_{co} &:= \{((\text{tid}, i, \text{fetched}[i]), (\text{tid}', i', \text{fetched}[i'])) \mid \\
&\quad \text{addr}(\text{tid}, i) = \text{addr}(\text{tid}', i') \text{ and } \text{co}(\text{tid}, i) < \text{co}(\text{tid}', i')\} \cup \\
&\quad \{(\text{init}_a, (\text{tid}', i', \text{fetched}[i'])) \mid a = \text{addr}(\text{tid}', i')\}, \\
\rightarrow_{src} &:= \{((\text{tid}, i, \text{fetched}[i]), (\text{tid}', i', \text{fetched}'[i'])) \mid \\
&\quad (\text{tid}, i) = \text{loaded}'[i']\} \cup \\
&\quad \{(\text{init}_a, (\text{tid}', i', \text{fetched}'[i'])) \mid \text{init}_a = \text{loaded}'(i')\}, \\
\rightarrow_{cf} &:= \{(a, b) \mid \exists c: c \rightarrow_{src} a \text{ and } c \rightarrow_{co} b\}.
\end{aligned}$$

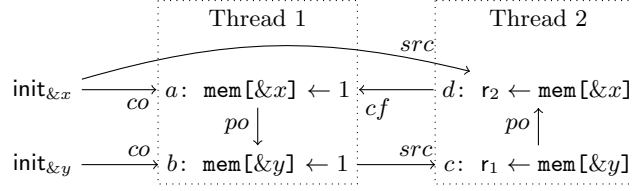


Fig. 2. Trace of computation σ_{MP} from Example 1.

We will also need address \rightarrow_{addr} and data \rightarrow_{data} dependence relations (defined as expected based on `addrdep` and `datadep`).

$$\begin{aligned} \rightarrow_{addr} &:= \{((tid, i, \text{fetched}[i]), (tid, i', \text{fetched}'[i])) \mid i \in \text{addrdep}(tid, i')\}, \\ \rightarrow_{data} &:= \{((tid, i, \text{fetched}[i]), (tid, i', \text{fetched}'[i])) \mid i \in \text{datadep}(tid, i')\}. \end{aligned}$$

Since \rightarrow_{po} includes all the information from the `fetched` component of a thread state, \rightarrow_{addr} and \rightarrow_{data} can be reconstructed from \rightarrow_{po} by inspecting the instructions labeling a node. They are therefore not included in the trace explicitly.

The *robustness problem* is, given a program \mathcal{P} , to check whether the set of all traces under Power is a subset of all traces under SC: $T_{\text{power}}(\mathcal{P}) \subseteq T_{\text{sc}}(\mathcal{P})$, where $T_{\text{mm}}(\mathcal{P}) := \{T(\sigma) \mid \sigma \in C_{\text{mm}}(\mathcal{P})\}$ for $\text{mm} \in \{\text{power}, \text{sc}\}$.

Shasha and Snir have shown that a trace belongs to an SC computation iff its happens-before relation is acyclic:

Lemma 6 ([15]). *A program \mathcal{P} is robust against Power iff there is no trace $T \in T_{\text{power}}(\mathcal{P})$ with cyclic \rightarrow_{hb} .*

Example 2. The trace of computation σ_{MP} (Figure 2) has a cyclic happens-before relation. By Lemma 6, this means that the program is not robust. Indeed, in no SC computation load d can read 0 whereas c has read 1.

4 Normal-Form Computations

We say that a computation $\tau \in C_{\text{power}}(\mathcal{P})$ is *in normal form of degree n* if there is a partitioning $\tau = \tau_1 \cdots \tau_n$, such that all `fetch` events are in τ_1 (NF-A) and events related to different instructions occur in different parts of the computation in the same order (NF-B):

NF-A $(\tau_2 \cdots \tau_n) \downarrow \text{fetch} = \varepsilon$.

NF-B Formally, for $j \in \{1, 2\}$ let e_j, e'_j be events related to instruction (tid_j, i_j) .

If $e_1, e_2 \in \tau_s$ and $e'_1, e'_2 \in \tau_{s'}$, then $e_1 <_{\tau_s} e_2$ iff $e'_1 <_{\tau_{s'}} e'_2$.

In the rest of this section we prove the following theorem:

Theorem 1. *A program is robust iff it has no normal-form computations of degree $|\mathcal{P}| + 3$ with cyclic happens-before relation.*

Consider a computation $\sigma \in \mathbf{C}_{\text{mm}}(\mathcal{P})$. By $\sigma \setminus (\text{tid}, i)$ we denote the computation obtained from σ by deleting all events related to the i 'th fetched instruction in thread tid .

Lemma 7. *Consider a non-empty computation $\sigma \in \mathbf{C}_{\text{power}}(\mathcal{P})$. Then there is a (tid_x, i_x) , such that $\sigma' = \sigma \setminus (\text{tid}_x, i_x)$ satisfies $|\sigma'| < |\sigma|$ and $\sigma' \in \mathbf{C}_{\text{power}}(\mathcal{P})$.*

Proof. Consider the last fetched instruction in each thread. If among such instructions there is a non-store instruction, delete it: its result cannot be used by any other instruction. If all these instructions are stores, delete the one, on which (1) no load or store depends via $(\rightarrow_{\text{src}} \cup \rightarrow_{\text{data}})^+ \cdot \rightarrow_{\text{addr}}$, and (2) no condition depends via $(\rightarrow_{\text{src}} \cup \rightarrow_{\text{data}})^+$.

Towards a contradiction, assume there is no such store. Consider a last fetched (store) instruction in a thread $\text{tid}_1: (\text{tid}_1, i_1)$. Case 1: there is a load or a store (tid_2, i'_2) whose address depends on (tid_1, i_1) . Case 2: there is a condition (tid_2, i'_2) whose value depends on (tid_1, i_1) . Consider the last fetched instruction in thread $\text{tid}_2: (\text{tid}_2, i_2)$. It must be a store, and it must have been committed after (tid_1, i_1) : a store can only be committed after all loads and stores fetched before it have their addresses determined (Case 1) and after all preceding conditions are committed (Case 2).

Continuing the reasoning, for any last fetched instruction in a thread (tid_j, i_j) there is a last instruction in a different thread $(\text{tid}_{j+1}, i_{j+1})$ which must have been committed later. Taking into account finiteness of the number of threads, we get a contradiction. \square

Fix a program \mathcal{P} . Consider a shortest Power computation $\alpha \in \mathbf{C}_{\text{power}}(\mathcal{P})$ with cyclic \rightarrow_{hb} . Let (tid_x, i_x) be the instruction determined by Lemma 7. Let $\alpha := \alpha_1 \cdot x_1 \cdot \alpha_2 \cdot x_2 \cdots \alpha_n$, where $\{x_1 \dots x_{n-1}\}$ are the events related to the i_x 'th instruction fetched in thread tid_x . Then $\alpha \setminus (\text{tid}_x, i_x) := \alpha' := \alpha_1 \cdot \alpha_2 \cdots \alpha_n$. Since α' is shorter than α , its \rightarrow_{hb} is acyclic. Therefore, there is a computation $\beta \in \mathbf{C}_{\text{sc}}(\mathcal{P})$ with $T(\beta) = T(\alpha')$.

Computations β and α' consist of the same fetch, load, and commit events: fetch events are determined by \rightarrow_{po} ; address component \mathbf{a} of load and store commit events is determined by $\rightarrow_{\text{addr}}, \rightarrow_{\text{data}}$ (derivable from \rightarrow_{po}), and \rightarrow_{src} ; since \rightarrow_{co} is the same for both computations, we can assume that matching store commit events have the same value of coherence key \mathbf{k} . Notably, β can have more propagate events than α' as Power semantics does not guarantee that all stores are propagated to all threads. Now we reorder events in each part α_j of α in the way they follow in β . This gives a computation $\gamma := \beta \downarrow \alpha_1 \cdot x_1 \cdot \beta \downarrow \alpha_2 \cdot x_2 \cdots \beta \downarrow \alpha_n$. In the rest of the section we show that γ is a valid Power computation of program \mathcal{P} and has the same trace as α .

Lemma 8. *For all $\text{tid} \in \text{TID}$ holds $\alpha \downarrow \text{fetch} \downarrow \text{tid} = \gamma \downarrow \text{fetch} \downarrow \text{tid}$.*

Proof. Since $T(\beta) = T(\alpha')$, by definition of α and properties of projection, for any $\text{tid} \in \text{TID}$ we have

$$\begin{aligned}
\alpha \downarrow \text{fetch} \downarrow \text{tid} &= \alpha_1 \downarrow \text{fetch} \downarrow \text{tid} \cdot x_1 \downarrow \text{fetch} \downarrow \text{tid} \cdots \alpha_n \downarrow \text{fetch} \downarrow \text{tid} \\
&= \cdots (\beta \downarrow \text{fetch} \downarrow \text{tid}) \downarrow (\alpha_i \downarrow \text{fetch} \downarrow \text{tid}) \cdot x_i \downarrow \text{fetch} \downarrow \text{tid} \cdots \\
&= \beta \downarrow \alpha_1 \downarrow \text{fetch} \downarrow \text{tid} \cdot x_1 \downarrow \text{fetch} \downarrow \text{tid} \cdots \beta \downarrow \alpha_n \downarrow \text{fetch} \downarrow \text{tid} \\
&= (\beta \downarrow \alpha_1 \cdot x_1 \cdots \beta \downarrow \alpha_n) \downarrow \text{fetch} \downarrow \text{tid} \\
&= \gamma \downarrow \text{fetch} \downarrow \text{tid}.
\end{aligned}$$

□

Lemma 9. Consider some (tid, i) and (tid', i') . Let $P(\sigma) := \text{true}$ if requirements (1)–(2) from Lemma 4 or (1)–(3) from Lemma 5 hold for σ , and $P(\sigma) := \text{false}$ otherwise. Then, if $P(\alpha)$ then $P(\gamma)$.

Proof. The proof is a case consideration: which of the two cases holds in the definition of P hold for σ , for α , and whether the distinguished load and commit events are located in the same part α_j . We consider two of the cases. The other are similar.

Assume requirements (1)–(2) from Lemma 4 hold for α and requirements (1)–(3) from Lemma 5 holds for sequentially consistent computation β . If load and commit events are in the same part, then $\alpha = \alpha_1 \cdot x_1 \cdots (\alpha'_j \cdot b \cdot \alpha''_j \cdot c \cdot d \cdot \alpha'''_j) \cdot x_j \cdots \alpha_n$, $\beta = \beta_1 \cdots c \cdot d \cdot \beta_2 \cdot b \cdot \beta_3$, where $b = (\text{load}, \text{tid}, i, a)$, $c = (\text{commit}, \text{tid}, i')$, $d = (\text{prop}, \text{tid}, \text{tid}, i', a)$, $i' < i$. Consequently, $\gamma = \beta \downarrow \alpha_1 \cdot x_1 \cdots \beta \downarrow \alpha_j \cdot x_j \cdots \beta \downarrow \alpha_n = \beta \downarrow \alpha_1 \cdot x_1 \cdots (\beta_1 \downarrow \alpha_j \cdot d \cdot \beta_2 \downarrow \alpha_j \cdot b \cdot \beta_3 \downarrow \alpha_j) \cdot x_j \cdots \beta \downarrow \alpha_n$ — looks like a read from memory situation. We check requirements (1)–(3) of Lemma 5 then. First, $\beta_2 \downarrow \alpha_j$ must have no **prop** events to thread tid with the address a — holds as β_2 does not have them. Second, $\beta_3 \downarrow \alpha_j$ must have no commits of earlier writes in thread tid — holds as β_3 does not have them. Third, $\beta \downarrow \alpha_l = (\beta_1 \cdot \beta_2 \cdot \beta_3) \downarrow \alpha_l$, $l \in [i+1..n]$ must have no commit events for stores with indices $[1..i-1]$, the same address and thread id . Consider $\beta_1 \downarrow \alpha_l$ — if it has such an event e , then two stores to the same address, e and c , are committed in different order in α' and β , which is impossible due to $T(\alpha') = T(\beta)$. Consider $\beta_2 \downarrow \alpha_l$ — it does not have such an event, because β_2 does not have **prop** events to address a , therefore, it does not have commits of own stores there too. Consider $\beta_3 \downarrow \alpha_l$ — it does not have such an event, because β_3 does not. Finally, none of x_l events, $l \in [i+1..n-1]$, must be a commit of earlier writes in thread tid — holds, as these events belong to the last fetched instruction of a thread.

Consider the case when load and commit events are in different parts, i.e. $\alpha = \alpha_1 \cdot x_1 \cdots (\alpha'_j \cdot b \cdot \alpha''_j) \cdots (\alpha'_k \cdot c \cdot d \cdot \alpha''_k) \cdots \alpha_n$, $\beta = \beta_1 \cdot c \cdot d \cdot \beta_2 \cdot b \cdot \beta_3$, where b, c, d are defined as before and $i' < i$. Then, $\gamma = \beta \downarrow \alpha_1 \cdot x_1 \cdots \beta \downarrow \alpha_j \cdot x_j \cdots \beta \downarrow \alpha_k \cdots \beta \downarrow \alpha_n = \beta \downarrow \alpha_1 \cdot x_1 \cdots \beta_1 \downarrow \alpha_j \cdot \beta_2 \downarrow \alpha_j \cdot b \cdot \beta_3 \downarrow \alpha_j \cdot x_j \cdots \beta_1 \downarrow \alpha_k \cdot c \cdot d \cdot \beta_2 \downarrow \alpha_k \cdot \beta_3 \downarrow \alpha_k \cdot x_k \cdots \beta \downarrow \alpha_n$ — looks like an early read case. Therefore, one must check that $\beta_2 \downarrow \alpha_k \cdot \beta_3 \downarrow \alpha_k \cdot x_k \cdots \beta \downarrow \alpha_n$ has no **commit** events matching $(\text{commit}, \text{tid}, [i'+1..i-1], *, a)$. Consider $\beta_2 \downarrow \alpha_k$ — does not have such events, because they would be immediately followed by a **prop** event to thread tid and

address \mathbf{a} , which contradicts requirement (2) of Lemma 5. Consider $\beta_3 \downarrow \alpha_k$ — does not have such events, because β_3 does not have them by requirement (3) of Lemma 5. Consider $\beta \downarrow \alpha_l$, $l \in [j+1..n]$ — does not have such events, because α_l do not have them by requirement (2) of Lemma 4. Finally, \mathbf{x}_l , $l \in [j+1..n-1]$ belong to the last fetched instruction of a thread, therefore do not contain the described **commit** events. \square

Lemma 10. $\gamma \in C_{\text{power}}(\mathcal{P})$.

Proof. We proceed by induction. Assume (1) $\gamma = \gamma_1 \cdot \mathbf{e} \cdot \gamma_2$, (2) $s_{0Z} \xrightarrow{\gamma_1} s_Z$, and (3) all loads satisfied in γ_1 have read from the same stores as in α . We show that $s_{0Z} \xrightarrow{\gamma_1 \cdot \mathbf{e}} s_{Z'}$ and all loads satisfied in $\gamma_1 \cdot \mathbf{e}$ have read from the same stores as in α . Let $s_Z = (\mathbf{ts}, s_Y)$ and $\mathbf{ts}(\mathbf{tid}) = (\mathbf{fetched}, \mathbf{committed}, \mathbf{loaded})$. Consider the event \mathbf{e} .

(**fetch**, \mathbf{tid} , i) A transition labeled by \mathbf{e} from state s_Z is feasible due to Lemma 8 and the fact that feasibility of a fetch transition is conditioned solely on the previous **fetch** transition with the same thread id.

(**load**, \mathbf{tid} , i , \mathbf{a}) For the transition to be feasible, $\mathbf{addr}(i) = \mathbf{a}$ must hold. In order to have $\mathbf{addr}(\mathbf{tid}, i) \neq \perp$, all loads in thread \mathbf{tid} , on which $\mathbf{addr}(\mathbf{tid}, i)$ depends, must be satisfied. Note that these loads are the same in α and γ due to Lemma 8. Since $\alpha \in C_{\text{power}}(\mathcal{P})$, these **load** events occurred before \mathbf{e} in α . Let \mathbf{e}' be one of these **load** events. If $\mathbf{e}' \in \alpha_i$ and $\mathbf{e} \in \alpha_j$, $i < j$, or $\mathbf{e}' \in \{\mathbf{x}_i \mid i \in [1..n-1]\}$, or $\mathbf{e} \in \{\mathbf{x}_i \mid i \in [1..n-1]\}$, then \mathbf{e}' and \mathbf{e} are located in γ in the same order. If $\mathbf{e}', \mathbf{e} \in \alpha_i$, then $\mathbf{e}', \mathbf{e} \in \beta$. Since the \rightarrow_{po} components of $T(\alpha)$ and $T(\beta)$ match up to a single deleted arc, \mathbf{e}' and \mathbf{e} are located in β (therefore, in $\beta \downarrow \alpha_i$ and γ) in this order. By inductive assumption (3) and the fact that functions in **FUN** are deterministic, $\mathbf{addr}(\mathbf{tid}, i) = \mathbf{a}$ holds.

Assume the load (\mathbf{tid}, i) has read from a store (\mathbf{tid}', i') in α . Then, by Lemmas 4, 5, 9, either conditions (1)–(3) of Lemma 5 hold, or conditions (1)–(2) of Lemma 4 hold. In the former case, (**prop**, \mathbf{tid} , \mathbf{tid}' , i' , \mathbf{a}) is the last **prop** event to \mathbf{tid} with address \mathbf{a} , therefore, a load from memory transition reading (\mathbf{tid}', i') is feasible from state s_Z . In the latter case, (\mathbf{tid}', i') is the latest non-committed store to address \mathbf{a} , and an early read transition reading (\mathbf{tid}', i') is possible. The proof that $\mathbf{addr}(\mathbf{tid}', i') \neq \perp$ is similar to the proof that $\mathbf{addr}(\mathbf{tid}, i) \neq \perp$.

(**commit**, \mathbf{tid} , i) The proof of $\mathbf{addr}(\mathbf{tid}, i) \neq \perp$ and $\mathbf{val}(\mathbf{tid}, i) \neq \perp$ is similar to the proof of $\mathbf{addr}(\mathbf{tid}, i) \neq \perp$ in the previous case. If $\mathbf{fetched}[i]$ is a load or a store, there must be no preceding loads and stores to unknown addresses, which holds and can be proven in a similar way. If $\mathbf{fetched}[i]$ is a load, requirement $\mathbf{loaded}[i] \neq \perp$ holds for the same reasons. If $\mathbf{fetched}[i]$ is a conditional, requirement $\mathbf{val}(\mathbf{tid}, i) \neq 0$ holds by inductive assumption (3), the fact that functions in **FUN** are deterministic, and the fact that $\alpha \in C_{\text{power}}(\mathcal{P})$.

(**commit**, \mathbf{tid} , i , \mathbf{k} , \mathbf{a}) Value \mathbf{k} is unique, since it was unique in α , and α and γ consist of the same **commit** events. We check $\mathbf{co}(\mathbf{prop}(\mathbf{tid}, \mathbf{a})) < \mathbf{k}$. Assume it does not hold. Then, there is $\mathbf{e}' = (\mathbf{prop}, \mathbf{tid}, \mathbf{tid}', i', \mathbf{a})$, where $\mathbf{co}(\mathbf{tid}', i') > \mathbf{k}$,

and e', e are located in γ in this order. If $e' \in \alpha_i, e \in \alpha_j, i < j$, or $e' \in \{x_i \mid i \in [1..n-1]\}$, or $e \in \{x_i \mid i \in [1..n-1]\}$, these events are located in α in this order, which contradicts $\alpha \in C_{\text{power}}(\mathcal{P})$. If $e', e \in \alpha_i$, these events are located in β in this order, which contradicts $\beta \in C_{\text{power}}(\mathcal{P})$.

This transition is immediately followed by a **prop** transition in γ , since it did so in α and β (unless $e \in \{x_i \mid i \in [1..n-1]\}$, which is a simpler case), and by properties of projection.

(**prop**, **tid**, **tid'**, i', a) The requirement $\text{co}(\text{prop}(\text{tid}, a)) < \text{co}(\text{tid}', i')$ is proven similarly to $\text{co}(\text{prop}(\text{tid}, a)) < k$ in the previous case.

As shown above, $s_{0Z} \xrightarrow{\gamma} s_Z$. What is left to check, is that $s_Z \in F_Z$. The requirement that all fetched instructions are committed trivially holds: β includes the same commit events as α' , therefore, by definition, γ contains the same commit events as α . The other two requirements that loads and stores agree with the coherence order hold due to Lemma 8, the inductive assumption (3), and the fact that α and γ consist of the same commit events (i.e. the coherence keys of matching stores are equal in these computations). \square

Lemma 11. $T(\gamma) = T(\alpha)$

Proof. Equality of \rightarrow_{po} follows from Lemma 8. Equality of source relation follows from Lemmas 4, 5, 9, 10. Store order is determined by **a** and **k** components of store commit events. Since computations α and γ consist of the same commit events, the \rightarrow_{co} relations in the traces of α and γ are the same. \square

Lemma 12. $\gamma \in C_{\text{power}}(\mathcal{P})$ and $T(\gamma) = T(\alpha)$.

Proof. Corollary of Lemmas 10 and 11. \square

Without loss of generality we may assume that all **fetch** events of α are located within $\alpha_1 \cdot x_1$: every thread can always first fetch all instructions and in the rest of the computation only execute them; such a reordering does not change the trace. Also, note that the maximal number of events an instruction can generate is $|\mathcal{P}| + 2$. This bound is achieved by a store that is fetched, committed, and propagated to all threads. Then the following lemma holds:

Lemma 13. *Computation γ is in normal form of degree $|\mathcal{P}| + 3$.*

Proof. By definition of γ and properties of projection. \square

Together with Lemma 6 this proves Theorem 1.

Example 3. Consider $\alpha := \text{fetch}(c) \cdot \text{fetch}(d) \cdot \text{fetch}(a) \cdot \cancel{\text{fetch}(b)} \cdot \text{commit}(a) \cdot \text{prop}(a, 1) \cdot \cancel{\text{commit}(b)} \cdot \cancel{\text{prop}(b, 1)} \cdot \cancel{\text{prop}(b, 2)} \cdot \text{load}(c) \cdot \text{load}(d) \cdot \text{commit}(d) \cdot \text{commit}(c)$, which is essentially σ_{MP} with **fetch** events moved to the front. We cancel the x_i events (crossed out) related to the store instruction b , as b is the last instruction of thread 1 and no address depends on it (we could also cancel the events of d instead). Therefore, $\alpha_1 := \text{fetch}(c) \cdot \text{fetch}(d) \cdot \text{fetch}(a)$, $\alpha_2 := \text{commit}(a) \cdot \text{prop}(a, 1)$, $\alpha_3 := \alpha_4 := \varepsilon$, $\alpha_5 := \text{load}(c) \cdot \text{load}(d) \cdot \text{commit}(d) \cdot \text{commit}(c)$, and $\alpha' :=$

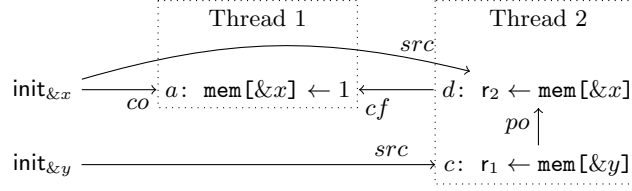


Fig. 3. Trace of the computations α' and β from Example 3.

$\alpha_1 \cdot \alpha_2 \cdot \alpha_3 \cdot \alpha_4 \cdot \alpha_5$. The trace of α' is shown in Figure 3. The SC computation with the same trace is $\beta := \text{fetch}(c) \cdot \text{load}(c) \cdot \text{commit}(c) \cdot \text{fetch}(d) \cdot \text{load}(d) \cdot \text{commit}(d) \cdot \text{fetch}(a) \cdot \text{commit}(a) \cdot \text{prop}(a, 1) \cdot \text{prop}(a, 2)$. The normal-form computation is $\gamma := \beta \downarrow \alpha_1 \cdot x_1 \cdots \beta \downarrow \alpha_5 = (\text{fetch}(c) \cdot \text{fetch}(d) \cdot \text{fetch}(a)) \cdot \text{fetch}(b) \cdot (\text{commit}(a) \cdot \text{prop}(a, 1)) \cdot \text{commit}(b) \cdot \text{prop}(b, 1) \cdot \text{prop}(b, 2) \cdot (\text{load}(c) \cdot \text{commit}(c) \cdot \text{load}(d) \cdot \text{commit}(d))$. It is feasible and has the same trace as α and σ_{MP} (Figure 2).

5 From Normal-Form Computations to Emptiness

We now reduce robustness to language emptiness. First, we define a multiheaded automaton capable of generating all normal-form computations of a program. Next, we intersect it with regular languages that check cyclicity of the happens-before relation. Altogether, the program is robust iff the intersection is empty.

5.1 Generating Normal-Form Computations

To generate all normal-form computations, we use so-called multiheaded automata [8]. Essentially, a multiheaded automaton generates a computation $\sigma_1 \dots \sigma_n$ by simultaneously generating its parts σ_i . The automaton has a head for each part, and the transition relation defines the head producing an event. Formally, an *n-headed automaton over Σ* is an automaton operating on the extended alphabet $[1..n] \times \Sigma$: $A = (S, [1..n] \times \Sigma, \Delta, s_0, F)$. The *language of A* is $\mathcal{L}(A) := \{\text{second}(\sigma \downarrow (\{1\} \times \Sigma) \cdots \sigma \downarrow (\{n\} \times \Sigma)) \mid s_0 \xrightarrow{\sigma} s \text{ for some } s \in F\}$, where $\text{second}((a_1, b_1) \cdots (a_m, b_m)) := b_1 \cdots b_m$. Multiheaded automata are closed under intersection with regular languages. Moreover, for finite multiheaded automata language emptiness is NL-complete [8]:

Lemma 14 ([8]). *Consider an n -headed automaton U and a finite automaton V over a common alphabet Σ . There is an n -headed automaton W with $\mathcal{L}(W) = \mathcal{L}(U) \cap \mathcal{L}(V)$ with the number of states $|S_W| \leq |S_U| \cdot |S_V|^{2n} + 1$.*

Lemma 15 ([8]). *Emptiness for n -headed automata is NL-complete.*

We will generate all normal-form computations of program \mathcal{P} with the n -headed automaton $M(\mathcal{P}) := (S_M, E, \Delta_M, s_{0M}, F_M)$, where $n := |\mathcal{P}| + 3$. The automaton generates all events related to a single instruction in one shot, but,

possibly, in different parts of the computation. All `fetch` events are generated in the first part of the computation. In order to generate them, the automaton keeps track of the destination state of the last fetched instruction in each thread (component `ctrl-state` of the automaton state).

Each instruction can only read the last value written to a register. Therefore, the automaton only needs to remember $|\text{REG}|$ register values per thread (component `reg-value`). However, an instruction cannot be executed until the values of all registers that it reads become known. To obey this restriction, the automaton memorizes the part of the computation in which the register value gets computed (`reg-comp-head`). For example, while handling an assignment $r_1 \leftarrow r_1 + r_2$, the automaton learns that the new value of r_1 is the sum of the current values of r_1 and r_2 . It also remembers that this value is available no earlier than the current values of r_1 and r_2 are computed. Similarly, the automaton remembers the parts of the computation in which the addresses of load and store instructions become known (`addr-comp-head`), and certain kinds of instructions get committed (`reg-comm-head`, `assume-comm-head`, `addr-comm-head`).

The automaton has to keep a separate memory state for each thread and for each part of the computation. The memory state of a thread in a part is updated when a store instruction gets propagated to this thread in this part. When a load instruction is handled, the automaton chooses a part where the `load` event takes place and uses the memory state of that part. Besides the memory valuation (`mem-value`), the memory state includes coherence keys (`last-key`) to guarantee that the generated computation respects the coherence order.

When starting the computation, the automaton non-deterministically guesses the memory valuations and coherence keys for all parts of the computation (except the first one). Upon termination, the automaton checks that the parts of the computation generated by each head fit together at the concatenation points. This ensures the overall computation is valid for the program. The trick is to remember the guess of the initial memory valuations and coherence keys in immutable components of the automaton state (`mem-valueg`, `last-keyg`). The final states require that the current memory state in part h of the computation coincides with the guessed initial state in part $h + 1$.

State space A state from S_M (except the special initial state s_{0M}) includes the following information:

- `ctrl-state(tid)` gives the current control state of thread `tid`.
- `reg-comp-head(tid, r)` gives the part in which last value assigned to register r in thread `tid` gets computed.
- `reg-value(tid, r)` gives this computed value.
- `reg-comm-head(tid, r)` gives the part in which the last instruction assigning a value to register r in thread `tid` gets committed.
- `assume-comm-head(tid)` gives the part in which the latest fetched condition in thread `tid` is committed.
- `mem-value(tid, a, h)` gives the value of the last write to a propagated to thread `tid` in the part h or earlier.

- $\text{last-key}(\text{tid}, \mathbf{a}, \mathbf{h})$ gives the coherence key of the last write to \mathbf{a} propagated to thread tid in the part \mathbf{h} or earlier.
- mem-value_g , last-key_g are immutable copies of the guessed values of the previous two components (see MH-GUESS below).
- $\text{early-mem-value}(\text{tid}, \mathbf{a}, \mathbf{h})$ gives the value written by the last fetched store to \mathbf{a} which is still in-flight in the part \mathbf{h} of computation, \perp if there is no such store, \top if the value of the store is unknown or there is a later in-flight store in this part with an unknown address.
- $\text{addr-comp-head}(\text{tid})$ gives the leftmost part of the computation, in which the addresses of all already fetched memory accesses are computed.
- $\text{addr-comm-head}(\text{tid}, \mathbf{a})$ gives the rightmost part of the computation having a commit to address \mathbf{a} by thread tid .
- $\text{instr-count}(\text{tid})$ gives the number of instructions fetched in thread tid .

The initial state s_{0M} does not contain any information.

Transition relation We define transitions by specifying the new (primed) values of the state components and the label λ of the transition. First, we define the transition guessing the initial memory state in each part of the computation:

MH-GUESS Assume the current state is s_{0M} . Then, there are transitions to the states satisfying $\text{ctrl-state}' := \lambda \text{tid}. q_{0\text{tid}}$, $\text{reg-comp-head}' := \lambda \text{tid}. \lambda r. 1$, $\text{reg-value}' := \lambda \text{tid}. \lambda r. 0$, $\text{reg-comm-head}' := \lambda \text{tid}. \lambda r. 1$, $\text{assume-comm-head}' := \lambda \text{tid}. 1$, $\text{early-mem-value}' := \lambda \text{tid}. \lambda a. \lambda h. \perp$, $\text{mem-value}' = \text{mem-value}'_g$, $\text{last-key}' = \text{last-key}'_g$, $\text{addr-comp-head}' := \lambda \text{tid}. 1$, $\text{addr-comm-head}' := \lambda \text{tid}. \lambda a. 1$, $\text{instr-count}' := \lambda \text{tid}. 0$. Also, $\text{mem-value}'(\text{tid}, \mathbf{a}, 1) := 0$, $\text{last-key}'(\text{tid}, \mathbf{a}, 1) := 0$ for all $\text{tid} \in \text{TID}$, $\mathbf{a} \in \text{ADDR}$. Moreover, $\text{last-key}'(\text{tid}, \mathbf{a}, \mathbf{h}) \leq \text{last-key}'(\text{tid}, \mathbf{a}, \mathbf{h} + 1)$ for $\mathbf{h} \in [1..n - 1]$, $\text{tid} \in \text{TID}$, $\mathbf{a} \in \text{ADDR}$ (we assume $\text{last-key}'(\text{tid}, \mathbf{a}, n) := \infty$). $\lambda := \varepsilon$.

Fix a state s_M . We overload $\text{eval}(\text{tid}, e)$ to mean the value of expression e for the valuation of registers defined by $\lambda r. \text{reg-value}(\text{tid}, r)$.

Let $\text{HEAD} := [1..n]$. Let $\text{tid} \in \text{TID}$, $\text{ctrl-state}(\text{tid}) = q_1$, $\text{instr} = q_1 \xrightarrow{\text{cmd}} q_2 \in \mathcal{I}_{\text{tid}}$. Let $h_1 := 1$. Let $h_2 \in \text{HEAD}$, $h_2 \geq h_1$, $h_2 \geq \text{reg-comp-head}(\text{tid}, r)$ for each register r read in cmd . Let $h_3 \in \text{HEAD}$, $h_3 \geq h_2$, $h_3 \geq \text{reg-comm-head}(\text{tid}, r)$ for each register r read in cmd , $h_3 \geq \text{assume-comm-head}(\text{tid})$. Let $i := \text{instr-count}(\text{tid}) + 1$ and $\text{instr-count}' := \text{instr-count}[\text{tid} \leftarrow i]$. Depending on the type of cmd , there are the following transitions from s_M labeled by events λ :

MH-ASSIGN $\text{cmd} = r \leftarrow e_v$. Let $v := \text{eval}(\text{tid}, e_v)$. Then $\text{reg-value}' := \text{reg-value}[(\text{tid}, r) \leftarrow v]$, $\text{reg-comp-head}' := \text{reg-comp-head}[(\text{tid}, r) \leftarrow h_2]$, $\text{reg-comm-head}' := \text{reg-comm-head}[(\text{tid}, r) \leftarrow h_3]$. $\lambda := (h_1, \text{fetch}, \text{tid}, \text{instr}) \cdot (h_3, \text{commit}, \text{tid}, i)$.

MH-ASSUME $\text{cmd} = \text{assume}(e_v)$. Let $\text{eval}(\text{tid}, e_v) \neq 0$. Then $\text{assume-comm-head}' := \text{assume-comm-head}[\text{tid} \leftarrow h_3]$. $\lambda := (h_1, \text{fetch}, \text{tid}, \text{instr}) \cdot (h_3, \text{commit}, \text{tid}, i)$.

MH-LOAD $\text{cmd} = r \leftarrow \text{mem}[e_a]$. Let $a := \text{eval}(\text{tid}, e_a)$. Let $h_3 \geq \text{addr-comm-head}(\text{tid}, a)$. If $\text{early-mem-value}(\text{tid}, a) = \perp$, let $v := \text{mem-value}(\text{tid}, a, h_2)$ (load from memory case). Otherwise, let $v := \text{early-mem-value}(\text{tid}, a, h_2)$ and assume $v \neq \top$ (early read case). Then $\text{reg-value}' := \text{reg-value}[(\text{tid}, r) \leftarrow v]$, $\text{reg-comp-head}' := \text{reg-comp-head}[(\text{tid}, r) \leftarrow h_2]$, $\text{reg-comm-head}' := \text{reg-comm-head}[(\text{tid}, r) \leftarrow h_3]$, $\text{addr-comp-head}' := \text{addr-comp-head}[\text{tid} \leftarrow \max\{\text{addr-comp-head}(\text{tid}), h_2\}]$, $\text{addr-comm-head}' := \text{addr-comm-head}[(\text{tid}, a) \leftarrow h_3]$. $\lambda := (h_1, \text{fetch}, \text{tid}, \text{instr}) \cdot (h_2, \text{load}, \text{tid}, i, a) \cdot (h_3, \text{commit}, \text{tid}, i)$.

MH-STORE $\text{cmd} = \text{mem}[e_a] \leftarrow e_v$. Let $a := \text{eval}(\text{tid}, e_a)$. Assume $h_3 \geq \text{addr-comp-head}(\text{tid})$, $h_3 \geq \text{addr-comm-head}(\text{tid}, a)$. Let $v := \text{eval}(\text{tid}, e_v)$. Let $k \in \mathbb{Q}$, $k \neq \text{last-key}(\text{tid}, a, h)$ for any $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in \text{HEAD}$. Then $\text{early-mem-value}' := \text{early-mem-value}[(\text{tid}, a, [h_1..h_2 - 1]) \leftarrow \top, (\text{tid}, a, [h_2..h_3 - 1]) \leftarrow v]$. We also set $\text{early-mem-value}' := \text{early-mem-value}'[(\text{tid}, a', h) \leftarrow \top]$ for all $a' \in \text{ADDR} \setminus \{a\}$, $h \in [h_1..h_2 - 1]$ with $\text{early-mem-value}(\text{tid}, a', h) \in \text{DOM}$. We define $\text{addr-comp-head}' := \text{addr-comp-head}[\text{tid} \leftarrow \max\{\text{addr-comp-head}(\text{tid}), h_2\}]$, $\text{addr-comm-head}' := \text{addr-comm-head}[(\text{tid}, a) \leftarrow h_3]$. Let $T \subseteq \text{TID} \setminus \{\text{tid}\}$, initially $\text{mem-value}' := \text{mem-value}$, $\text{last-key}' := \text{last-key}$, and $\lambda := (h_1, \text{fetch}, \text{tid}, \text{instr}) \cdot (h_3, \text{commit}, \text{tid}, i, k, a)$. For $\text{tid}' = \text{tid}$ and for each $\text{tid}' \in T$: let $h \in \text{HEAD}$, $h \geq h_3$ ($h := h_3$ for $\text{tid}' = \text{tid}$), $\text{last-key}(\text{tid}', a, h) < k \leq \text{last-key}_g(\text{tid}', a, h+1)$, then $\text{mem-value}' := \text{mem-value}'[(\text{tid}', a, h) \leftarrow v]$, $\text{last-key}' := \text{last-key}'[(\text{tid}', a, h) \leftarrow k]$, $\lambda := \lambda \cdot (h, \text{prop}, \text{tid}', \text{tid}, i, a)$.

For brevity we allowed a single transition to be labeled by several events. An automaton with such transitions can be trivially translated to the canonical form by breaking one such transition into several consecutive ones.

Final states The set of final states F_M is a subset of $S_M \setminus \{s_{0M}\}$ consisting of all states with $\text{mem-value}(\text{tid}, a, h) = \text{mem-value}_g(\text{tid}, a, h+1)$, $\text{last-key}(\text{tid}, a, h) = \text{last-key}_g(\text{tid}, a, h+1)$ for all $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in [1..n-1]$.

Soundness and completeness

Lemma 16. $\mathcal{L}(M) \subseteq C_{\text{power}}(\mathcal{P})$.

Proof. Consider $\sigma = \lambda_1 \cdots \lambda_m$, such that $s_{0M} \xrightarrow{\lambda_1} s_{M1} \xrightarrow{\lambda_2} \cdots \xrightarrow{\lambda_m} s_{Mm} \in F_M$. For $h \in \text{HEAD}$, let $\tau_h^s := \text{second}((\lambda_1 \cdots \lambda_s) \downarrow (\{h\} \times E))$, $s \in [0..m]$.

Let $(s_Z^0 \dots s_Z^n) \in (S_Z)^n$ be the states of Z defined so that SND-B holds for $s = 0$ (see below). By induction on $s \in [1..m]$ we show:

SND-A $s_{Zh}^0 \xrightarrow{\tau_h^s} s_{Zh}^s$.

SND-B For all $\text{tid} \in \text{TID}$, $h \in \text{HEAD}$, $s_{Zh}^s = (\text{ts}, (\text{co}, \text{prop}))$, $\text{ts}(\text{tid}) = (\text{fetched}, \text{committed}, \text{loaded})$ holds:

- SND-B1** fetched is the list of instructions fetched by $(\tau_1^m \cdots \tau_{h-1}^m \cdot \tau_h^s) \downarrow \text{fetch} \downarrow \text{tid}$.
- SND-B2** committed consists of the indices of instructions committed by $(\tau_1^m \cdots \tau_{h-1}^m \cdot \tau_h^s) \downarrow \text{commit} \downarrow \text{tid}$.
- SND-B3** loaded contains the information about the stores being read by loads in $(\tau_1^m \cdots \tau_{h-1}^m \cdot \tau_h^s)$ determined according to Lemmas 4 and 5.
- SND-B4** $\text{co}(\text{tid}, i) = k$ if $(\text{commit}, \text{tid}, i, k, a) \in \tau_1^m \cdots \tau_{h-1}^m \cdot \tau_h^s$ for some $a \in \text{ADDR}$, otherwise, $\text{co}(\text{tid}, i) = \perp$.
- SND-B5** $\text{prop}(\text{tid}, a) = (\text{tid}', i')$ if $(\text{prop}, \text{tid}, \text{tid}', i', a) = \text{last}((\tau_1^m \cdots \tau_{h-1}^m \cdot \tau_h^s) \downarrow (\text{prop}, \text{tid}, *, *, a))$, otherwise, $\text{prop}(\text{tid}, a) = \text{init}_a$.
- SND-C** For each $\text{tid} \in \text{TID}$: $\text{ctrl-state}(\text{tid}) = \text{dst}(\text{last}(s_{Z_1^s}.\text{ts}(\text{tid}).\text{fetched}))$ (or $q_{0\text{tid}}$ if no instructions were fetched).
- SND-D** For each $\text{tid} \in \text{TID}$, $r \in \text{REG}$, for each $h \in [\text{reg-comp-head}(\text{tid}, r)..n]$: $\text{reg-value}(\text{tid}, r) = \text{eval}(\text{tid}, \text{instr-count}(\text{tid}) + 1, r)$ computed for the state $s_{Z_h^s}$.
- SND-E** For each $\text{tid} \in \text{TID}$, $r \in \text{REG}$, $h \in [\text{reg-comm-head}(\text{tid}, r)..n]$: let i be the index of the latest instruction in $s_{Z_h^s}.\text{ts}(\text{tid}).\text{fetched}$ writing to r , then $i \in s_{Z_h^s}.\text{ts}(\text{tid}).\text{committed}$.
- SND-F** For each $\text{tid} \in \text{TID}$, $h \in [\text{assume-comm-head}(\text{tid})..n]$: $s_{Z_h^s}$ does not contain uncommitted conditional instructions in thread tid having indices $\leq \text{instr-count}(\text{tid})$.
- SND-G** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in \text{HEAD}$: let $w := s_{Z_h^s}.\text{prop}(\text{tid}, a)$. If $w = \text{init}_a$, $\text{mem-value}(\text{tid}, a, h) = 0$. If $w = (\text{tid}', i')$, $\text{mem-value}(\text{tid}, a, h) = \text{val}(\text{tid}', i')$ computed in $s_{Z_h^s}$.
- SND-H** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in \text{HEAD}$: $\text{last-key}_g(\text{tid}, a, h) \leq s_{Z_h^s}.\text{co}(s_{Z_h^s}.\text{prop}(\text{tid}, a)) = \text{last-key}(\text{tid}, a, h) \leq \text{last-key}_g(\text{tid}, a, h + 1)$.
- SND-K** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in \text{HEAD}$: let $i \in \mathbb{N}$ be the maximal index, such that $s_{Z_h^s}.\text{ts}(\text{tid}).\text{fetched}[i]$ is a store, $\text{addr}(\text{tid}, i) = a$ in $s_{Z_n^s}$. Let i' be the maximal index, such that $s_{Z_h^s}.\text{ts}(\text{tid}).\text{fetched}[i']$ is a store, $\text{addr}(\text{tid}, i') \in \{\perp, a\}$ in $s_{Z_h^s}$. Then $\text{early-mem-value}(\text{tid}, i, h) = \perp$ if such i does not exist or $i \in s_{Z_h^s}.\text{ts}(\text{tid}).\text{committed}$. Otherwise, $\text{early-mem-value}(\text{tid}, i, h) = \top$ if $\text{addr}(\text{tid}, i') = \perp$ or $\text{val}(\text{tid}, i) = \perp$ in $s_{Z_h^s}$. Otherwise, $\text{early-mem-value}(\text{tid}, i, h) = \text{val}(\text{tid}, i)$ computed in $s_{Z_h^s}$.
- SND-L** For each $\text{tid} \in \text{TID}$, $h \in [\text{addr-comp-head}(\text{tid})..n]$, $i \in [1..|s_{Z_h^s}.\text{ts}(\text{tid}).\text{fetched}|]$: $\text{addr}(\text{tid}, i) \neq \perp$ in $s_{Z_h^s}$.
- SND-M** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in [\text{addr-comm-head}(\text{tid}, a)..n]$: if $\text{addr}(\text{tid}, i) = a$ in $s_{Z_n^s}$ for some i , then $i \in s_{Z_h^s}.\text{ts}(\text{tid}).\text{committed}$.

Finally we will show that $s_{Z_h^m} = s_{Z_{h+1}^0}$ for all $h \in [1..n - 1]$ and $s_{Z_n^m} \in F_Z$, thus proving the claim of the lemma.

Base case: $s = 1$, we must show that there s_{M_1} satisfies the inductive statement. This is easy to check by definition of the destination state of MH-GUESS transition.

Step case: assume the inductive statement holds for some $s \in [0..m - 1]$. Consider λ_s (for notational convenience and without loss of generality we assume below that $h_j \neq h_{j'}$ for $j \neq j'$):

Assignment $\lambda_s = (h_1, \text{fetch}, \text{tid}, \text{instr}) \cdot (h_3, \text{commit}, \text{tid}, i), \text{instr} = q_1 \xrightarrow{r \leftarrow e_v} q_2$.

Let $e_1 := (\text{fetch}, \text{tid}, \text{instr})$, $e_3 := (\text{commit}, \text{tid}, i)$.

We need to show that $s_{Z_{h_1}}^{s-1} \xrightarrow{e_1} s_{Z_{h_1}}^s$, i.e. that the assignment instruction can be fetched. This follows from the choice of $h_1 := 1$ in MH-ASSIGN and SND-B1, SND-C.

We also need to show that $s_{Z_{h_3}}^{s-1} \xrightarrow{e_3} s_{Z_{h_3}}^s$, i.e. that the assignment instruction can be committed. First, the e_3 transition requires the instruction being committed to be fetched, which holds due to SND-B1 and $h_3 \geq h_1$. Second, this instruction must be not committed yet, which holds by SND-B2 and the fact that M commits each instruction once and only once. Third, all control dependencies must be committed. This is by the choice of h_3 in MH-ASSIGN and SND-F. Fourth, all the preceding data dependencies must be committed. This is by the choice of h_3 in MH-ASSIGN and SND-E. Finally, the argument of the function must be computed. This is by choice of $h_3 \geq h_2$ in MH-ASSIGN, Lemma 3, and SND-D.

In the end, we must show that the invariants hold in the new state. The only non-trivial thing is SND-D, which holds due to SND-D, definition of v in MH-ASSIGN, definitions of eval , and the fact that functions in FUN are deterministic.

Assume $\lambda_s = (h_1, \text{fetch}, \text{tid}, q_1 \xrightarrow{\text{instr}} q_2) \cdot (h_3, \text{commit}, \text{tid}, i), \text{instr} = \text{assume}(e_v)$.

The proof is similar to the previous case. The **commit** transition additionally requires $\text{eval}(\text{tid}, i, e_v) \neq 0$, which holds due to the fact that a similar check in MH-ASSUME holds, SND-D, definitions of eval , the fact that functions in FUN are deterministic.

Load $\lambda_s = (h_1, \text{fetch}, \text{tid}, \text{instr}) \cdot (h_2, \text{load}, \text{tid}, i, a) \cdot (h_3, \text{commit}, \text{tid}, i), \text{instr} = r \leftarrow \text{mem}[e_a]$. Let $e_1 := (\text{fetch}, \text{tid}, \text{instr})$, $e_2 := (\text{load}, \text{tid}, i, a)$, $e_3 := (\text{commit}, \text{tid}, i)$.

$s_{Z_{h_1}}^{s-1} \xrightarrow{e_1} s_{Z_{h_1}}^s$ holds for the same reasons as before.

Next, we show that $s_{Z_{h_2}}^{s-1} \xrightarrow{e_2} s_{Z_{h_2}}^s$, where this transition is a POW-EARLY transition in the early read case of MH-LOAD and a POW-LOAD transition in the load from memory case. First, we must show that $s_{Z_h}^s.\text{ts}(\text{tid}).\text{loaded}[i] = \perp$. This holds by SND-B3 and the fact that M generates a **load** event once and only once for a single fetched load instruction.

Assume the early read case. This means, $\text{early-mem-value}(\text{tid}, a, h_2) \in \text{DOM}$. By SND-K, this means, the last fetched store with an unknown address or address of the load is not yet committed, has the address of the load and has the value known. By POW-EARLY, the load can take the value from this store, and SND-B3 holds in the new state.

Consider the load from memory case. This means, $\text{early-mem-value}(\text{tid}, a, h_2) = \perp$. By SND-K, this means, there is no earlier fetched store with the same address which is not yet committed. By POW-LOAD, the load can take the value from the last propagated store, and SND-B3 holds in the new state.

Argumentation for $s_{Z_{h_3}}^{s-1} \xrightarrow{e_3} s_{Z_{h_3}}^s$ is similar to the previous cases. Additionally, first we must show that $s_{Z_h}^s.\text{ts}(\text{tid}).\text{loaded}[i] \neq \perp$. This is by $h_3 \geq h_2$

(MH-LOAD), SND-B3. Second, we must ensure that all preceding instructions accessing the same address \mathbf{a} are committed, and there are no previously fetched instructions with unknown address. This holds by choice of \mathbf{h}_3 in MH-LOAD, SND-L, and SND-M.

In the new state, SND-D holds by definition of \mathbf{v} in POW-LOAD, definitions of eval, SND-G, and SND-K. Proofs for the other conditions are simpler.

Store $\lambda_s = (\mathbf{h}_1, \text{fetch}, \text{tid}, \text{instr}) \cdot (\mathbf{h}_3, \text{commit}, \text{tid}, i, \mathbf{k}, \mathbf{a}) \cdot (\mathbf{h}_3, \text{prop}, \text{tid}, \text{tid}, i, \mathbf{a}) \cdot (\mathbf{h}_4, \text{prop}, \text{tid}_1, \text{tid}, i, \mathbf{a}) \cdots (\mathbf{h}_{u+3}, \text{prop}, \text{tid}_u, \text{tid}, i, \mathbf{a})$. Let $\mathbf{e}_1 := (\text{fetch}, \text{tid}, \text{instr})$, $\mathbf{e}_3 := (\text{commit}, \text{tid}, i, \mathbf{k}, \mathbf{a})$, $\mathbf{e}_4 := (\text{prop}, \text{tid}, \text{tid}, i, \mathbf{a})$, $\mathbf{e}_{j+3} := (\text{prop}, \text{tid}_j, \text{tid}, i, \mathbf{a})$ for $j \in [1..u]$.

$s_{Z_{\mathbf{h}_1}}^{s-1} \xrightarrow{\mathbf{e}_1} s_{Z_{\mathbf{h}_1}}^s$ holds for the same reasons as before.

$s_{Z_{\mathbf{h}_3}}^{s-1} \xrightarrow{\mathbf{e}_3} s_{Z_{\mathbf{h}_3}}^s$ holds for the same reasons as in the case of a load. The requirement that the coherence key is unique in POW-STORE follows from a similar requirement in MH-STORE and SND-H. By POW-STORE, the only available transition from $s_{Z_{\mathbf{h}_2}}^s$ is a propagation of the write to its thread, i.e. \mathbf{e}_4 , which indeed follows \mathbf{e}_3 in τ . Next, we show that \mathbf{e}_4 and further propagate transitions are feasible.

First, POW-PROP rule requires the write being propagated to have a coherence key (i.e. to be committed), which holds by choice of \mathbf{h}_j , $j \in [3..u+3]$ in MH-STORE and SND-B2. Second, it requires the coherence key of the latest propagated store to be less than the key of the store being propagated. This is adhered due to the check $\text{last-key}(\text{tid}', \mathbf{a}, \mathbf{h}) < \mathbf{k}$ and SND-H.

It is easy to see that the inductive statements hold in the new state as well.

Now we prove $s_{Z_{\mathbf{h}}}^m = s_{Z_{\mathbf{h}+1}}^0$ for all $\mathbf{h} \in [1..n-1]$. The equality of **ts** components immediately follows from SND-B inductive statement.

Now we prove $s_{Z_n}^m \in F_Z$. FIN-COMM holds, because Z always emits a commit event for each fetched instruction.

Let us turn to FIN-LD property. First, one should note that M generates **prop** events for stores to the same address in each part τ_j in the ascending order by \mathbf{k} . This is by MH-STORE. Together with SND-H, this means that these events are sorted in τ in the ascending order by \mathbf{k} . The rest of the proof of FIN-LD is a simple case consideration: whether the loads i, i' were done from memory or from a local store early.

FIN-LD-ST is proven by a similar case consideration.

□

We call α a *prefix* of σ and write $\alpha \sqsubseteq \sigma$ if $\sigma = \alpha \cdot \beta$ for some β .

Lemma 17. $\{\tau \in C_{\text{power}}(\mathcal{P}) \mid \tau \text{ is in normal form of degree } n\} \subseteq \mathcal{L}(M)$.

Proof. Let $\tau = \tau_1 \cdots \tau_n \in C_{\text{mm}}(\mathcal{P})$ be a normal-form computation, i.e. $s_{0Z} \xrightarrow{\tau} s_Z \in F_Z$. We show that there is a sequence of transitions $s_{0M} \xrightarrow{\lambda_1} s_{M1} \xrightarrow{\lambda_2} \cdots \xrightarrow{\lambda_m} s_{Mm} \in F_M$, such that $\tau_{\mathbf{h}} = \text{second}((\lambda_1 \cdots \lambda_n) \downarrow (\{\mathbf{h}\} \times \mathbf{E}))$.

Let $\tau_{\mathbf{h}}^s := \text{second}((\lambda_1 \cdots \lambda_s) \downarrow (\{\mathbf{h}\} \times \mathbf{E}))$, $s_{0Z} \xrightarrow{\tau_1 \cdots \tau_{\mathbf{h}-1}, \tau_{\mathbf{h}}^s} s_{Z_{\mathbf{h}}}^s \rightarrow^* s_Z$. By induction on $s \in [1, \infty)$ we show the following inductive statements:

- CMPL-A** There is a sequence of s transitions: $s_{0M} \xrightarrow{\lambda_1} s_{M1} \xrightarrow{\lambda_2} \dots \xrightarrow{\lambda_s} s_{Ms}$.
- CMPL-B** For all $h \in \text{HEAD}$: $\tau_h = \tau_h^s \cdot \tau_h^s$ for some τ_h^s .
- CMPL-C** If $e_1, e_2 \in \tau$ are two events related to instruction (tid, i) , then $e_1 \in \tau_h^s$ for some h iff $e_2 \in \tau_{h'}^s$ for some h' .
- CMPL-D** For each $\text{tid} \in \text{TID}$: $\text{ctrl-state}(\text{tid}) = \text{dst}(\text{last}(s_{Z1}^s.\text{ts}(\text{tid}).\text{fetched}))$ (or $\text{ctrl-state}(\text{tid}) = q_{0\text{tid}}$ if no instructions were fetched).
- CMPL-F** For each $\text{tid} \in \text{TID}$, $r \in \text{REG}$, $h \in [\text{reg-comp-head}(\text{tid}, r)..n]$: $\text{reg-value}(\text{tid}, r) = \text{eval}(\text{tid}, \text{instr-count}(\text{tid}) + 1, r)$ computed for the state s_{Zh}^s .
- CMPL-F'** For each $\text{tid} \in \text{TID}$, $r \in \text{REG}$, $h \in [1..\text{reg-comp-head}(\text{tid}, r) - 1]$: $\text{eval}(\text{tid}, \text{instr-count}(\text{tid}) + 1, r) = \perp$.
- CMPL-G** For each $\text{tid} \in \text{TID}$, $r \in \text{REG}$, $h \in [\text{reg-comm-head}(\text{tid})..n]$: let i be the index of the last instruction in $s_{Zh}^s.\text{ts}(\text{tid}).\text{fetched}$ writing to r , then $i \in s_{Zh}^s.\text{ts}(\text{tid}).\text{committed}$.
- CMPL-G'** For each $\text{tid} \in \text{TID}$, $r \in \text{REG}$, $h \in [1..\text{reg-comm-head}(\text{tid}, r) - 1]$: let i be the index of the last instruction in $s_{Zh}^s.\text{ts}(\text{tid}).\text{fetched}$, then $i \notin s_{Zh}^s.\text{ts}(\text{tid}).\text{committed}$.
- CMPL-K** For each $\text{tid} \in \text{TID}$, $h \in [\text{assume-comm-head}(\text{tid})..n]$: let i be an index of an **assume**() instruction in $s_{Zh}^s.\text{ts}(\text{tid}).\text{fetched}$, then $i \in s_{Zh}^s.\text{ts}(\text{tid}).\text{committed}$.
- CMPL-K'** For each $\text{tid} \in \text{TID}$, $h \in [1..\text{assume-comm-head}(\text{tid}) - 1]$: let i be an index of the last **assume**() instruction in $s_{Zh}^s.\text{ts}(\text{tid}).\text{fetched}$, then $i \notin s_{Zh}^s.\text{ts}(\text{tid}).\text{committed}$.
- CMPL-L** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in \text{HEAD}$: let $w := s_{Zh}^s.\text{prop}(\text{tid}, a)$. If $w = \text{init}_a$, $\text{mem-value}(\text{tid}, a, h) = 0$. If $w = (\text{tid}', i')$, $\text{mem-value}(\text{tid}, a, h) = \text{val}(\text{tid}', i')$ computed in s_{Zh}^s .
- CMPL-M** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in \text{HEAD}$: $\text{last-key}_g(\text{tid}, a, h) < s_{Zh}^s.\text{co}(s_{Zh}^s.\text{prop}(\text{tid}, a)) = \text{last-key}(\text{tid}, a, h) \leq \text{last-key}_g(\text{tid}, a, h + 1)$.
- CMPL-N** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in \text{HEAD}$: let $i \in \mathbb{N}$ be the maximal index, such that $s_{Zh}^s.\text{ts}(\text{tid}).\text{fetched}[i]$ is a store, $\text{addr}(\text{tid}, i) = a$ in s_{Zh}^s . Let i' be the maximal index, such that $s_{Zh}^s.\text{ts}(\text{tid}).\text{fetched}[i']$ is a store, $\text{addr}(\text{tid}, i') \in \{\perp, a\}$ in s_{Zh}^s . Then $\text{early-mem-value}(\text{tid}, i, h) = \perp$ if such i does not exist or $i \in s_{Zh}^s.\text{ts}(\text{tid}).\text{committed}$. Otherwise, $\text{early-mem-value}(\text{tid}, i, h) = \top$ if $\text{addr}(\text{tid}, i') = \perp$ or $\text{val}(\text{tid}, i) = \perp$ in s_{Zh}^s . Otherwise, $\text{early-mem-value}(\text{tid}, i, h) = \text{val}(\text{tid}, i)$ computed in s_{Zh}^s .
- CMPL-P** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in [\text{addr-comm-head}(\text{tid}, a)..n]$: if $\text{addr}(\text{tid}, i) = a$ in s_{Zh}^s for some i , then $i \in s_{Zh}^s.\text{ts}(\text{tid}).\text{committed}$.
- CMPL-P'** For each $\text{tid} \in \text{TID}$, $a \in \text{ADDR}$, $h \in [1..\text{addr-comm-head}(\text{tid}, a) - 1]$: there is i with $\text{addr}(\text{tid}, i) = a$ in s_{Zh}^s , such that $i \in s_{Zh}^s.\text{ts}(\text{tid}).\text{committed}$.
- CMPL-R** For each $\text{tid} \in \text{TID}$: $\text{instr-count}(\text{tid}) = |s_{Z1}^s.\text{ts}(\text{tid}).\text{fetched}|$.

Base case: $s = 1$. We choose the first (MH-GUESS) transition $s_{0M} \xrightarrow{\lambda_1} s_{M1}$, so that the inductive statements hold:

Guess We define mem-value and last-key components of s_{M1} according to CMPL-L and CMPL-M requirements. The other inductive statements trivially hold.

Assume the inductive statements hold for s and $\overline{\tau}_h^s \neq \varepsilon$ for some $h \in \text{HEAD}$. We show they hold for $s' := s + 1$. The proof is done by pointing out an appropriate transition $s_{Ms} \xrightarrow{\lambda_{s+1}} s_{Ms+1}$. We choose the first possible option out of the following:

Assignment Assume $e_1 \sqsubseteq \overline{\tau}_{h_1}^s$, $e_3 \sqsubseteq \overline{\tau}_{h_3}^s$, where $h_1 < h_3$ ($h_1 = h_3$ is possible, but here and further we write strict inequalities for notational convenience), $e_1 := (\text{fetch}, \text{tid}, q_1 \xrightarrow{\text{cmd}} q_2)$, $e_3 := (\text{commit}, \text{tid}, i)$, $h_1 = 1$, $i = \text{instr-count}(\text{tid})$, $\text{cmd} = r \leftarrow e_v$. Then, as we show next, a MH-ASSIGN transition is feasible. First, $s_{Z_{h_1}}^s \xrightarrow{e_1}$, therefore, the state of the last fetched instruction in thread tid in $s_{Z_{h_1}}^s$ is q_1 . By CMPL-D, $\text{ctrl-state}(\text{tid}) = q_1$ too. Second, we choose $h_2 := \max\{\text{reg-comm-head}(\text{tid}, r) \mid r \text{ is read in cmd}\}$. It satisfies the requirements from MH-ASSIGN. Note that $h_2 \leq h_3$ by CMPL-F' and POW-COMMIT: an instruction cannot be committed, until its arguments are computed. Third, we must show that for each register r read by the instruction holds $h_3 \geq \text{reg-comm-head}(\text{tid}, r)$ and h_3 . This holds by CMPL-G', CMPL-K', and POW-COMMIT: an instruction cannot be committed until its data and control dependencies are committed. In the destination state, CMPL-F holds by CMPL-F in the source state, definition of $\text{reg-value}'$ in MH-ASSIGN and definitions of eval . The other inductive statements trivially hold.

Assume Assume $e_1 \sqsubseteq \overline{\tau}_{h_1}^s$, $e_3 \sqsubseteq \overline{\tau}_{h_3}^s$, where $h_1 < h_3$, $e_1 = (\text{fetch}, \text{tid}, q_1 \xrightarrow{\text{cmd}} q_2)$, $e_3 = (\text{commit}, \text{tid}, i)$, where $i = \text{instr-count}(\text{tid})$, $h_1 = 1$, $i = \text{instr-count}(\text{tid})$, $\text{cmd} = \text{assume}(e_v)$. Then, a MH-ASSUME transition is feasible.

The proof is similar to the proof for the case of assignment. The MH-ASSUME transition additionally requires $\text{eval}(\text{tid}, e_v) \neq 0$. This holds by CMPL-F, definition of $\text{reg-value}'$ in MH-ASSIGN and definitions of eval .

The inductive statements trivially hold in the destination state.

Load Assume $e_1 \sqsubseteq \overline{\tau}_{h_1}^s$, $e_2 \sqsubseteq \overline{\tau}_{h_2}^s$, $e_3 \sqsubseteq \overline{\tau}_{h_3}^s$, where $h_1 < h_2 < h_3$, $e_1 = (\text{fetch}, \text{tid}, q_1 \xrightarrow{\text{cmd}} q_2)$, $e_2 = (\text{load}, \text{tid}, i, a)$, $e_3 = (\text{commit}, \text{tid}, i)$, $i = \text{instr-count}(\text{tid})$, $\text{cmd} = r \leftarrow \text{mem}[e_v]$. We show that a MH-LOAD transition is feasible. We point out only differences with respect to the proof for the assignment case.

Assume e_2 was produced by a POW-EARLY transition. This means, the last store writing to a has its address known and is not committed yet in $s_{Z_{h_2}}^s$. Then, by CMPL-N, $\text{early-mem-value}(\text{tid}, a, h_2) \in \text{DOM}$, and we have $v := \text{early-mem-value}(\text{tid}, a, h_2)$. Assume e_2 was produced by a POW-LOAD transition. Then, POW-EARLY transition was not possible (Lemma 4, Lemma 5). This means, there was no in-flight stores to a in $s_{Z_{h_2}}^s$. Then, by CMPL-N, $\text{early-mem-value}(\text{tid}, a, h_2) = \perp$, and we have $v := \text{mem-value}(\text{tid}, a, h_2)$. In both cases, by CMPL-N, CMPL-L we have $\text{reg-value}'$ and $\text{reg-comp-head}'$ satisfying CMPL-F and CMPL-F'.

Additionally, we must show that $h_3 \geq \text{addr-comm-head}(\text{tid}, a)$. This holds by CMPL-P' and CMPL-N.

Store Assume $u \in \mathbb{N}$, $e_j \sqsubseteq \overline{\tau_{h_j}^s}$ for $j \in [1..u+3]$, where $h_2 = h_3$, $e_1 = (\text{fetch}, \text{tid}, q_1 \xrightarrow{\text{cmd}} q_2)$, $e_2 = (\text{commit}, \text{tid}, i, k, a)$, $e_3 = (\text{prop}, \text{tid}, \text{tid}, i, a)$, $e_j = (\text{prop}, \text{tid}_j, \text{tid}, i, a)$ for $j \in [4..u+3]$, $i = \text{instr-count}(\text{tid})$, $\text{cmd} = \text{mem}[e_a] \leftarrow e_v$. Assume that there are no other **prop** events for (tid, i) in τ , except for $e_3 \dots e_{u+3}$. We show that a MH-STORE transition is feasible. The requirements to be checked are similar to those in the load case. The requirement that k is not already used holds by CMPL-M and the fact that the same requirement in POW-STORE is met.

Consider the requirements in MH-STORE for generating **prop** events. The requirement that propagation event to thread tid is generated in the same part as **commit** is met by assumption $h_3 = h_2$. The requirement $\text{last-key}(\text{tid}', a, h) < k \leq \text{last-key}_g(\text{tid}', a, h+1)$ is met by CMPL-L, choice of last-key_g in the initial transition, and POW-PROP.

This means, inductive invariant CMPL-A holds for $s+1$. Also, CMPL-B holds by choice of $e_1 \dots e_{u+3}$, CMPL-D holds trivially. CMPL-C holds by assumption that there are no other **prop** events in τ , except for $e_3 \dots e_{u+3}$. CMPL-F, CMPL-F', CMPL-G, CMPL-G' hold as store instruction does not affect register values. CMPL-K, CMPL-K' hold as a store instruction is not **assume()**. CMPL-L holds by definition of $\text{mem-value}'$ in MH-STORE. CMPL-M holds by definition of $\text{last-key}'$ in MH-STORE. CMPL-N holds by definition of $\text{early-mem-value}'$ in MH-STORE. CMPL-P, CMPL-P' hold by definition of $\text{addr-comm-head}'$ in MH-STORE. CMPL-R hold by definition of $\text{instr-count}'$ in MH-STORE.

Now we must show that one of the cases above always takes place. Consider the event $e = \text{first}(\overline{\tau_1^s})$. By CMPL-C and the fact that $\tau \in \mathcal{C}_{\text{power}}(\mathcal{P})$, it is a **fetch** event $(\text{fetch}, \text{tid}, i, \text{instr})$. Choose the case based on the kind of instr . By NF-A and NF-B, all events related to the instruction (tid, i) constitute prefixes of $\overline{\tau_h^s}$, $h \in \text{HEAD}$. The requirement $i = \text{instr-count}(\text{tid})$ holds by CMPL-R. The requirements like $h_1 \leq h_2 \leq h_3$ in the load case naturally follow from the fact that $\tau \in \mathcal{C}_{\text{power}}(\mathcal{P})$.

Assume $\tau_h^s = \tau_h$ for all $h \in \text{HEAD}$. Then $\tau_h^s \in F_M$ by choice of mem-value_g and last-key_g in s_{M1} and CMPL-L, CMPL-M. □

Lemma 18. $\{\tau \in \mathcal{C}_{\text{power}}(\mathcal{P}) \mid \tau \text{ is in normal form of degree } n\} \subseteq \mathcal{L}(M(\mathcal{P})) \subseteq \mathcal{C}_{\text{power}}(\mathcal{P})$.

Proof. Corollary of Lemmas 16 and 17. □

5.2 Checking Cyclicity of the Happens-Before Relation

We call a happens-before cycle *beautiful*, if it has the following form:

$$\begin{aligned} (\text{tid}_1, i_1, \text{instr}_1) \rightarrow_{po}^* (\text{tid}_1, i'_1, \text{instr}'_1) \rightarrow_{hop} \dots \\ \rightarrow_{hop} (\text{tid}_n, i_n, \text{instr}_n) \rightarrow_{po}^* (\text{tid}_n, i'_n, \text{instr}'_n) \rightarrow_{hop} (\text{tid}_1, i_1, \text{instr}_1). \end{aligned}$$

Here, $\rightarrow_{hop} := (\rightarrow_{co} \cup \rightarrow_{src} \cup \rightarrow_{cf})$ and $\text{tid}_k \neq \text{tid}_l$ for $k \neq l$. We call $\theta := \text{tid}_1 \dots \text{tid}_n$ the *profile* of the cycle.

Example 4. The happens-before cycle shown in Figure 2 is beautiful.

Lemma 19 ([8]). *A computation $\tau \in C_{power}(\mathcal{P})$ has a happens-before cycle iff it has a beautiful happens-before cycle.*

Given a cycle profile θ , we define the automaton $M'(\mathcal{P}, \theta)$ as a modification of $M(\mathcal{P})$ that marks one event in each thread $\text{tid}_j \in \theta$ by **enter** (identifying $(\text{tid}_j, i_j, *)$) and a later (or the same) event by **leave** (identifying $(\text{tid}_j, i'_j, *)$, $i_j \leq i'_j$). Note that $M(\mathcal{P})$ generates the events in program order, which ensures $(\text{tid}_j, i_j, *) \rightarrow_{po}^* (\text{tid}_j, i'_j, *)$. Technically, $M'(\mathcal{P}, \theta)$ introduces the following changes:

- The alphabet is $E' := E \times 2^{\{\text{enter}, \text{leave}\}}$.
- The automaton generates only **load** and **prop** events, as only they are relevant for cycle detection.
- The **prop** events include **k** component of the corresponding **commit** event.

To check $(\text{tid}_j, i'_j, *) \rightarrow_{hop} (\text{tid}_{j+1}, i_{j+1}, *)$, we use an intersection with a regular language $H^{\text{tid}_j, \text{tid}_{j+1}}$. The language $H^{\text{tid}_1, \text{tid}_2}$ includes a computation τ iff one or more of the following conditions hold:

- H-ST** $(e_1, m_1), (e_2, m_2) \in \tau$, $\text{leave} \in m_1$, $\text{enter} \in m_2$, $e_1 = (\text{prop}, \text{tid}_1, \text{tid}_1, k_1, a)$, $e_2 = (\text{prop}, \text{tid}_2, \text{tid}_2, k_2, a)$, and $k_1 < k_2$.
- H-SRC** $\tau = \tau_1 \cdot (e_1, m_1) \cdot \tau_2 \cdot (e_2, m_2) \cdot \tau_3$, $\text{leave} \in m_1$, $\text{enter} \in m_2$, $e_1 = (\text{prop}, \text{tid}_2, \text{tid}_1, a)$, $e_2 = (\text{load}, \text{tid}_2, a)$, τ_2 does not contain events $(\text{prop}, \text{tid}_2, *, a)$.
- H-CF1** $\tau = \tau_1 \cdot (e_3, m_3) \cdot \tau_2 \cdot (e_2, m_2) \cdot \tau_3$, $\text{leave} \in m_2$, $e_3 = (\text{prop}, \text{tid}_1, \text{tid}_3, k_3, a)$, $e_2 = (\text{load}, \text{tid}_1, a)$, τ_2 does not contain events $(\text{prop}, \text{tid}_1, *, *, a)$, $(e_3, m_3) \in \tau_1 \cdot \tau_2 \cdot \tau_3$, $m_3 \in \text{enter}$, $e_3 = (\text{prop}, \text{tid}_2, \text{tid}_2, k_2)$, $k_3 < k_2$.
- H-CF2** $(e_1, m_1), (e_2, m_2) \in \tau$, $\text{enter} \in m_1$, $\text{leave} \in m_2$, $e_1 = (\text{load}, \text{tid}_1, a)$, $e_2 = (\text{prop}, \text{tid}_2, \text{tid}_2, k_2, a)$ and there is no $(e_3, m_3) \in \tau$ with $e_3 = (\text{prop}, \text{tid}_3, \text{tid}_3, k_3, a)$ with $k_3 < k_2$.

Lemma 20. *Program \mathcal{P} has a beautiful cycle with profile $\theta = \text{tid}_1 \dots \text{tid}_n$ iff*

$$M'(\mathcal{P}, \theta) \cap H^{\text{tid}_1, \text{tid}_2} \cap \dots \cap H^{\text{tid}_n, \text{tid}_1} \neq \emptyset.$$

Note that $M'(\mathcal{P}, \theta)$ is infinite-state. To ensure $M'(\mathcal{P}, \theta)$ has finitely many states, we note that the instruction indices are irrelevant for the detection of happens-before cycles (**instr-count** can be dropped), and that the number of different coherence keys that must be stored in the state at any moment is polynomial in the size of \mathcal{P} . Indeed, the **last-key** and **last-key_g** components of the state each store at most $|\text{ADDR}| \cdot |\mathcal{P}| \cdot n$ different coherence keys. Each modification of the **last-key** component of the state can be extended by a normalization step that would turn coherence keys to consecutive natural numbers starting from zero.

The normalization step must preserve the less-than relation on the keys. In order for the detection of happens-before cycles to work correctly, the automaton has to remember the coherence keys of marked store events: they must be preserved during normalization. Altogether, this results into $O(|\text{ADDR}| \cdot |\mathcal{P}|^2 \cdot n)$ different keys, which is polynomial in the size of \mathcal{P} .

Theorem 2. *Robustness against Power is PSPACE-complete.*

Proof. By Theorem 1, Lemma 19, and Lemma 20, a program is non-robust iff the equation from Lemma 20 holds for some θ . In order to check robustness, we enumerate all profiles θ and check the equation from Lemma 20. The enumeration can be done in PSPACE. By construction and Lemma 14, the size of the intersection automaton is exponential in the size of the program. By Lemma 15, language emptiness for it can be checked in PSPACE in the size of the program, which gives us the upper bound.

The PSPACE lower bound follows from PSPACE-hardness of SC state reachability. One can reduce reachability to robustness by inserting an artificial happens-before cycle in the target state. \square

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