

Network-on-Chip Architectures

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Network-on-Chip Architectures

A Holistic Design Exploration

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Abstract

The continuing reduction of feature sizes into the nanoscale regime has led to dramatic increases in transistor densities. Computer architects are actively pursuing multi-core designs with billions of transistors on a single die. Integration at these levels has highlighted the criticality of the on-chip interconnects; global interconnect delays are dominating gate delays and affecting overall system performance. Packet-based Network-on-Chip (NoC) architectures are viewed as a possible solution to burgeoning global wiring delays in many-core chips, and have recently crystallized into a significant research domain. NoCs are steadily becoming the de facto interconnect solution in complex Systems-on-Chip (SoC), because of their scalability and optimized electrical properties. However, current research also indicates that the chip area and power budgets are increasingly being dominated by the interconnection network. To combat this escalating trend, attention should be paid to the optimization of the interconnect architecture.

Unlike traditional multi-computer macro-networks, on-chip networks instill a new flavor to communication research due to their inherently resource-constrained nature. Scarcity in the area and power budgets devoted to the interconnection fabric necessitates a re-interpretation of the networking paradigm. Furthermore, despite the lightweight character demanded of the NoC components, modern designs require ultra-low communication latencies in order to cope with inflating data bandwidths. These conflicting requirements transform the NoC design process into a grand challenge for the system designer. The work presented in this volume aims to address these issues through a comprehensive and holistic exploration of the design space. To truly appreciate the nuances underlying the NoC realm, the design aspects of the on-chip network are viewed through a penta-faceted prism encompassing five major issues: (1) *performance*, (2) *silicon area consumption*, (3) *power/energy efficiency*, (4) *reliability*, and (5) *variability*. These five aspects serve as the fundamental design drivers and critical evaluation metrics in the quest for efficient NoC implementations.

The research described in this volume explores the field by employing a two-pronged approach: (a) *MICRO-architectural innovations* within the major NoC components, and (b) *MACRO-architectural choices* aiming to seamlessly merge the interconnection backbone with the remaining system modules. These two research threads, along with the aforementioned five key metrics mount a holistic and in-depth attack on most issues surrounding the design and integration of NoCs

in modern multi-core architectures. Based on this premise of two complementary core themes, the volume is divided into two corresponding parts; the first part delves into the world of MICRO-architectural exploration of the NoC paradigm, while the second part shifts the focus to a MACRO-architectural abstraction level. Ultimately, both parts work in unison in attacking several pressing issues concerning on-chip interconnects in the new multi/many-core reality.

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List of Abbreviations

AC	Allocation comparator
ACK	Acknowledgment
ACLV	Across chip line-width variations
AD	Adaptive
AG	Affinity group
ASIC	Application specific integrated circuits
BC	Bit-complement
BIST	Built-in self-test
CB	Connection box
CC	Cache compression
CDMA	Code-division multiple access
CMOS	Complementary metal-oxide semiconductor
CMP	Chip multi-processor
CPU	Central processing unit
DAMQ	Dynamically allocated multi-queue
DAMQWR	DAMQ-with-recruit-registers
DEMUX	De-multiplexer (i.e. decoder)
DimDe	Dimensionally decomposed router
DLT	Direction lookup table
DN	Direct neighbor
DNUCA	Dynamic non-uniform cache architecture
DOR	Dimension-order routing
DRAM	Dynamic random access memory
DT	Deterministic
dTDMA	Dynamic time-division multiple access
E2E	End-to-end
ECC	Error correcting codes
EDP	Energy-delay product
EM	Electromigration
F2B	Face-to-back
F2F	Face-to-face
FBF	Fullest buffer first

FC-CB	Fully connected circular buffer
FCFS	First-come first-served
FEC	Forward error correction
FIFO	First-in first-out
FP	Fast path
HBH	Hop-by-hop
HCE	Hot carrier effects
HDL	Hardware description language
HoL	Head-of-line
IIL	Inter-intra layer
ILP	Instruction-level parallelism
IN	Indirect neighbor
IP	Intellectual property
IS	Information set
LCR	Leakage classification register
LWF	Longest wait first
MEMS	Micro-electro-mechanical systems
MEP	Multiple entry point
MESI	Modified-exclusive-shared-invalid
MLBS	Multi-layer buried structures
MPSoC	Multi-processor system-on-chip
MSI	Modified-shared-invalid
MUX	Multiplexer
NACK	Negative acknowledgment
NBTI	Negative bias temperature instability
NC	Network interface controller compression
NetInMem	Network-in-memory
NIC	Network interface controller
NoC	Network-on-chip
NR	Normal random
NUCA	Non-uniform cache architecture
OPC	Optical proximity correction
PA	Proximity-aware
PBD	Platform-based design
PC	Physical channel
PDP	Power-delay product
PE	Processing element
PEF	Performance, energy and fault-tolerance
PFA	Path frequency analyzer
PFT	Path frequency table
PIM	Parallel iterative matching

PS	Path set
PTM	Predictive technology model
PV	Process variation
QoS	Quality-of-service
RC	Routing computation
RDF	Random dopant fluctuations
RoCo	Row-column decoupled router
RT	Routing table
RTL	Register-transfer level
SA	Switch allocation
SEC/DED	Single error correction and double error detection
SER	Soft-error rate
SIMD	Single-instruction multiple-data
SIP	Service information provider
SNUCA	Static non-uniform cache architecture
SoC	System-on-chip
SOI	Silicon-on-insulator
SON	Service-oriented networking
SS	Self-similar
ST	Sliding timeslice
STB	Set-top box
STI	Sony, Toshiba, and IBM
TDDB	Time-dependant dielectric breakdown
TDMA	Time-division multiple access
TLP	Thread-level parallelism
TMR	Triple module redundancy
TN	Tornado
TPA	Thermal proximity-aware
TSMC	Taiwan Semiconductor Manufacturing Company
TTM	Time-to-market
UBS	Unified buffer structure
UCL	Unified control logic
UR	Uniform random
UTP	Unique-Token protocol
VA	Virtual channel arbitration
VC	Virtual channel
VCDAMQ	Virtual channel dynamically allocated multi-queue
ViChR	Virtual channel regulator
XBAR	Crossbar