Efficient Test Methodologies for High-Speed Serial Links

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This book is dedicated to Joomi, my wife.

Preface

With the increasing demand for higher data bandwidth, communication systems' data rates have reached the multi-gigahertz range and even beyond. Advances in semiconductor technologies have accelerated the adoption of high-speed serial interfaces, such as PCI-Express, Serial-ATA, and XAUI, in order to mitigate the high pin-count and the data-channel skewing problems. However, with the increasing number of I/O pins and greater data rates, significant challenges arise for testing high-speed interfaces in terms of test cost and quality, especially in high volume manufacturing (HVM) environments.

This dissertation proposes novel testing techniques for high-speed interfaces, which can significantly reduce testing costs while maintaining high test coverage. The primary focus is on efficient testing methods for jitter and bit-error-rate (BER), which are widely used to represent the quality of a communication system. The reader is assumed to have a basic understanding of high-speed I/O and its test methodologies.

There are eight chapters in this dissertation. Chapter 1 gives a general introduction to high-speed I/O systems and describes commonly used testing methods along with their limitations.

Chapter 2 presents an efficient jitter measurement technique using fast comparator sampling. The comparator under-sampling technique is discussed, followed by the efficient jitter calculation algorithm. To validate the accuracy of the technique, the experimental setup and results using a high-speed sampling prototype and various types of measurement instruments are presented.

The BER estimation technique for high-speed serial links that incorporate the linear clock and data recovery (CDR) circuit is described in Chapter 3. The jitter transfer characteristics of the linear CDR loop are analyzed based on the conventional phase-locked loop (PLL) theory. This chapter then describes how the input jitter and the CDR circuit's internal jitter affect the recovered clock jitter and the dependency of the BER on the characteristics of the CDR circuit. The BER estimation technique is extended to the serial links which incorporate the bang-bang (BB) CDR circuit. This method is explained in Chapter 4. Due to the highly non-linear characteristics of the BB CDR loop, the jitter transfer function of the loop strongly varies depending on the input jitter magnitude. Thus, the loop's dependency on the jitter magnitude is fully characterized for accurate BER estimation.

Chapter 5 first reviews the basic concepts of the timing margining test, which is a widely adopted design-for-test (DFT) technique. Then, this chapter describes four possible gaps that the timing margining test might have compared to conventional jitter testing. Chapter 6 deals with the total jitter (TJ) estimation technique for improving the quality of the timing margining test, which can accurately predict the TJ at a very low BER level using only the information from the higher BER region. The limitations of the existing TJ estimation method, which is based on the dual-Dirac model, is described, and then a high-order polynomial fitting technique is proposed to overcome the limitations.

A two-tone testing method for continuous-time adaptive equalizers is described in Chapter 7. This chapter starts with an introduction to the continuous-time adaptive equalizers. Then, the proposed two-tone testing method is described followed by the transistor-level implementation details of the technique.

Chapter 8 concludes the dissertation by summarizing the results of the research conducted and discussing possible future research areas.

This research could not be accomplished without guidance and support of professors, colleagues, family members, and friends. First of all, I would like to thank my advisor, Professor Tim Cheng, for his endless support and great advice during the challenging periods. I feel grateful and privileged to have worked with him. I would also like to thank a number of professors and professionals who reviewed the dissertation and gave me helpful feedback: Professor Forrest D. Brewer, Professor Stephen I. Long, Professor Patrick Yue, and Dr. Mike P. Li.

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