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Regular Nanofabrics in Emerging Technologies

Design and Fabrication Methods for Nanoscale Digital Circuits

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Contents

List of Acronyms

1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
AFM	Atomic force microscope
AHC	Arranged hot code
Al	Aluminum
ALD	Atomic layer deposition
As	Arsenic
ASIC	Application specific integrated circuits
Au	Gold
BGC	Balanced gray code
BHF	Buffered HF
BRC	Binary reflexive code
BTB	Band-to-band
CAD	Computer-aided design
Ce	Cerium
CF	Coupling fault
CG	Control gate
Cl	Chlorine
CLB	Complex logic block
CNT	Carbon nanotube
CNTFET	Carbon nanotube field effect transistor
Cr	Chromium
CMI	Center of micro- and nano-technologies [1]
CMOL	CMOS/molecular hybrid
CMOS	Complementary metal oxide semiconductor
CMP	Mechanical–chemical planarization or mechanical–chemical polishing
CVD	Chemical vapor deposition

DIBL	Drain induced barrier lowering
DRIE	Deep reactive Ion etching
E-beam	Electron beam
EDA	Electronic design automation
EDP	Energy-delay-product
EOT	Equivalent oxide thickness
EPFL	Ecole Polytechnique Fédérale de Lausanne, Swiss Federal Institute of Technology at Lausanne
EUV	Extreme ultraviolet
EUV-IL	Extreme ultraviolet interference lithography
F	Fluorine
FET	Field effect transistor
FIB	Focused ion beam
FO4	Fan-out-of-4
FPGA	Field programmable gate array
Ga	Gallium
GAOI	Generalized AOI, generalized AND-OR-Inverter
GC	Gray code
Ge	Germanium
GIDL	Gate-induced drain leakage
GNAND	Generalized NAND
GNOR	Generalized NOR
HC	Hot code
HMDS	Hexamethyldisilazane ($C_6H_{19}Si_2N$)
IC	Integrated circuit
In	Indium
IST	Iterative spacer technique
ITRS	International technology roadmap for semiconductors
Kr	Krypton
LB	Langmuir–Blodgett
LPCVD	Low pressure chemical vapor deposition
LTO	Low temperature oxide
LUT	Look-up table
MEMS	Microelectromechanical system
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MSPT	Multi-spacer patterning technique
MVL	Multi-valued logic
MW	Mesowire
N	Nitrogen
Ni	Nickel
NIL	Nanoimprint lithography

NoC	Network-on-chip
NRC	*n*-Ary reflexive code
NW	Nanowire
O	Oxygen
OP	Operating point
OPC	Optical proximity correction
PANI	Polyanilin
PD	Pull-down
PDMS	Polydimethylsiloxane $[(C_2H_6OSi)_n]$
PEDAL	Planar edge defined alternate layer
PEO	Polyethylene oxide, polyethylene glycol $(C_{2n+2}H_{4n+6}O_{n+2})$
PG	Polarity gate
PLA	Programmable logic array
PMMA	Polymethylmethacrylate $[(C_5O_2H_8)_n]$
Poly-Si	Poly-crystalline silicon
Poly-SiNWFET	Poly-crystalline silicon field effect transistor
PR	Photoresist
PSF	Pattern sensitivity fault
Pt	Platinum
PU	Pull-up
Q-bit	Quantum bit
QCA	Quantum cellular automata
QWFET	Quantum well field effect transistor
RAM	Random access memory
RDR	Restrictive design rules
RET	Resolution enhancement techniques
RIE	Reactive ion etching
RTD	Resonant tunneling diode
S	Sulfur
Sb	Antimony
SB	Schottky barrier
SCE	Short channel effect
SEM	Scanning electron microscopy
SET	Single-electron transistors
Si	Silicon
SiNW	Silicon nanowire
SiNWFET	Silicon nanowire field effect transistor
SNAP	Superlattice nanowire pattern transfer
SoC	Systems-on-chip
SOI	Silicon-on-insulator
SRAM	Static random access memory
TC	Tree code
TEM	Transmission electron microscopy

Ti	Titanium
ULSI	Ultra large scale integration
VLS	Vapor–liquid–solid
VLSI	Very large scale integration
VPGA	Via patterned gate array
WPLA	Whirlpool PLA, Whirlpool programmable logic array

Reference

1. Center for Micro- and Nanotechnologies (CMI) at EPFL. http://cmi.epfl.ch

List of Symbols

Symbol	Definition	Unit
α	(i) Half-spacing between successive threshold voltages normalized to V_0	1
	(ii) Counter variable	1
β	Transistor gain factor $\mu C_{\text{ox}} W/L$	AV^{-2}
β_i	β at transistor i	
δ	Shift of any $V_{\text{X},i}$ from $V_{\text{A},i}$ normalized to V_0	1
ΔV_{T}	Distance between two successive $V_{\text{T},i}$'s	V
$\delta(x)$	(i) Dirac distribution around $\text{x} = 0$	$\varnothing$
	(ii) Kronecker delta function	$\varnothing$
δI	Small signal of I	A
$\delta I_{\text{d},i}$	Small signal of $I_{\text{d},i}$	A
δI_{u}	Small signal of I_{u}	A
δV_{DS}	Small signal of V_{DS}	V
$\delta V_{\text{DS},i}$	δV_{DS} at transistor i	V
δV_{DS}	Vector of $\delta V_{\text{DS},i}$	V (vector)
δV_{GS}	Small signal of V_{GS}	V
$\delta V_{\text{GS},i}$	δV_{GS} at transistor i	V
δV_{T}	Small signal of V_{T}	V
$\delta V_{\text{T},i}$	δV_{T} at transistor i	V
δV_{T}	Vector of $\delta V_{\text{T},i}$	V (vector)
ϵ	Test error probability	1
η	(i) Statistical factor $\eta = P_{\text{nbr}} \times P_{\text{unq}} \times P_{\text{cnt}} \times P_{\text{int}}$	1
	(ii) Sensitivity of V_{DS} to V_{T} in a decoder under test	1
η^{BU}	Statistical η for bottom-up technologies	1
η^{TD}	Statistical η for top-down technologies	1
Φ	Fabrication complexity $\Phi = \sum \phi_i$	1
ϕ_i	Number of photolithography/doping steps at MSPT step i	1
μ_α	Average number of code words having α identical digits	1
ν	Average number of patterns covered by a code word under defects	1

(continued)

(continued)

Symbol	Definition	Unit
Ω	Code space	$\varnothing$
Ω'	Addressable code space under defects	$\varnothing$
$\lvert\Omega\rvert_{\mathrm{un}}$	Size of uniquely addressed code space	$\varnothing$
$\lvert\Omega\rvert_{\mathrm{im}}$	Size of immune code space	$\varnothing$
$\mathbf{\Sigma}$	Variability matrix	V^2 (matrix)
$\sigma(x)$	Sigmoid function of x	$\varnothing$
σ	Threshold voltage standard deviation ($=\sigma_{\mathrm{T}}$)	V
$\sigma_{\delta\mathrm{d},i}$	Standard deviation of $\delta I_{\mathrm{d},i}$	A
$\sigma_{\delta\mathrm{u}}$	Standard deviation of δI_{u}	A
$\sigma_{\mathrm{d},i}$	Standard deviation of $I_{\mathrm{d},i}$	A
$\sigma_{\mathrm{d}}^{N_{\mathrm{def}}}$	Standard deviation of $I_{\mathrm{d}}^{N_{\mathrm{def}}}$	A
σ_{T}	Standard deviation of V_{T}	V
σ_{u}	Standard deviation of I_{u}	A
τ	(i) Number of digits that flip in order to generate defect-induced noise (context of decoder design)	1
	(ii) Intrinsic delay of fan-out-of-1 inverter (context of ambipolar CNTFET)	s
$\overline{\tau}$	Mean value of number of digits τ	1
υ	(i) Normalized shift of V_{A} from middle of two successive threshold voltages normalized to V_0	1
	(ii) counter variable	1
A	(i) Pattern space	$\varnothing$
	(ii) Event of having $I_{\mathrm{l}} \leq I_{\mathrm{s}}$	$\varnothing$
$\mathbf{A}$	First linearization matrix of the decoder	1 (matrix)
B	Event of having defect-induced noise, $B = \cup B_i$	$\varnothing$
B_i	Event of having exactly i nanowires generating defect-induced noise	$\varnothing$
$\mathbf{B}$	Second linearization matrix of the decoder	1 (matrix)
$\mathbf{a}$	Pattern	1 (vector)
$\mathbf{b}$	Pattern	1 (vector)
$\mathbf{b}^*$	Defective pattern	1 (vector)
C_{eff}	Effective crossbar (or memory) density	cm^{-2}
$C_{\mathrm{eff}}^{\mathrm{BU}}$	Effective crossbar (or memory) density in bottom-up technologies	cm^{-2}
$C_{\mathrm{eff}}^{\mathrm{TD}}$	Effective crossbar (or memory) density in top-down technologies	cm^{-2}
$\mathbf{c}$	Code word	1 (vector)
$\mathbf{c}^*$	Defective code word	1 (vector)
$\mathbf{c}^a$	Code word to the pattern a	1 (vector)
$\mathbf{c}^b$	Code word to the pattern b	1 (vector)
$\mathbf{d}$	Multi-digit error vector	1 (vector)
D	(i) Crosspoint density, memory density	cm^{-2}
	(ii) Elements of error subtree	$\varnothing$
D_{RAW}	Raw crosspoint (memory) density	cm^{-2}
D_{EFF}	Effective crosspoint (memory) density	cm^{-2}

(continued)

(continued)

Symbol	Definition	Unit
f	(i) Probability distribution function	$\varnothing$
	(ii) Photolithography half-pitch	nm
	(iii) Non-linear bijective application between N_D and V_T	$\varnothing$
f_u	Probability distribution function of useful signal	$\varnothing$
f_d^i	Probability distribution function of defect-induced noise generated by nanowire i	$\varnothing$
f_d	Probability distribution function of total defect-induced noise	$\varnothing$
g	Bijective application between pattern and V_T	$\varnothing$
g_{DS}	Output conductance of a FET	S
g_m	Transconductance of a FET	S
g_T	Sensitivity of I_{DS} to V_T: $\partial I_{DS}/\partial V_T$	S
h	Non-linear bijective application between elements of **D** and those of **P**	$\varnothing$
D	Doping matrix	cm^{-3} (matrix)
I	Unit $M \times M$-matrix	1 (matrix)
I	Current through a nanowire under test	A
i	Counter variable	1
I_0	First thresholder parameter	A
I_1	Second thresholder parameter	A
$\overline{I}_{\delta d,i}$	Mean value of $\delta I_{d,i}$	A
$\overline{I}_{\delta u}$	Mean value of δI_u	A
I_d	Defect-induced noise in decoder under test	A
$I_{d,i}$	Defect-induced noise generated by nanowire i	A
$\overline{I}_{d,i}$	Mean value of $I_{d,i}$	A
$I_d^{N_{def}}$	Total defect-induced noise: $\sum I_{d,i}$	A
$\overline{I}_d^{N_{def}}$	Mean value of $I_d^{N_{def}}$	A
I_{ds}	Drain-source current	A
I_i	Intrinsic noise in decoder under test	A
$I_{i,0}$	Intrinsic noise generated by a single nanowire in decoder under test	A
I_{off}	Transistor off-current	A
I_{on}	Transistor on-current	A
I^{OP}	Operating point of I	A
I_s	Sensed signal in decoder under test $= I_u + I_d + I_i$	A
I_u	Useful signal	A
$\overline{I}_u$	Mean value of I_u	A
j	Counter variable	1
k	(i) Parameter of optimal-size multi-valued hot code	1
	(ii) Counter variable	1
k	Parameter vector of multi-valued hot code	1 (vector)
L	Transistor length	nm
L_l	Photolithography pitch	nm
L_n	Sub-photolithographic pitch, nanoscale pitch	nm

(continued)

(continued)

Symbol	Definition	Unit
M	Length of code word, number of doping sequences in a nanowire (equivalent definitions)	1
N	Number of nanowires in a contact groups	1
N_{D}	Doping level (donors or acceptors)	cm^{-3}
N_{def}	Number of nanowires generating defect-induced noise in a decoder under test	A
N_{off}	Number of non-activated nanowires in a decoder under test	A
N_{use}	Number of useful nanowires in a decoder under test ($N_{\mathrm{use}} = 0$ or 1)	A
n	Logic value	1
$\mathbf{P}$	Pattern matrix	1 (matrix)
P_0	Probability that no nanowire is addressed	1
P_1	Probability that 1 nanowire is addressed	1
P_2	Probability that ≥ 2 nanowires are addressed	1
P_{cnt}	Probability of a good nanowire control	1
P_{contact}	Probability of a good nanowire ohmic contact	1
P_{int}	Probability of no nanowire loss at the interface between contact groups	1
P_{nbr}	Probability of a non-broken nanowire	1
P_{unq}	Probability of a unique nanowire	1
p_{I}	Probability of a type-I error in a code space	1
p_{II}	Probability of a type-II error in a code space	1
p_α	Probability that μ_α code words undergo error sequences that make them covered	1
p_{d}	Probability of a flip-down error in a code word	1
p_{im}	Probability of an immune code space	1
p_{u}	Probability of a flip-up error in a code word	1
p_{U}	Probability of a uniquely covered code space	1
q	On/off current ratio to detect a digit	1
r_i	$R_{\mathrm{M}} \| g_{\mathrm{m},i}$	Ω
R_{M}	Resistance of the nanowire memory part	Ω
S	(i) Set of all (p_α, μ_α)	$\varnothing$
	(ii) Set of indexes of digits that undergo flip-ups	$\varnothing$
$\mathbf{S}$	Step doping matrix	cm^{-3} (matrix)
s	Sequence digit shifts to generate defect-induced noise	1 (vector)
$\mathcal{T}$	Error transformation matrix	$\varnothing$
$\mathbf{t}^i$	Error transformation affecting digit level i	$\varnothing$
$\mathbf{V}$	Threshold voltage matrix	V (matrix)
$\mathbf{v}$	Vector with all entries set to 1	1 (vector)
V_+	V_{PG} for n-type device	V
V_-	V_{PG} for p-type device	V
V_0	(i) Decoder normalization voltage, set to V_{DD} (context of decoder test)	V

(continued)

(continued)

Symbol	Definition	Unit
	(ii) V_{PG} for a low-conductivity transistor (context of ambipolar CNTFET)	V
V_A	Applied voltage at the decoder (gate-to-ground voltage)	V
$V_{A,i}$	V_A at transistor i	V
V_{CG}	Control gate voltage (ambipolar CNTFET)	V
V_{DD}	Supply voltage	V
V_{ds}	Drain-source voltage (context of measurement)	V
V_{DS}	Drain-source voltage (context of testing)	V
$V_{DS,i}$	V_{DS} at transistor i	V
V_{gs}	Gate-source voltage (contest of measurement)	V
V_{GS}	Gate-source voltage (context of testing)	V
$V_{GS,i}$	V_{GS} at transistor i	V
V_P	Power supply of decoder under test	V
V_{PG}	Polarity gate voltage (ambipolar CNTFET)	V
V_{SS}	Ground, reference voltage	V
V_T	Threshold voltage	V
$\overline{V}_T$	Mean value of V_T	V
$\overline{\mathbf{V}}_T$	vector of $\overline{V}_{T,i}$	V (vector)
$\overline{V}_{T,i}$	$\overline{V}_T$ at transistor i	V
$\mathbf{V}_T$	Vector of $V_{T,i}$	V (vector)
$\mathbf{V}_T^{OP}$	$\mathbf{V}_T$ at operating point	V (vector)
$V_{T,i}$	V_T at transistor i	V
$V_{X,i}$	Threshold voltage to detect digit i	V
V_{Tn}	Threshold voltage of n-type device	V
V_{Tp}	Threshold voltage of p-type device	V
W	Transistor width	nm
Y	Statistical yield	1