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Brajesh Kumar Kaushik · Sudeb Dasgupta
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VLSI Design and Test

21st International Symposium, VDAT 2017
Roorkee, India, June 29 – July 2, 2017
Revised Selected Papers

Springer

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Preface

VLSI Design and Test (VDAT) is a leading event of the VLSI Society of India. The 21st symposium in this series, the VLSI Design and Test Symposium (VDAT 2017), was held from June 29 to July 2, 2017, at the Indian Institute of Technology Roorkee, India. The objective of the symposium is to bring professional engineers, academics, and researchers from India and abroad to discuss emerging topics of VLSI and related fields on a common platform and to share new ideas, experiences, and knowledge. The chief guest at the event was Dr. V. K. Saraswat, Padma Shri, Padma Bhushan, Member NITI Aayog.

The scientific program consisted of peer-reviewed paper presentations in parallel technical sessions. In addition, keynote lectures, presentations by industry professionals, panel discussions, tutorials, and a poster presentation were conducted during the conference. Research contributions in the following areas were invited for VDAT 2017:

1. Digital Design
2. Analog/Mixed Signal
3. VLSI Testing
4. Devices and Technology – I
5. VLSI Architectures
6. Emerging Technologies and Memory
7. Devices and Technology – II
8. System Design
9. Low Power Design and Test
10. RF Circuits
11. Architecture and CAD
12. Design Verification

This year we received 246 papers from around the world. After a rigorous review process, the Program Committee selected 48 regular papers and 27 short papers for the proceedings (the acceptance rate was 30%). In all, 150 expert reviewers were involved in rating the papers and on an average each paper received at least three independent reviews. The program of the symposium spanned over four days; the main conference program was preceded by a day of tutorial presentations that had six tutorials delivered by eminent researchers and practitioners in the field. The symposium hosted the following tutorials:

1. Gauri Sankar Malla, “Achieving the Best STA Accuracy for Advanced Nodes.”
2. N. R. Mohapatra and Mr. Pardeep Kumar, “Computational Lithography for Advanced CMOS Nodes.”
3. M. Hasan, “Circuit and System Design Issues for IoT Sensor Node.”
4. K. Bhattacharya, “Design of Modern mm-Wave Transmitters and Power Amplifiers in Silicon and FD SoI CMOS.”

5. Nishit Gupta and Deepak Jharodia, “Transaction Level Modelling with System C for System Level Design.”
6. H. S. Jatana and Ashutosh Yadav, “Advanced Analog Design.”

Several invited talks and keynote speeches were delivered by experts from India and abroad enlightening the participants on various aspects of emerging issues in VLSI research. These talks were delivered by Prof. P. Chakrabarti (IIT-BHU), Dr. Devesh Dwivedi (Global Foundaries, Bangalore), Prof. Maryam Shojaei (IIT-Bombay), Dr. Sudarshan Kumar (HSMC), Mr. Subhasish Mukherjee (Cadence), Mr. Sanjay Gupta (Vice President and India Country Manager, NXP), and Prof. Masahiro Fujita (Tokyo University). VDAT 2017 was a focused research event encompassing themes related to various disciplines of VLSI.

We sincerely thank all the officials and sponsors for their support in recognizing the value of this conference. We would like to express our thanks to the keynote speakers and the tutorial speakers for kindly agreeing to deliver their lectures. Thanks to the authors and reviewers of all the papers for their quality research work. We heartily thank every member of the Conference Committee for their unyielding support in making this event a success.

November 2017

Brajesh Kumar Kaushik
Sudeb Dasgupta
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VDAT 2017 was organized by the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, India.

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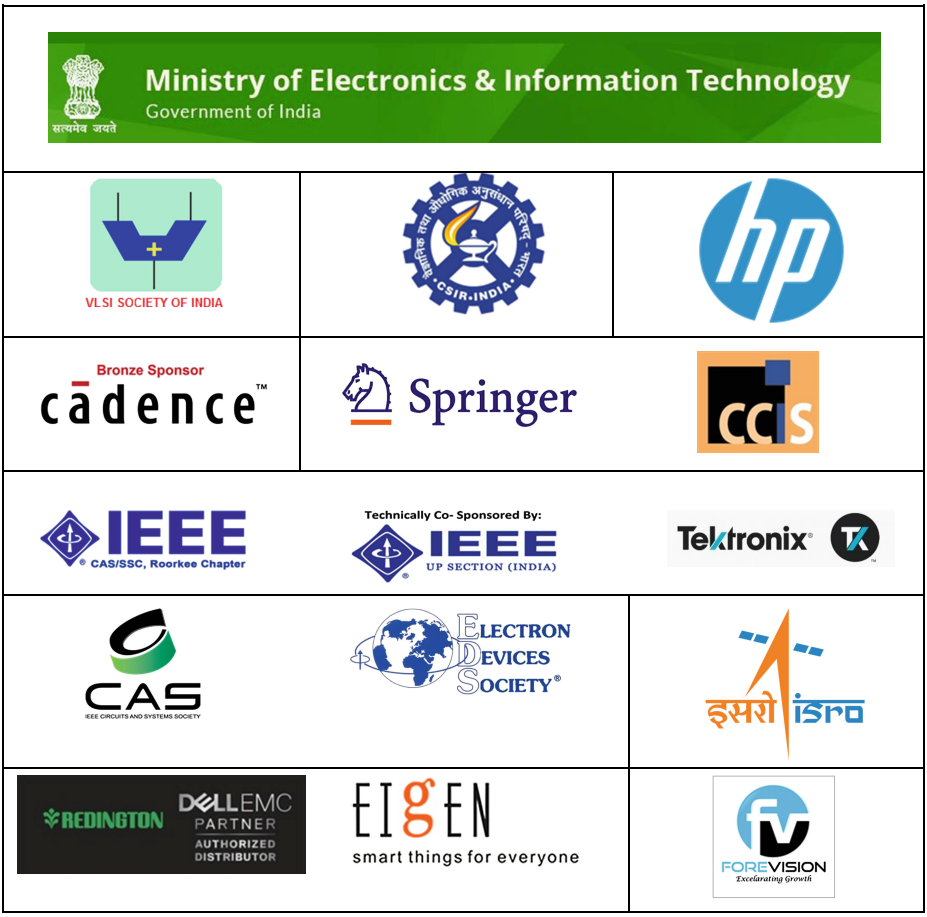

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