Model and Design of Improved Current Mode Logic Gates

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Differential and Single-ended

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Preface

Technological evolution has facilitated the coexistence of digital and analog circuits on a single chip. A single-chip realization has a profound impact on performance, cost, and size. Such chip eases signal acquisition which falls primarily in analog domain and signal processing that is predominately done in the digital domain. The digital circuit design revolves around CMOS due to negligible static power, but it consumes dynamic power which becomes severe at high frequencies and also results in large current spikes during switching event (switching noise). As a consequence, the resolution of analog circuits may decrease; therefore, this issue needs special attention. Alternate logic styles are explored to reduce switching noise which work on keeping power supply current nearly constant during the switching event and/or working with smaller voltage swings. Current mode logic (CML) style is one among these which addresses both the issues and is the main focus of the book.

The book presents the background and a brief review of available literature on CML gates in Chap. 1. The remaining chapters of the book describe newer topologies obtained by modifying the basic parts of CML, namely pull-down network, current source, and load. Chapter 2 is devoted to detailed analysis and design procedure of differential CML and single-ended (PFSCL) gates. The realization of the basic logic gates in differential CML and the single-ended (PFSCL) style is also included. Chapter 3 details the inclusion of triple-tail cell concept in pull-down network of the differential CML gate. This modification leads to lower power supply requirement. It, however, increases the implementation area. The multiple threshold transistor-based triple-tail cell is described next that reduces the overall area requirement. Mathematical formulations for the design-oriented model are elucidated with an intention to develop an understanding of the impact of design and process parameters. The performance of the proposed topologies is illustrated for low-power, high-speed, and power-efficient design cases.

Chapter 4 presents improved dynamic CML (D-CML) gates and self-timed buffer for design of multi-stage applications. Chapter 5 deals with the speed improvement in the CML gates by modifying their load. The load uses the capacitive coupling phenomenon. A complete mathematical model for static parameters and the delay is developed for differential CML and PFSCL gates.

A systematic design procedure to size the bias current and the transistor's aspect ratio to meet design goals is also presented.

Efficient realization of a logic function in PFSCL style is the aim of Chap. 6. A method to reduce the gate count in comparison with the conventional NOR-based logic function realization is described. A new fundamental cell developed by applying triple-tail cell concept in PFSCL style is presented and analyzed. The use of fundamental cell in realizing various logic functions is discussed, and the overall improvement in terms of gate count, propagation delay, and power is compared with the conventional ones.

Tri-state circuits are the essential elements in bus-organized and programmable logic devices and are explored in Chap. 7. Tri-state circuits in CML style are worked upon in this chapter.

This book details the improved designs of CML gates that are suited to mixed-signal environments. An in-depth analysis and step-by-step design procedure will help the researcher to design a gate for given constraints.

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Contents

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