Closing the Gap Between ASIC & Custom

Tools and Techniques for High-Performance ASIC Design The cover was designed by Steven Chan. It shows the Soft-Output Viterbi Algorithm (SOVA) chip morphed with a custom 64-bit datapath. The SOVA chip picture is courtesy of Stephanie Ausberger, Rhett Davis, Borivoje Nikolic, Tina Smilkstein, and Engling Yeo. The SOVA chip was fabricated with STMicroelectronics. The 64-bit datapath is courtesy of Andrew Chang and William Dally. GSRC and MARCO logos were added.

Closing the Gap Between ASIC & Custom

Tools an Techniques for High-Performance ASIC Design



University of California Berkeley

KLUWER ACADEMIC PUBLISHERS NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW eBook ISBN: 0-306-47823-4 Print ISBN: 1-4020-7113-2

©2004 Kluwer Academic Publishers New York, Boston, Dordrecht, London, Moscow

Print ©2002 Kluwer Academic Publishers Dordrecht

All rights reserved

No part of this eBook may be reproduced or transmitted in any form or by any means, electronic, mechanical, recording, or otherwise, without written consent from the Publisher

Created in the United States of America

Visit Kluwer Online at: and Kluwer's eBookstore at: http://kluweronline.com http://ebooks.kluweronline.com

Contents

Pre	Preface xi List of trademarks xv		
Lis			
1.	Int	roduction and Overview of the Book	1
	Da	vid Chinnery, Kurt Keutzer – UC Berkeley	
	1.	WHY ARE CUSTOM CIRCUITS SO MUCH FASTER?	. 1
	2.	WHO SHOULD CARE?	. 1
	3.	DEFINITIONS: ASIC, CUSTOM, ETC.	.3
	4.	THE 35,000 FOOT VIEW: WHY IS CUSTOM FASTER?	.4
	5.	MICROARCHITECTURE	. 9
	6.	TIMING OVERHEAD: CLOCK TREE DESIGN AND	
		REGISTERS	12
	7.	LOGIC STYLE	15
	8.	LOGIC DESIGN	17
	9.	CELL DESIGN AND WIRE SIZING	18
	10.	LAYOUT: FLOORPLANNING AND PLACEMENT TO	
		MANAGE WIRES	20
	11.	PROCESS VARIATION AND IMPROVEMENT	22
	12.	SUMMARY AND CONCLUSIONS	26
	13.	WHAT'S NOT IN THE BOOK	28
	14.	ORGANIZATION OF THE REST OF THE BOOK	28

CONTRIBUTING FACTORS

2.	Im	proving Performance through Microarchitecture	33
	Da	wid Chinnery, Kurt Keutzer – UC Berkeley	
	1.	EXAMPLES OF MICROARCHITECTURAL	
		TECHNIQUES TO INCREASE SPEED	34
	2.	MEMORY ACCESS TIME AND THE CLOCK PERIOD	44
	3.	SPEEDUP FROM PIPELINING	45
3.	Re	ducing the Timing Overhead	57
	Da	wid Chinnery, Kurt Keutzer – UC Berkeley	
	1.	CHARACTERISTICS OF SYNCHRONOUS	
		SEQUENTIAL LOGIC	58

	2.	EXAMPLE WHERE LATCHES ARE FASTER	77
	3.	OPTIMAL LATCH POSITIONS WITH TWO CLOCK	
		PHASES	81
	4.	EXAMPLE WHERE LATCHES ARE SLOWER	83
	5.	PIPELINE DELAY WITH LATCHES VS. PIPELINE	
		DELAY WITH FLIP-FLOPS	87
	6.	CUSTOM VERSUS ASIC TIMING OVERHEAD	90
4.	Hi	gh-Speed Logic, Circuits, Libraries and Layout	101
	An	drew Chang, William J. Dally – Stanford University	
	Da	wid Chinnery, Kurt Keutzer, Radu Zlatanovici – UC Berkeley	
	1.	INTRODUCTION	101
	2.	TECHNOLOGY INDEPENDENT METRICS	102
	3.	PERFORMANCE PENALTIES IN ASIC DESIGNS	
		FROM LOGIC STYLE, LOGIC DESIGN, CELL DESIGN,	
		AND LAYOUT	108
	4.	COMPARISON OF ASIC AND CUSTOM CELL AREAS	129
	5.	ENERGY TRADEOFFS BETWEEN ASIC CELLS AND	
		CUSTOM CELLS	134
	6.	FUTURE TRENDS	138
	7.	SUMMARY	139
5.	Fii	nding Peak Performance in a Process	145
	Da	wid Chinnery, Kurt Keutzer – UC Berkeley	
	1.	PROCESS AND OPERATING CONDITIONS	146
	2.	CHIP SPEED VARIATION DUE TO STATISTICAL	
		PROCESS VARIATION	155
	3.	CONTINUOUS PROCESS IMPROVEMENT	157
	4.	SPEED DIFFERENCES DUE TO ALTERNATIVE	
		PROCESS IMPLEMENTATIONS	159
	5.	PROCESS TECHNOLOGY FOR ASICS	161
	6.	POTENTIAL IMPROVEMENTS FOR ASICS	164

DESIGN TECHNIQUES

6.	Ph	ysical Prototyping Plans for High Performance	169
	Mi	chel Courtoy, Pinhong Chen, Xiaoping Tang, Chin-Chi Teng,	
	Yu	<i>ii Kukimoto</i> – Silicon Perspective, a Cadence Company	
	1.	INTRODUCTION	169
	2.	FLOORPLANNING	170
	3.	PHYSICAL PROTOTYPING	172

vi

	4.	TECHNIQUES IN PHYSICAL PROTOTYPING	180
	5.	CONCLUSIONS	185
7.	Au	tomatic Replacement of Flip-Flops by Latches in ASICs	187
	Da	wid Chinnery, Kurt Keutzer – UC Berkeley	
	Jag	gesh Sanghavi, Earl Killian, Kaushik Sheth – Tensilica	
	1.	INTRODUCTION	187
	2.	THEORY	191
	3.	ALGORITHM	199
	4.	RESULTS	203
	5.	CONCLUSION	207
8.	Us	eful-Skew Clock Synthesis Boosts ASIC Performance	209
	Wc	<i>iyne Dai</i> – UC Santa Cruz	
	Da	wid Staepelaere – Celestry Design Technologies	
	1.	INTRODUCTION	209
	2.	IS CLOCK SKEW REALLY GLOBAL?	210
	3.	PERMISSIBLE RANGE SKEW CONSTRAINTS	211
	4.	WHY CLOCK SKEW MAY BE USEFUL	213
	5.	USEFUL SKEW DESIGN METHODOLOGY	216
	6.	USEFUL SKEW CASE STUDY	218
	7.	CLOCK AND LOGIC CO-DESIGN	220
	8.	SIMULTANEOUS CLOCK SKEW OPTIMIZATION AND	
		GATE SIZING	220
	9.	CONCLUSION	221
9.	Fa	ster and Lower Power Cell-Based Designs with	
	Tr	ansistor-Level Cell Sizing	225
	Mi	chel Côté, Philippe Hurat – Cadabra, a Numerical	
	Te	chnologies Company	
	1.	INTRODUCTION	225
	2.	OPTIMIZED CELLS FOR BETTER POWER AND	
		PERFORMANCE	226
	3.	PPO FLOW	228
	4.	PPO EXAMPLES	235
	5.	FLOW CHALLENGES AND ADOPTION	238
	6.	CONCLUSIONS	239
10	De	sign Optimization with Automated Flex-Cell Creation	241
	De	bashis Bhattacharya, Vamsi Boppana – Zenasis Technologies	
	1.	FLEX-CELL BASED OPTIMIZATION – OVERVIEW	244
	2.	MINIMIZING THE NUMBER OF NEW FLEX-CELLS	
		CREATED	249

	3.	CELL LAYOUT SYNTHESIS IN FLEX-CELL BASED	254
	4	GREATER PERFORMANCE THROUGH BETTER	237
	4.		255
	5	DUVSICAL DESIGN AND ELEV CELL BASED	
	5.	ODTIMIZATION	250
	6	CASE STUDIES WITH DESULTS	261
	0. 7.	CONCLUSIONS	
11	Ex	nloiting Structure and Managing Wires to Increase	
11.	De	nsity and Performance	269
	An	drew Chang William I Dally – Stanford University	-07
	1	INHERENT DESIGN STRUCTURE	269
	2	SUCCESSIVE CUSTOM TECHNIQUES FOR	
	2.	EXPLOITING STRUCTURE	
	3	FUTURE DIRECTIONS	285
	4.	SUMMARY	285
12	Sei	mi-Custom Methods in a High-Performance	
	Mi	croprocessor Design	289
	Gr	egory A. Northrop – IBM	
	1.	INTRODUCTION	
	2.	CUSTOM PROCESSOR DESIGN	
	3.	SEMI-CUSTOM DEISGN FLOW	
	4.	DESIGN EXAMPLE – 24 BIT ADDER	
	5.	OVERALL IMPACT ON CHIP DESIGN	
13.	. Co	ntrolling Uncertainty in High Frequency Designs	305
	Ste	phen E. Rich, Matthew J. Parker, Jim Schwartz – Intel	
	1.	INTRODUCTION	
	2.	FREQUENCY TERMINOLOGY	
	3.	UNCERTAINTY DEFINED	
	4.	WHY UNCERTAINTY REDUCES THE MAXIMUM	
		POSSIBLE FREQUENCY	
	5.	PRACTICAL EXAMPLE OF TOOL UNCERTAINTY	
	6.	FOCUSED METHODOLOGY DEVELOPMENT	
	7.	METHODS FOR REMOVING PATHS FROM THE	
		UNCERTAINTY WINDOW	
	8.	THE UNCERTAINTY LIFECYCLE	
	9.	CONCLUSION	

viii

14.	Inc	reasing Circuit Performance through Statistical Design	
	Tec	hniques	323
	Mic	hael Orshansky – UC Berkeley	
	1.	PROCESS VARIABILITY AND ITS IMPACT ON	
		TIMING	324
	2.	INCREASING PERFORMANCE THROUGH	
		PROBABILISTIC TIMING MODELING	329
	3.	INCREASING PERFORMANCE THROUGH DESIGN	
		FOR MANUFACTURABILITY TECHNIQUES	334
	4.	ACCOUNTING FOR IMPACT OF GATE LENGTH	
		VARIATION ON CIRCUIT PERFORMANCE: A CASE	
		STUDY	
	5.	CONCLUSION	342

DESIGN EXAMPLES

15. Ac	chieving 550MHz in a Standard Cell ASIC Methodology	345
Da	wid Chinnery, Borivoje Nikolić, Kurt Keutzer – UC Berkeley	
1.	INTRODUCTION	345
2.	A DESIGN BRIDGING THE SPEED GAP BETWEEN	
	ASIC AND CUSTOM	
3.	MICROARCHITECTURE: PIPELINING AND LOGIC	
	DESIGN	348
4.	REGISTER DESIGN	353
5.	CLOCK TREE INSERTION AND CLOCK	
	DISTRIBUTION	356
6.	CUSTOM LOGIC VERSUS SYNTHESIS	357
7.	REDUCING UNCERTAINTY	358
8.	SUMMARY AND CONCLUSIONS	358
16. Tł	ne iCORE TM 520MHz Synthesizable CPU Core	361
Ni	ck Richardson, Lun Bin Huang, Razak Hossain, Julian Lewis,	
Ta	ommy Zounes, Naresh Soni – STMicroelectronics	
1.	INTRODUCTION	361
2.	OPTIMIZING THE MICROARCHITECTURE	363
3.	OPTIMIZING THE IMPLEMENTATION	375
4.	PHYSICAL DESIGN STRATEGY	378
5.	RESULTS	379
6.	CONCLUSIONS	380

17.	7. Creating Synthesizable ARM Processors with Near Custom			
	Performance			
	Da	vid Flynn – ARM		
	Mie	chael Keating – Synopsys		
	1.	INTRODUCTION	383	
	2.	THE ARM7TDMI EMBEDDED PROCESSOR	384	
	3.	THE NEED FOR A SYNTHESIZABLE DESIGN	391	
	4.	THE ARM7S PROJECT	392	
	5.	THE ARM9S PROJECT	400	
	6.	THE ARM9S DERIVATIVE PROCESSOR CORES	403	
	7.	NEXT GENERATION CORE DEVELOPMENTS	406	

Index

Х

411

Preface

by Kurt Keutzer

Those looking for a quick overview of the book should fast-forward to the Introduction in Chapter 1. What follows is a personal account of the creation of this book.

The challenge from Earl Killian, formerly an architect of the MIPS processors and at that time Chief Architect at Tensilica, was to explain the significant performance gap between ASICs and custom circuits designed in the same process generation. The relevance of the challenge was amplified shortly thereafter by Andy Bechtolsheim, founder of Sun Microsystems and ubiquitous investor in the EDA industry. At a dinner talk at the 1999 *International Symposium on Physical Design*, Andy stated that the greatest near-term opportunity in CAD was to develop tools to bring the performance of ASIC circuits closer to that of custom designs. There seemed to be some synchronicity that two individuals so different in concern and character would be pre-occupied with the same problem. Intrigued by Earl and Andy's comments, the game was afoot.

Earl Killian and other veterans of microprocessor design were helpful with clues as to the sources of the performance discrepancy: layout, circuit design, clocking methodology, and dynamic logic. I soon realized that I needed help in tracking down clues. Only at a wonderful institution like the University of California at Berkeley could I so easily commandeer an ablebodied graduate student like David Chinnery with a knowledge of architecture, circuits, computer-aided design and algorithms. David has grown from graduate research assistant to true collaborator over the course of this work, and today he truly "owns" the book.

The search for the performance gap between ASICs and custom circuits soon led us far beyond our provincial concerns of logic and circuit design. We found ourselves touring lands as distant as processor microarchitecture and as exotic as semiconductor process variation. We got a chance to share our initial discoveries at an invited session at the *Design Automation Conference* (DAC) in 2000. Whatever concerns we had that the topic was

too esoteric to be of broad interest were quickly allayed. The DAC session, chaired by Bryan Ackland, was parked at the very end of the conference at a time when most conference participants are already on the plane back home. Nevertheless, the room was packed more tightly than any conference room in my memory. Attendees sat in the aisles and some were bold enough to sit cross-legged on the speakers' dais during the talks. Later one of the video operators complained that she was unable to get past the crowd wedged at the door in order to staff her video monitor. The public interest in the topic was very encouraging.

Every weary traveler in an unfamiliar land knows the joy of meeting a compatriot. Andrew Chang and William Dally were already well on their own way to forming conclusions about the relationship between ASIC and custom performance when they presented their views in the DAC 2000 session mentioned above. While the angle of our work was to show that ASIC techniques could be augmented to achieve nearly custom performance, the focus of their work was to show the superiority of custom design techniques over those of ASICs. Our discussions on these disparate views have now continued for over two years and Chapter 4 shows the resulting synthesis. Detailed arguments between Andrew Chang and David Chinnery examined our assumptions and questioned our conclusions, enabled us to arrive at a thorough and careful analysis of ASIC and custom performance.

In the following Fall a new faculty member at Berkeley, **Borivoje** Nikolić, found his way to my office. Reading our paper at DAC 2000 he noted the relationship between the design techniques he had used at Texas Instruments and those identified in the paper. With Borivoje's knowledge of circuit design in general, and a read channel design (described in Chapter 15) in particular, our work got a much stronger foundation. As a result we were able to better identify and illustrate the key design techniques necessary to improve performance in an ASIC methodology. The initial results of this collaboration appeared at DAC 2001 and we were again encouraged by the large audience for the work

In our investigative travels we encountered a few other designers whose work we are pleased to include in this book. Michael Keating's work on synthesizable versions of the ARM is an invaluable example. It is one of the few cases where a synthesized ASIC design could be compared side-by-side with a custom version. Discussions with Michael had a significant influence on our thinking.

If you can imagine the thrill of a detective stumbling onto an unexpected clue then you'll understand our enthusiasm when we spotted STMicroelectronics' work on the design of the 520MHz iCORETM processor. As soon as we saw it we were anxious to include it in the book.

Along our investigations we encountered many others attempting to build tools for improving the performance of ASIC design. Their work speaks for itself in Chapters 6 through 14.

In addition to our co-authors, we'd like to acknowledge at least a few of those individuals with whom we've had relevant discussions. We've had animated discussions on the sources of performance in integrated circuit design with: Bryan Ackland, Matthew Adiletta, Shekhar Borkar, Patrick Bosshart, Dan Dobberpuhl, Abbas El Gamal, Douglas Galbraith, Mehdi Hatamian, Bill Huffman, Mark Horowitz, Arangzeb Khan, Ram Krishnamurthy, Jan Rabaey, Mark Ross, Paul Rodman, Takayasu Sakurai, Mark Vancura, Kees Vissers, Tony Waitz, Scott Weber, and Neil Weste. In retrospect, an unconscious seed of this work may have been planted at an ISSCC panel in 1992. In a panel chaired by Mark Horowitz in which Bosshart, Dobberpuhl, Hatamian, and I debated the respective merits of synthesis and custom methodologies.

Over the years we've also had innumerable discussions on the role of tools and technologies for high performance design. I'd like to acknowledge just a few of those individuals: Robert Brayton, Raul Camposano, Srinivas Devadas, Antun Domic, Jack Fishburn, Masahiro Fujita, Dwight Hill, Joe Hutt, Andrew Kahng, Desmond Kirpatrick, Martin Lefebvre, Don MacMillan, Sharad Malik, David Marple, Richard Rudell, Alex Saldanha, Alberto Sangiovanni-Vincentelli, Ken Scott, Carl Sechen, Farhana Sheikh, Greg Spirakis, Dennis Sylvester, Chandu Vishewariah, and Albert Wang.

One of the points of the book is to demonstrate the role that semiconductor processing variation plays in determining circuit performance. Thanks to a number of people for enlightening us on this topic, including: Jeff Bokor, Christopher Hamlin, Chenming Hu, T-J King, and Costas Spanos.

Helpful editorial work came from Matthew Guthaus, Chidamber Kulkarni, Andrew Mihal, Michael Orshansky, Farhana Sheikh, and Scott Weber. The cover was beautifully rendered by Steve Chan.

The home of this work is the Gigascale Silicon Research Center (GSRC) funded by the Microelectronics Advanced Research Consortium (MARCO). This book is in some regards a clandestine effort to realize the vision of Richard Newton, GSRC's first Director. Richard's vision was for *Custom Performance with ASIC productivity*. At some point we wisely realized it would be easier to try to realize this dream than to convince Richard that it was impossible.

In closing we'd like to especially to thank Earl Killian. Not only did he pose the question that first inspired our investigations but he has been the most insightful critic of our work throughout. Earl has always been willing to take the time to respond in depth on any technical question or to read in detail any idea. Earl's commitment to technical clarity and integrity has been a continuous inspiration. We must confess that up to our most recent email exchange our work has still not fully answered Earl's question to his satisfaction. Nevertheless, our relentless attempts to do so have vastly improved the quality of this book.

For emotional support we'd also like to thank the people close to us. David gratefully thanks his grandparents, Ronald and Alex Ireland, for their wonderful support and encouragement throughout the years. Kurt thanks Barbara Creech for her understanding and support during the writing of this book.

List of Trademarks

Throughout this book we make reference to various chips and software. The following trademarks are referred to in this book:

Advanced Micro Devices, Inc.: Athlon, K6

Cadence Design Systems, Inc.: CTGen, Pearl, Silicon Ensemble, Verilog

Compaq, Inc.: Alpha

International Business Machines, Inc.: PowerPC

Intel Corporation, Inc.: Pentium II, Pentium 4

Mentor Graphics, Inc.: Calibre

STMicroelectronics, Inc.: iCORE

Synopsys, Inc.: Design Compiler, Design Ware, Module Compiler, Physical Compiler, Power Compiler, PrimeTime, PrimePower,

Tensilica, Inc.: Xtensa