Closing the Gap Between ASIC & Custom

Tools and Techniques for High-Performance ASIC Design

The cover was designed by Steven Chan. It shows the Soft-Output Viterbi Algorithm (SOVA) chip morphed with a custom 64-bit datapath. The SOVA chip picture is courtesy of Stephanie Ausberger, Rhett Davis, Borivoje Nikolic, Tina Smilkstein, and Engling Yeo. The SOVA chip was fabricated with STMicroelectronics. The 64-bit datapath is courtesy of Andrew Chang and William Dally. GSRC and MARCO logos were added.

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Contents

DESIGN TECHNIQUES

DESIGN EXAMPLES

Preface

by Kurt Keutzer

Those looking for a quick overview of the book should fast-forward to the Introduction in Chapter 1. What follows is a personal account of the creation of this book.

The challenge from Earl Killian, formerly an architect of the MIPS processors and at that time Chief Architect at Tensilica, was to explain the significant performance gap between ASICs and custom circuits designed in the same process generation. The relevance of the challenge was amplified shortly thereafter by Andy Bechtolsheim, founder of Sun Microsystems and ubiquitous investor in the EDA industry. At a dinner talk at the 1999 *International Symposium on Physical Design,* Andy stated that the greatest near-term opportunity in CAD was to develop tools to bring the performance of ASIC circuits closer to that of custom designs. There seemed to be some synchronicity that two individuals so different in concern and character would be pre-occupied with the same problem. Intrigued by Earl and Andy's comments, the game was afoot.

Earl Killian and other veterans of microprocessor design were helpful with clues as to the sources of the performance discrepancy: layout, circuit design, clocking methodology, and dynamic logic. I soon realized that I needed help in tracking down clues. Only at a wonderful institution like the University of California at Berkeley could I so easily commandeer an able-bodied graduate student like David Chinnery with a knowledge of architecture, circuits, computer-aided design and algorithms. David has grown from graduate research assistant to true collaborator over the course of this work, and today he truly "owns" the book.

The search for the performance gap between ASICs and custom circuits soon led us far beyond our provincial concerns of logic and circuit design. We found ourselves touring lands as distant as processor microarchitecture and as exotic as semiconductor process variation. We got a chance to share our initial discoveries at an invited session at the *Design Automation Conference* (DAC) in 2000. Whatever concerns we had that the topic was

too esoteric to be of broad interest were quickly allayed. The DAC session, chaired by Bryan Ackland, was parked at the very end of the conference at a time when most conference participants are already on the plane back home. Nevertheless, the room was packed more tightly than any conference room in my memory. Attendees sat in the aisles and some were bold enough to sit cross-legged on the speakers' dais during the talks. Later one of the video operators complained that she was unable to get past the crowd wedged at the door in order to staff her video monitor. The public interest in the topic was very encouraging.

Every weary traveler in an unfamiliar land knows the joy of meeting a compatriot. Andrew Chang and William Dally were already well on their own way to forming conclusions about the relationship between ASIC and custom performance when they presented their views in the DAC 2000 session mentioned above. While the angle of our work was to show that ASIC techniques could be augmented to achieve nearly custom performance, the focus of their work was to show the superiority of custom design techniques over those of ASICs. Our discussions on these disparate views have now continued for over two years and Chapter 4 shows the resulting synthesis. Detailed arguments between Andrew Chang and David Chinnery examined our assumptions and questioned our conclusions, enabled us to arrive at a thorough and careful analysis of ASIC and custom performance.

In the following Fall a new faculty member at Berkeley, Borivoje Nikolić, found his way to my office. Reading our paper at DAC 2000 he noted the relationship between the design techniques he had used at Texas Instruments and those identified in the paper. With Borivoje's knowledge of circuit design in general, and a read channel design (described in Chapter 15) in particular, our work got a much stronger foundation. As a result we were able to better identify and illustrate the key design techniques necessary to improve performance in an ASIC methodology. The initial results of this collaboration appeared at DAC 2001 and we were again encouraged by the large audience for the work

In our investigative travels we encountered a few other designers whose work we are pleased to include in this book. Michael Keating's work on synthesizable versions of the ARM is an invaluable example. It is one of the few cases where a synthesized ASIC design could be compared side-by-side with a custom version. Discussions with Michael had a significant influence on our thinking.

If you can imagine the thrill of a detective stumbling onto an unexpected clue then you'll understand our enthusiasm when we spotted STMicroelectronics' work on the design of the 520MHz iCORE™ processor. As soon as we saw it we were anxious to include it in the book.

Along our investigations we encountered many others attempting to build tools for improving the performance of ASIC design. Their work speaks for itself in Chapters 6 through 14.

In addition to our co-authors, we'd like to acknowledge at least a few of those individuals with whom we've had relevant discussions. We've had animated discussions on the sources of performance in integrated circuit design with: Bryan Ackland, Matthew Adiletta, Shekhar Borkar, Patrick Bosshart, Dan Dobberpuhl, Abbas El Gamal, Douglas Galbraith, Mehdi Hatamian, Bill Huffman, Mark Horowitz, Arangzeb Khan, Ram Krishnamurthy, Jan Rabaey, Mark Ross, Paul Rodman, Takayasu Sakurai, Mark Vancura, Kees Vissers, Tony Waitz, Scott Weber, and Neil Weste. In retrospect, an unconscious seed of this work may have been planted at an ISSCC panel in 1992. In a panel chaired by Mark Horowitz in which Bosshart, Dobberpuhl, Hatamian, and I debated the respective merits of synthesis and custom methodologies.

Over the years we've also had innumerable discussions on the role of tools and technologies for high performance design. I'd like to acknowledge just a few of those individuals: Robert Brayton, Raul Camposano, Srinivas Devadas, Antun Domic, Jack Fishburn, Masahiro Fujita, Dwight Hill, Joe Hutt, Andrew Kahng, Desmond Kirpatrick, Martin Lefebvre, Don MacMillan, Sharad Malik, David Marple, Richard Rudell, Alex Saldanha, Alberto Sangiovanni-Vincentelli, Ken Scott, Carl Sechen, Farhana Sheikh, Greg Spirakis, Dennis Sylvester, Chandu Vishewariah, and Albert Wang.

One of the points of the book is to demonstrate the role that semiconductor processing variation plays in determining circuit performance. Thanks to a number of people for enlightening us on this topic, including: Jeff Bokor, Christopher Hamlin, Chenming Hu, T-J King, and Costas Spanos.

Helpful editorial work came from Matthew Guthaus, Chidamber Kulkarni, Andrew Mihal, Michael Orshansky, Farhana Sheikh, and Scott Weber. The cover was beautifully rendered by Steve Chan.

The home of this work is the Gigascale Silicon Research Center (GSRC) funded by the Microelectronics Advanced Research Consortium (MARCO). This book is in some regards a clandestine effort to realize the vision of Richard Newton, GSRC's first Director. Richard's vision was for *Custom Performance with ASIC productivity.* At some point we wisely realized it would be easier to try to realize this dream than to convince Richard that it was impossible.

In closing we'd like to especially to thank Earl Killian. Not only did he pose the question that first inspired our investigations but he has been the most insightful critic of our work throughout. Earl has always been willing to take the time to respond in depth on any technical question or to read in

detail any idea. Earl's commitment to technical clarity and integrity has been a continuous inspiration. We must confess that up to our most recent email exchange our work has still not fully answered Earl's question to his satisfaction. Nevertheless, our relentless attempts to do so have vastly improved the quality of this book.

For emotional support we'd also like to thank the people close to us. David gratefully thanks his grandparents, Ronald and Alex Ireland, for their wonderful support and encouragement throughout the years. Kurt thanks Barbara Creech for her understanding and support during the writing of this book.

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