STATIC CROSSTALK-NOISE ANALYSIS

For Deep Sub-Micron Digital Designs

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KLUWER ACADEMIC PUBLISHERS
NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW

eBook ISBN: 1-4020-8092-1
Print ISBN: 1-4020-8091-3

Created in the United States of America

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Preface

As the feature sizes decrease in deep sub-micron circuit designs, coupling capacitance dominates total capacitance, and crosstalk noise problems become significant and responsible for major timing variations and signal integrity issues.

Timing analysis is an important method to verify that a chip can meet performance requirements. Given a circuit network and its component models, timing analysis calculates signal propagation delay to verify whether the results can be delivered on time at the outputs. Unlike dynamic timing analysis, static timing analysis uses a vectorless approach to analyze the network topology without simulation. Traditional static timing analysis ignores cross coupling effects between wires, or approximates the coupling capacitance by a 2X (Miller factor) grounded decoupled capacitance to account for the worst case delay. This approach not only reduces delay calculation accuracy, but can also be shown to underestimate the delay in certain scenarios. We propose an efficient method to estimate this Miller factor so that the delay response of a decoupled circuit model can emulate the original coupling circuit. Under the assumptions of zero initial voltage, equal charge transfer, and $0.5V_{DD}$ as the switching threshold voltage, an upper bound of 3X for maximum delay and a lower bound of -1X for minimum delay is proven.

Crosstalk coupling is also very sensitive to switching windows, in which signal nets can make transitions. It is the signal switching that causes the wire to inject extra current to its neighboring wires and affect their signal delay or arrival times. Thus, it is important to capture the switching windows for evaluating the crosstalk effect. However, the switching windows again depends on the signal arrival times. The way to resolve this mutual dependency is through iterations. We will build the theoretical foundation to analyze the nature of these iterations considering modeling, accuracy, and mathematical properties and also propose effective ways to converge these iterations. A time slot approach is used to reduce pessimism of crosstalk analysis.

Crosstalk is also subject to functional correlation which is similar to the false path problem (i.e., the neighboring wires might not switch all at the same time in the same direction due to logic correlation). To evaluate a maximum crosstalk noise, we must search and compute the logic condition that produces the maximum peak noise. A conservative approach assumes every net can switch at the same time in the same direction, while the approach we propose can eliminate this false switching combination. A similar idea arises in timing analysis to eliminate false paths. However, the maximum crosstalk problem is even more complicated due to its optimization nature and interaction across a large set of signals.

The goal of this work is to achieve a computationally efficient, accurate, but conservative approach to crosstalk analysis for digital circuits.