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Research paper

A low-cost 10-Gbit/s millimeter-wave wireless link working at E-band

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Abstract: Test results for a 10-Gbps prototype demonstrator working at 71~76 GHz frequency band with a 2-bit/s/Hz spectral efficiency are reported. To overcome the speed limitation of the commercial DA/ADs, a two-channel analog IF multiplexing and demultiplexing topology is adopted as a trade-off between cost and spectrum efficiency. The same approach is also used to achieve up to 20 Gbps with a full 10-GHz bandwidth of the allocated commercial bands (71~76 GHz and 81~86 GHz).

Key words: millimeter-wave radio communication, E-band, wireless link, transmitter, receiver.

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1 Introduction

The use of the E-band (71~76 GHz/81~86 GHz) for commercial purposes has attracted a lot of interests because it is possible to achieve a multi-Gbps data rate in full duplex even with a simple modulation scheme[1,2]. The high working frequency provides an increasing absolute bandwidth and therefore, growing data rates in fixed networks for fiber extension Unlike the 60-GHz band, the atmospheric attenuation at these frequencies is very low, which enables long-distance data links[3].

Currently, many point-to-point commercial wireless links in the millimeter-wave spectrum have been reported. However, they were implemented with either low-order modulation BPSK/QPSK schemes over multi-GHz bandwidths or high-order 2048/4096 QAM (Quadrature Amplitude Modulation) schemes in narrow bandwidths (e.g., 50 MHz). As a result, they lead to poor spectral efficiencies of lower than 1 bit/s/Hz or limited speed up to several Gbit/s. Recently, several E-band systems were reported. The CSIRO group reported a 6-Gbit/s combined data rate over a 250 m outdoor path using 8PSK (eight Phase-Shift Keying) modulation with a 2.4-bit/s/Hz spectral efficiency[4]. Another group in Korea presented an eight-channel point-to-point broadband wireless communication system with 16QAM[5].

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In this paper, we report a 10-Gbps millimeter-wave point-to-point link working at 71~76 GHz frequency band using a spectral-efficient modulation type. With 16QAM, we achieved 2 bit/s/Hz efficiency over the entire 5-GHz bandwidth. The same approach can be used to achieve up to 20 Gbit/s with a full 10-GHz bandwidth of the allocated commercial bands (71~76 GHz and 81~86 GHz).

2 System architecture

A simplified block diagram of the E-band wireless link system architecture is shown in Fig.1. It includes a digital interface, a digital modem, an IF module, wideband mm-wave transmitter and receiver sections, and a high-directivity horn antenna. The transmitter and receiver signals are corresponded using a frequency domain diplexer.

The transmitter consists of two digital modulators, two DACs (Digital-to-Analog Converters), two IF upconverters, and one RF upconverter. Each digital modulator generates 16QAM signals with a symbol rate of 1.25 Gs/s and an oversampling ratio of 3. Two IF upconverters then upconvert the two modulated signals to the IF band (from 2.5 GHz to 7.5 GHz) with a channel spacing of 225 MHz. The RF upconverter upconverts the IF signal and transmits the resultant signal in the E-band spectrum of 71~76 GHz. As for the receiver, the RF downconverter downconverts the RF signal from the E-band spectrum of 71~76 GHz to the IF band (2.5 GHz to 7.5 GHz). Two IF downconverters downconvert each channel signal to the baseband. Then, these signals are sampled by the high-speed A/D converters and decoded by the FPGA into digital channels, and multiplexed into a single digital stream.

3 Analog IF modules

Owing to the speed limitation of A/D (Analog-to-Digital) and D/A (Digital-to-Analog) converters commercial available, the continuous bandwidth of practical efficient digital modems is limited up to 5 GHz. In order to improve the spectrum efficiency, a frequency-

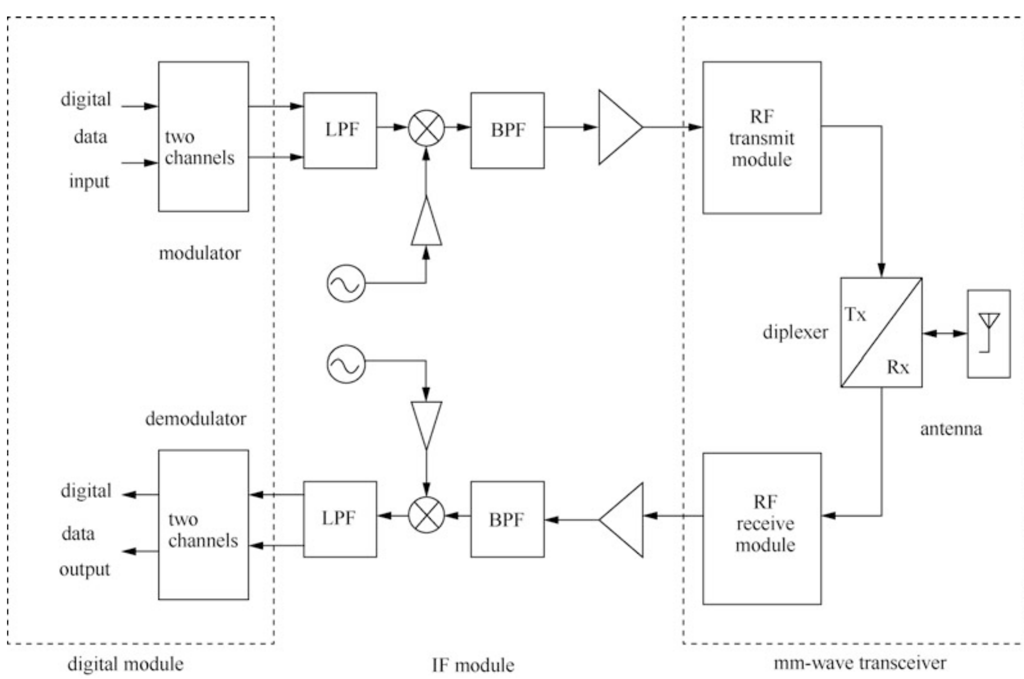

Figure 1 Block diagram of the system

domain multichannel multiplexing topology is adopted. At the transmitter side, it multiplexes N high-speed channels (with a bandwidth of BW_0 each) into a single RF channel with a bandwidth of $BW = N \cdot BW_0$, where BW is the continuous bandwidth of the signal processing.

At the receiver side, the input binary data is demultiplexed into N identical channels with bandwidth BW_0. Theoretically, a narrower bandwidth leads to more channels, more AD/DAs, a more complicated system, and a higher modulation scheme. In this implementation, as a tradeoff between component cost and system performance, two channels and a bandwidth of 2.25 GHz are chosen.

Fig.2 shows a block diagram of the analog IF module.

In the IF transmitter circuit, the output power of the baseband signal ranges from −10 dBm to 0 dBm, and the maximum input rating of the Tx RF upconverter is 0 dBm. Thus, the IF transmitter circuit needs only one amplifier stage. The LO (Local Oscillators) were selected to work at high oscillation frequency because the harmonics were far away from the operating frequency.

In the IF receiver circuit, the power of RF Rx downconverter maximum ratings is −30 dBm.

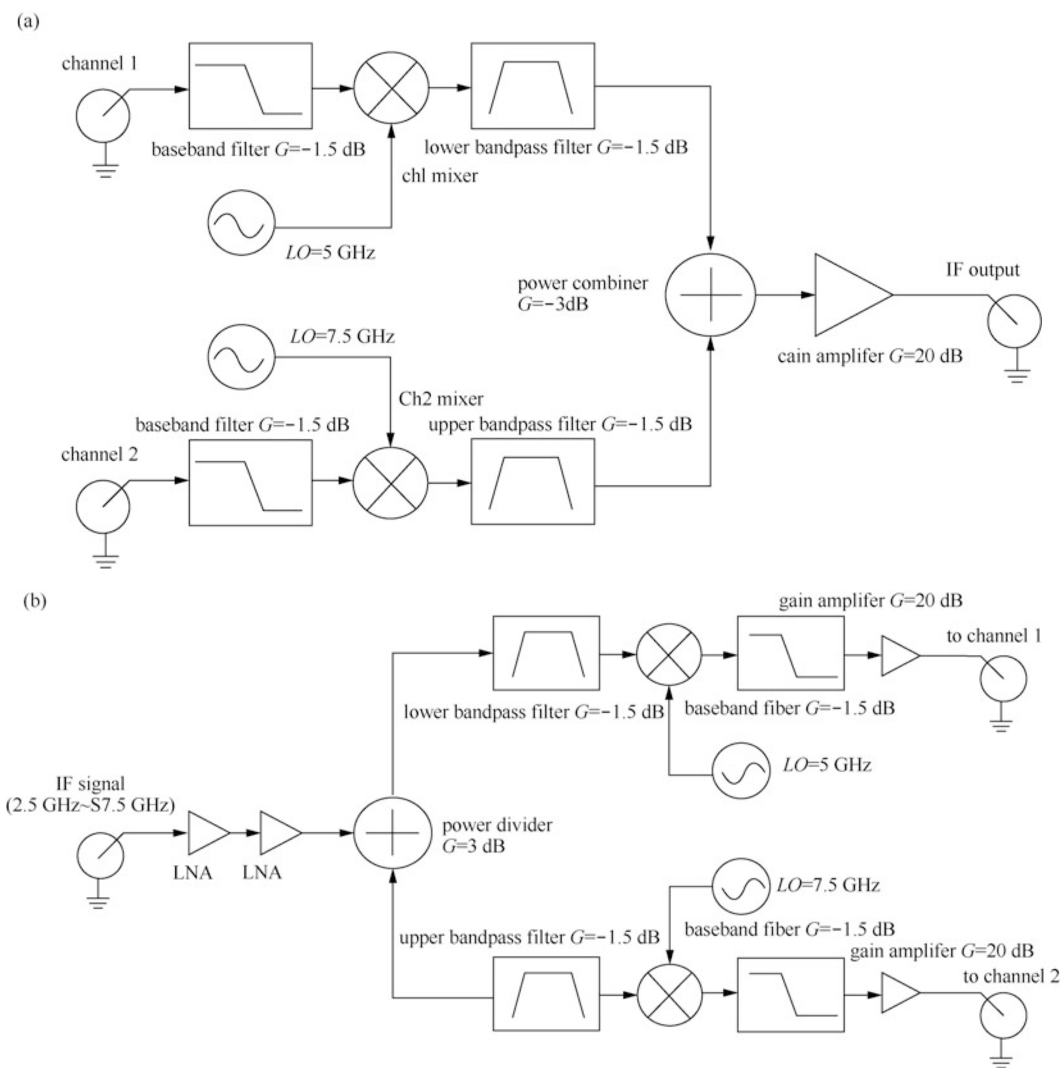

Figure 2 Details of the IF module: (a) IF transmitter module; (b) IF receiver module

Considering the frequency conversion loss and passive device loss (e.g., low-pass filter, band-pass filter, and power divider), at least three amplifier stages are needed in the IF receiver circuit to achieve enough IF output power. As shown in Fig.2(b), the first two amplifier stages are realized as a low-noise amplifier, and the amplifier behind the mixer is realized as a variable-gain amplifier.

The IF circuit was designed and fabricated using FR4 and Rogers4350 B boards. As shown in Fig.3, surface-mount amplifiers, a mixer, capacitors, and inductors were fabricated using an FR4 board, while the microstrip transmission line circuits were fabricated using multilayer RO4350B material with a dielectric constant of 3.65. Benefiting from high reliability and a simple design, the transmission line structure is used to realize the filter and power divider/combiner.

As shown in Fig.2(a) and Fig.2(b), the fraction bandwidth of the power divider/combiner is 100% over the IF bandwidth (i.e., from 2.5 GHz to 7.5 GHz), while the fraction bandwidth of the lower passband filter and upper passband filter are 66.7% and 40%, respectively. The fraction bandwidth for the lower pass-band filter and upper pass-band filter are 66.7% and 40%, respectively. Furthermore, in order to avoid interference between the two channels, the passband filter needs a harmonic suppression of at least 20 dB[6].

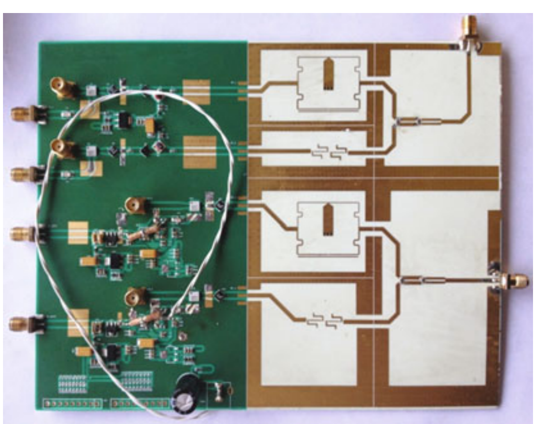

Figure 3 Fabricated IF module

4 Millimeter-wave mmic modules

The circuits are implemented using a GaAs 0.1-μm gate-length PHEMT technology from UMS (United Monolithic Semiconductors). As shown in Fig.4, the proposed E-band transmitter circuit consists of a doubler, a two-stage LO buffer amplifier, and a balanced resistive mixer. At the upconversion part, a balanced resistive mixer is selected owing to the high RF-LO isolation. In addition, high sideband suppression can be achieved by the differential IQ input. Fig.5 gives the micro-photograph of the fabricated transmitter chip. It has a size of $2.5 \times 2.5\ mm^2$.

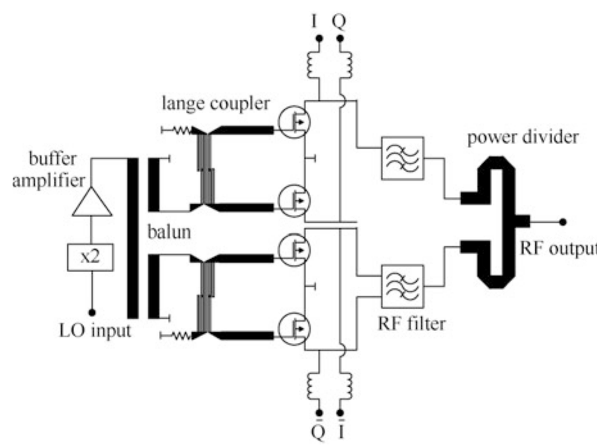

Figure 4 Schematic of IQ modulator

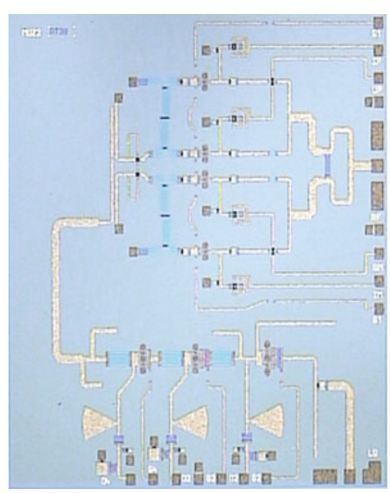

Figure 5 Microphotograph of IQ modulator MMIC

The proposed E-band receiver circuit consists of an image rejection mixer with I/Q output, a three-stage low-noise amplifier, and a frequency doubler, as depicted in Fig.6. At the downconversion part, an image-rejection mixer is adopted to suppress the image frequency. Fig.6 gives the microphotograph of the fabricated receiver chip. It has a size of 2×2.5 mm^2.

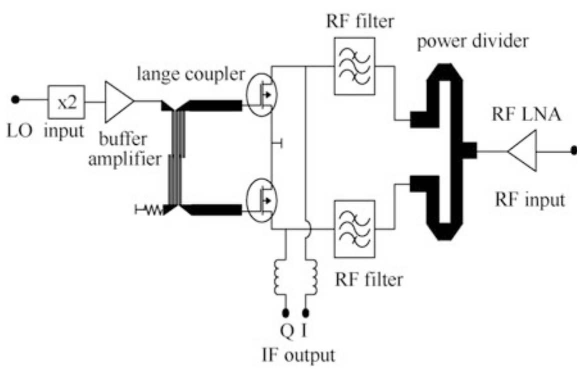

Figure 6 Schematic representation of the receiver

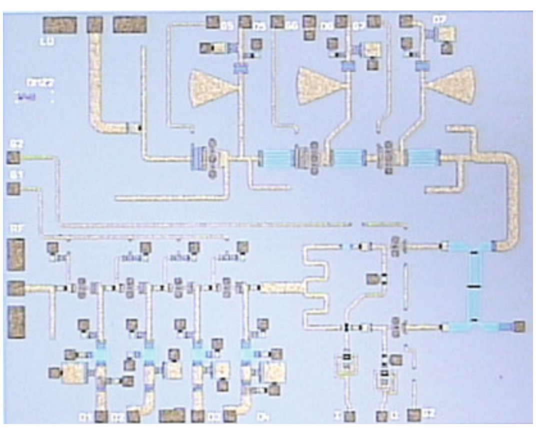

Figure 7 Microphotograph of receiver MMIC

In order to transmit and receive higher-order modulation signals (such as 16QAM) with a low BER (Bit Error Rate), an LO with low phase noise characteristics is required. However, pure signal generation in the mm-wave bands realized directly by a fundamental frequency oscillator is quite difficult. As an alternative solution, using lower-frequency oscillators related with frequency multipliers to obtain the desired frequencies signal generation is flexible. The added phase noise by the frequency doubler itself is theoretically 6 dB, and the clock generation scheme is used in this design.

To facilitate the proceeding measurements, the T/R modules were packaged using a COB (Chip-on-Board) method to provide a WR-12 waveguide port for further antenna connection.

5 Experimental results

The entire test setup is shown in Fig.8. Traffic is generated from two 10-Gbit/s Ethernet cards installed on two desktop PCs. The Ethernet cards are connected to the baseband cards via optical fiber. The baseband boards process digital IF signals and output/accept analog signals to/from the IF system. Baseband cards are connected to the IF boards via cables. The IF board is connected to the RF system, while a pair of small cone antennas are connected for RF loopback.

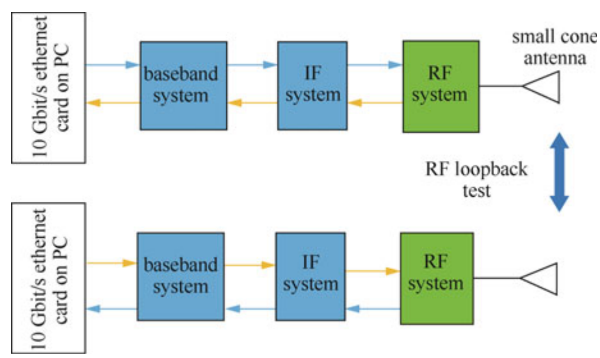

Figure 8 Block diagram of test setup

Signals are generated and received on the two PCs directly. Hence, this test is for bidirectional transmissions. The data rate is measured for TCP traffic. The TCP throughput is measured using the Iperf command. Each Ethernet packet contains 1 460 B of TCP data but has a total length of 1 538 B owing to TCP, IPv4, MAC, and PHY headers and trailers. The maximum expected TCP throughput for 10-Gbit/s Ethernet is 10×1 460/1 538 = 9.49 Gbit/s.

A complete system test (loopback through antennas) is conducted in an office environment.

Each Ethernet card is installed on a PC and is connected to the optical interface on the baseband board. Two Ethernet cards talk to each other through the E-band system. Since the system is designed for a backhaul system where multipath signals are much less than those in an office environment, the system performance of the system will be underestimated. In the test, a measured SNR above 23 dB was obtained. Accordingly, this leads to a data rate of approximately 9.4 Gbit/s over the air, which demonstrates a good overall performance of the RF subsystem and the complete system.

6 Conclusion

In this study, a low-cost 10-Gbps E-band wireless link with 2.4-bit$\cdot$s$^{-1}\cdot$Hz^{-1} spectral efficiency was built and tested indoors. The system achieved up to 20 G/bit/s when the full 10-GHz bandwidth was used.

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