

Lecture Notes in Computer Science

Edited by G. Goos and J. Hartmanis

374

Kay A. Robbins
Steven Robbins

The Cray X-MP/Model 24

A Case Study in Pipelined Architecture
and Vector Processing



Springer-Verlag

New York Berlin Heidelberg London Paris Tokyo Hong Kong

Editorial Board

D. Barstow W. Brauer P. Brinch Hansen D. Gries D. Luckham
C. Moler A. Pnueli G. Seegmüller J. Stoer N. Wirth

Authors

Kay A. Robbins

Steven Robbins

Division of Mathematics, Computer Science, and Statistics

The University of Texas at San Antonio

San Antonio, TX 78285, USA

CR Subject Classification (1987): C.1.2, D.4.1

ISBN 0-387-97089-4 Springer-Verlag New York Berlin Heidelberg

ISBN 3-540-97089-4 Springer-Verlag Berlin Heidelberg New York

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, re-use of illustrations, recitation, broadcasting, reproduction on microfilms or in other ways, and storage in data banks. Duplication of this publication or parts thereof is only permitted under the provisions of the German Copyright Law of September 9, 1965, in its version of June 24, 1985, and a copyright fee must always be paid. Violations fall under the prosecution act of the German Copyright Law.

© Springer-Verlag Berlin Heidelberg 1989

Printed in Germany

Printing and binding: Druckhaus Beltz, Hemsbach/Bergstr.

2145/3140-543210 – Printed on acid-free paper

Contents

Preface	iii
1 Overview of the Cray X-MP/Model 24	1
1.1 Introduction	1
1.2 The Cray X-MP/Model 24 Architecture	2
2 The Control Section	4
2.1 The Instruction Cycle	4
2.2 The Instruction Issue Phase	5
2.3 The Instruction Buffers and the Instruction Fetch	7
2.4 Instruction Execution	10
3 The Scalar Section	11
3.1 The Scalar Section Hardware	11
3.2 Execution in the Scalar Section	13
4 The Address Section	17
4.1 The Address Section Hardware	17
4.2 Addresses on the Cray X-MP	19
5 Vectors and Vector Operations	21
5.1 Basic Operation of the Vector Section	21
5.2 Instruction Issue and Source Register Reservation	25
5.3 Result Register Reservations and Chaining	28
5.4 Vector Memory Operations Without Conflicts	30
5.5 Vectorization	31
5.6 The Effect of Dependencies on Vectorization	40
6 Memory Access	44
6.1 Memory Organization	44
6.2 Scalar Memory Transfers	44
6.3 Vector Transfers	47
6.4 Memory Conflicts for Vector Operations	49
6.5 Bidirectional Memory Access	54
6.6 Instruction Fetches	56

7	Interprocessor Communication and Multitasking	57
7.1	Introduction	57
7.2	Shared Memory on the Dual Processor System	58
7.3	Hardware Support for Interprocessor Communication	58
7.4	The Test-And-Set Operation for Mutual Exclusion	59
7.5	Multiprogramming	61
7.6	The Busy Waiting Problem	62
7.7	Fortran Locks and Events	65
7.8	Fortran Tasks	67
7.9	Static Scheduling and Self-scheduling of Loops	75
7.10	The Future	78
A	PMS Diagram of the Cray X-MP I/O Subsystem	80
B	Exchange Package for the Cray X-MP	82
C	Lawrence Livermore Loops	85
D	Sample Programs	88
D.1	Introduction	88
D.2	Examples from Chapter 3	91
D.3	Examples from Chapter 5	96
D.4	Examples from Chapters 6 and 7	110
E	Instruction Execution Summary for the Cray X-MP	125
F	XMPSIM Users Manual	145
F.1	Introduction	145
F.2	Basic Simulator Operation	145
F.3	The Cray X-MP Instruction Cycle	148
F.4	Creating a Source Program	150
F.5	Invoking the Simulator	150
F.6	The Main Display	153
F.7	The Configuration Menu	153
F.8	Description of the Assembly Phase	157
F.9	Tokenization of Cray Assembly Language Instructions	158
F.10	Internal Data Structures	161
F.11	Data Types for Numeric Values	161
F.12	Simulator Restrictions	162
	Bibliography	163

Preface

This monograph examines the issues relevant to the design of vector and pipelined computer systems. The Cray X-MP/24 is used as a case study to examine how design tradeoffs affect performance. Enough technical details are provided so that a reader may work out timings for the Cray X-MP without reference to a hardware manual.

We hope that a serious look at the details of the design will give the reader insights that a superficial discussion cannot yield. Our study left us with a great appreciation of the machine and an admiration for its designers. The insights we have given will be useful to the scientist who would like to obtain maximum performance from a vector machine, to the computer science student, and to the compiler writer. This monograph can also be used to supplement a regular textbook such as Baer [2] or Stone [44] in a graduate or senior level course in computer architecture.

The book begins with an overview of the Cray X-MP system. Chapter 2 discusses various aspects of control including the instruction cycle, the management of the instruction buffers, and the instruction issue mechanism. The scalar section is examined in Chapter 3 and the addressing mechanism is examined in Chapter 4. Chapter 5 discusses vectorization and chaining. Chapter 6 looks at memory access and conflict resolution. Multi-tasking and interprocessor communication are introduced in Chapter 7. Appendix A gives a PMS diagram of the Cray X-MP, and Appendix B shows the exchange package for the Cray X-MP. Appendix C lists the Lawrence Livermore loops, a standard benchmark for scientific computing. Appendix D shows a list of sample programs and discusses some of the more subtle aspects of performing accurate instruction timings. Appendix E contains a complete list of Cray assembly language instructions and their timings. Appendix F contains the Users Manual for XMPSIM, a Cray simulator which runs on an IBM PC and is available from the authors.

The authors gratefully acknowledge the support of Cray Research through their University of Texas System Grants Program. Computational support was provided by the University of Texas Center for High Performance Computing. Several people have read different versions of this book and made suggestions. We would particularly like to thank Nora Fangon, Alyson Thring, Warren Wayne, Luther Keeler, and Neal Wagner for their helpful comments.