Implementation of Efficient Reconfigurable FIR Filter With Control Logic for 5G Applications

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Research Article

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Abstract

Filters are used to achieve frequency selectivity on the spectrum of input signal. Due to the stability of FIR filters, they are used in most of the applications. In the conventional FIR filters the frequency band is fixed and can't be changed once it is designed. Hence there is a necessity of an FIR filter with auto adjustment of band width. The design of FIR filter requires more number of filter coefficients to get the desired bandwidth specification. This results in a large slice for FPGA implementation. Here it is proposed a state machine to select different FIR filters with the designated set of coefficients. Each FIR filter is having different set of coefficients and based on the frequency of the clock signal the FIR filter is selected. Therefore frequency selectivity can be achieved. The Proposed method is to implement Reconfigurable FIR Filter with control logic for auto adjustment of fre-quency selections to achieve better band width requirements. The filter order is initially selected as 4 and presented the simulation results. The order of the filter(n) increased to 24 for verifying the bandwidth selection. The proposed architecture is compared with the existing architecture with 16bits and 11taps. Simulation results presented are verified using Xilinx ISE design suite 14.7. Total number of 4 input LUTs utilized are 630 for n=24. Power consumed by the overall design is 195mW.

Full-text

Due to technical limitations, full-text HTML conversion of this manuscript could not be completed. However, the manuscript can be downloaded and accessed as a PDF.

Figures

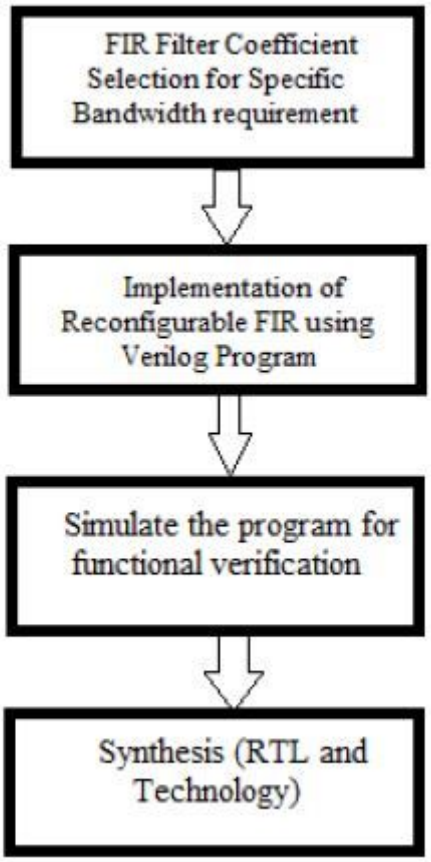

Figure 1

Design Flow

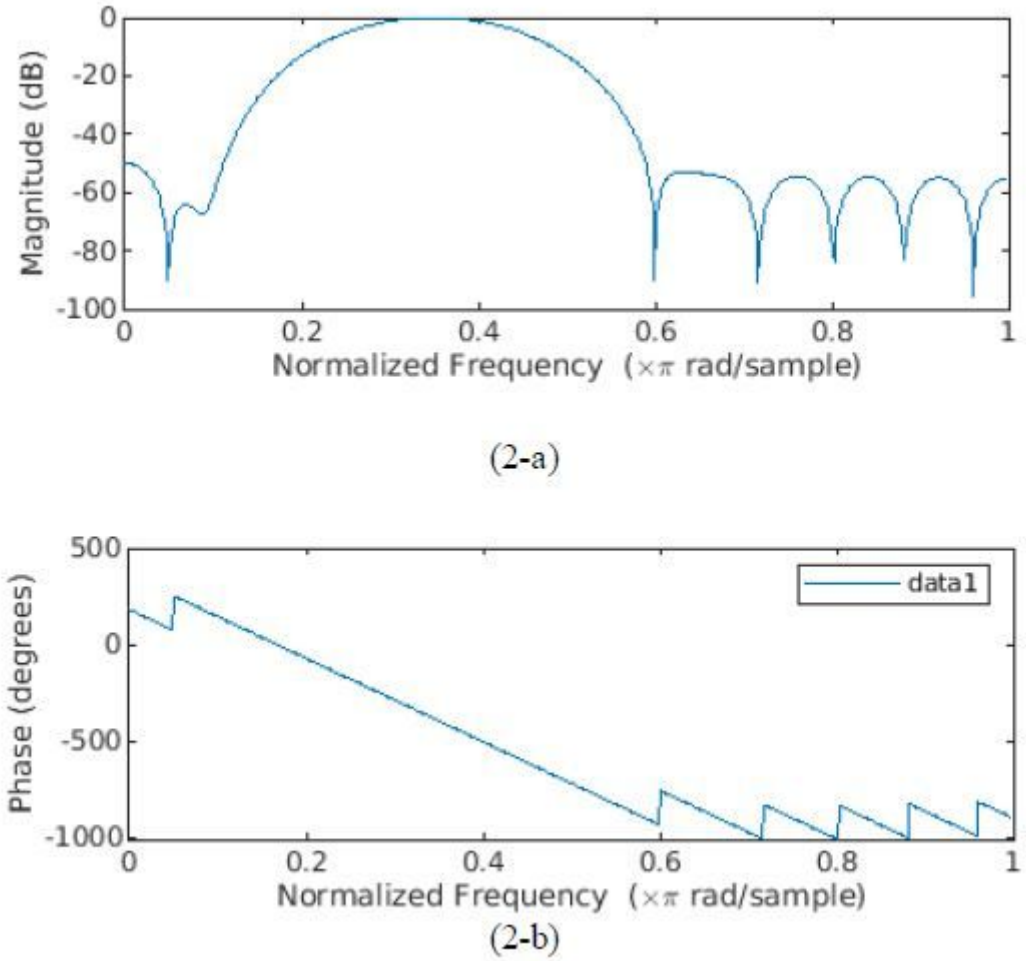

Figure 2

Magnitude (2-a) Phase (2-b) responces with h1 set of coefficients

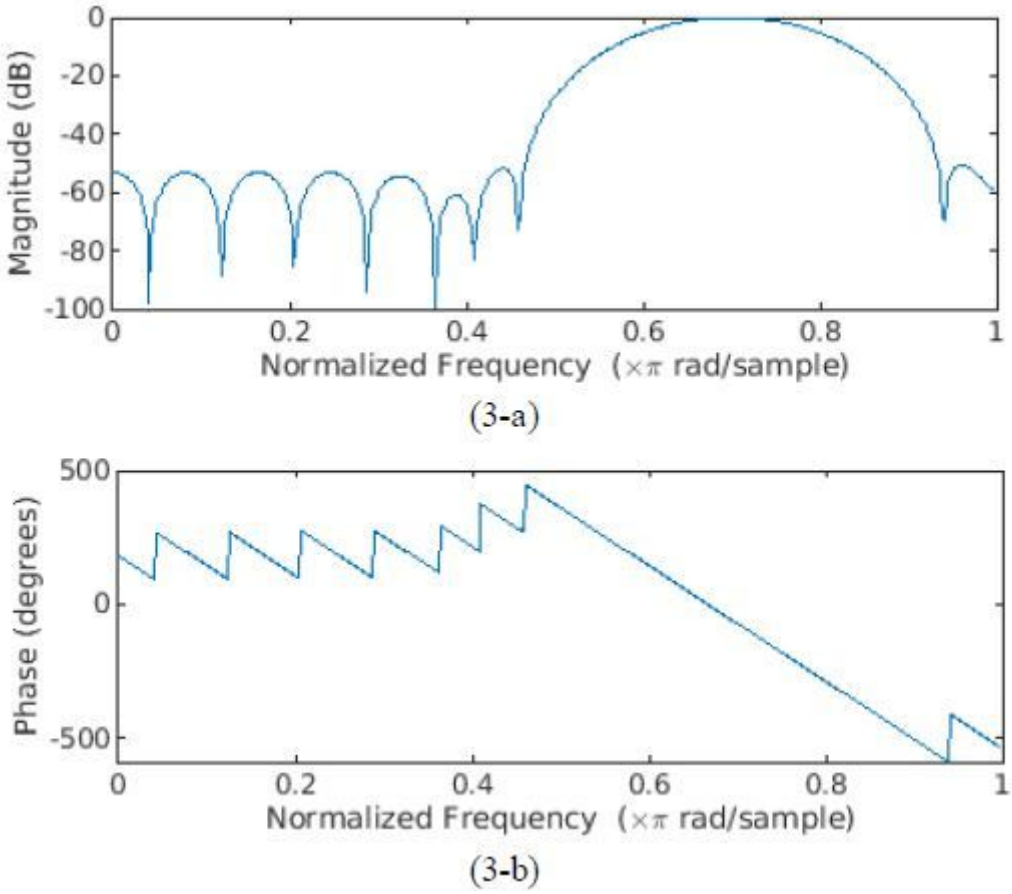

Figure 3

Magnitude (3-a) Phase (3-b) responces with h2 set of coefficients

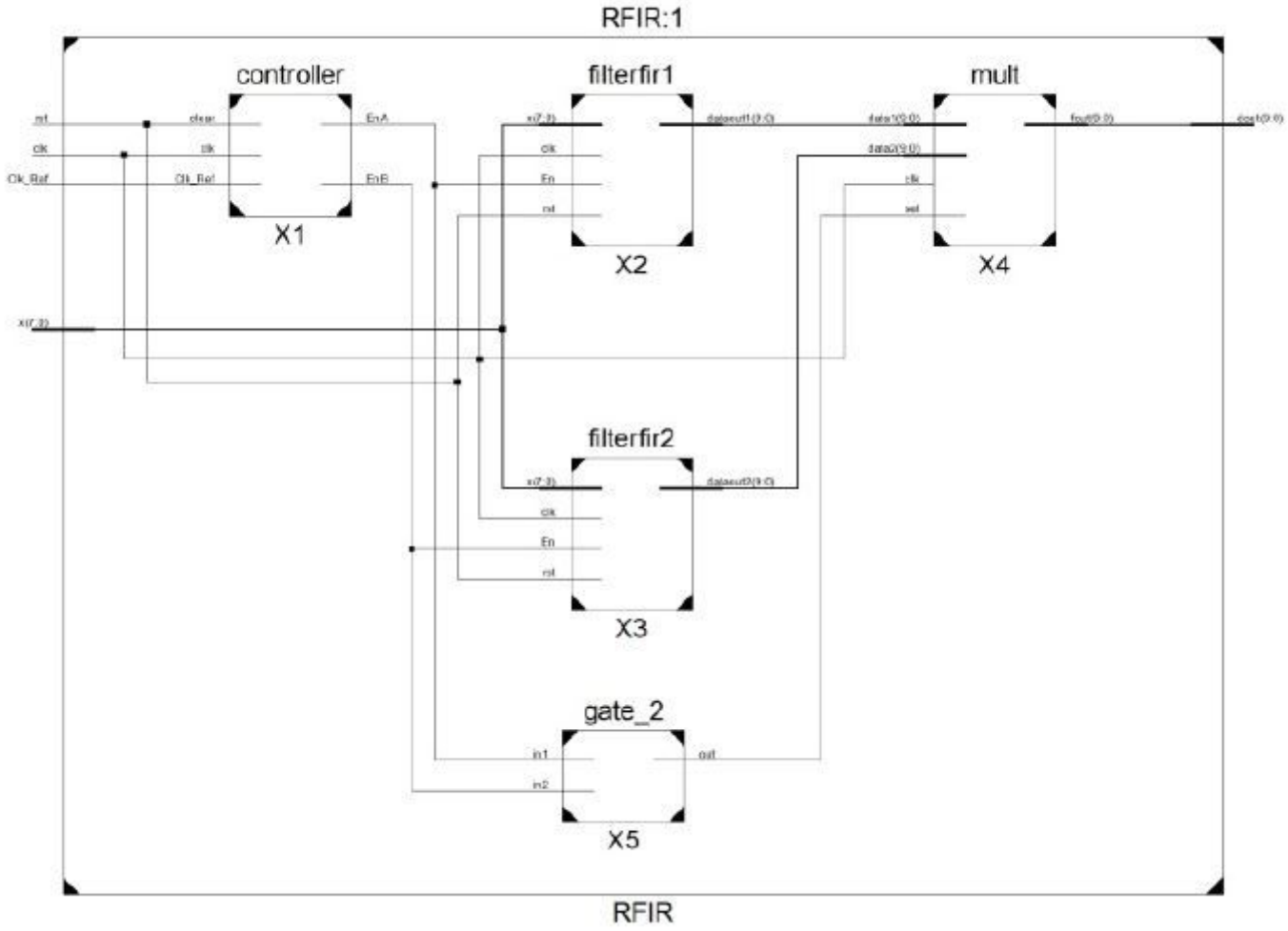

Figure 4

RTL schematic of the Reconfigurable FIR filter with control logic

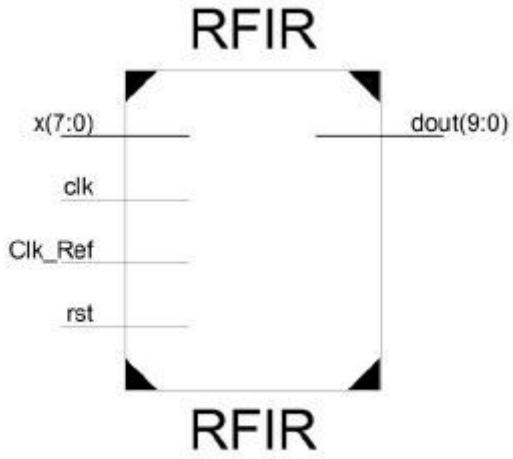

Figure 5

Top Module of Proposed RFIR filter

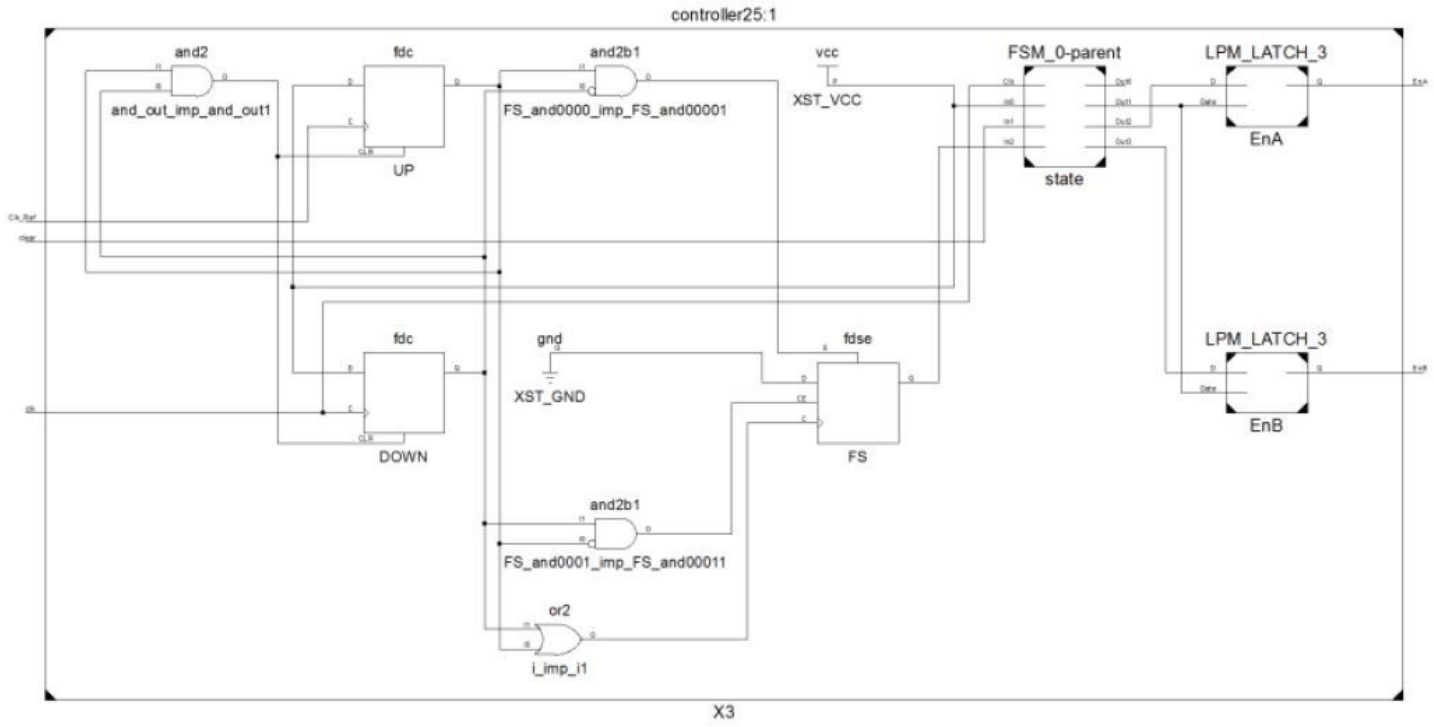

Figure 6

Schematic Diagram of Control Logic

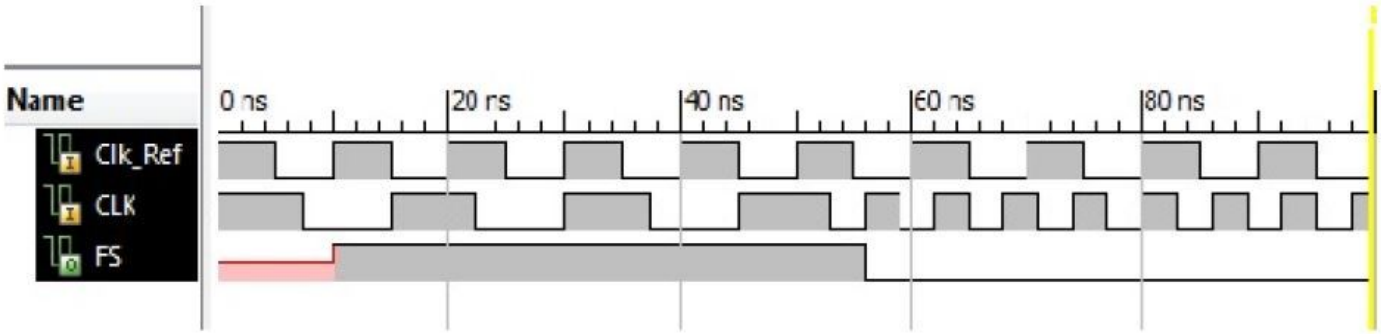

Figure 7

Simulation result of the frequency selection logic in control unit

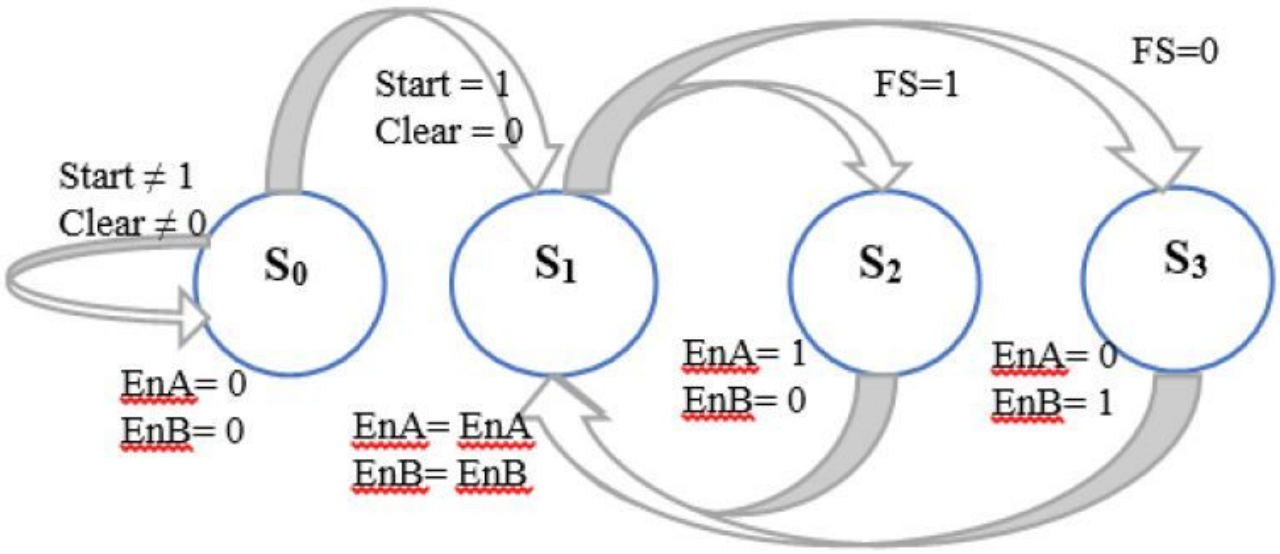

Figure 8

Finite State machine