An Efficient Passive RFID System for Ubiquitous Identification and Sensing Using Impulse UWB Radio

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***Abstract* – The next generation RFID system for ubiquitous identification and sensing requires both energy and system efficiency. This paper describes an efficient passive RFID system using impulse ultra-wideband radio (IR-UWB), at a 10m operation range. Unlike conventional passive RFID systems which rely on backscatter and narrowband radio, IR-UWB is introduced as the uplink (communication from a tag to a reader). By utilizing a specialized communication protocol and a novel ALOHA-based anti-collision algorithm, such Semi-UWB architecture enables a high network throughput (2000 tag/sec) under the low power and low cost constraint. A tag design for proof of concept is finally presented.**

I. INTRODUCTION

Radio frequency Identification (RFID) applications with sensor circuitry are expected as a key component in the future's ubiquitous intelligence and computing. These RFID-based identification and sensing systems have potentially a wide range of applications such as product tracking, space and environment monitoring and positioning. The passive RFID system with battery-free tags is more attractive since the tag is small size, low cost, long life cycle and free-maintenance, compared to the active one. Backscatter is one of the most commonly used techniques in current passive RFID systems. Tags backscatter the incoming RF signal from the reader, change the antenna load to modulate the data [1]. This simple implementation, unfortunately, is suffering from several disadvantages. It is very sensitive to interference, multi-path fading, multi-user interference and collision problem, and it is susceptible to passive and active attack [2]. Therefore, such a solution is no longer acceptable for the new generation of RFID which requires higher data rate, longer operation range and faster processing speed, while maintaining low power and low cost.

The Federal Communications Commission (FCC) defines a radio system to be an UWB system if the fractional bandwidth *Bf* or the −10 dB bandwidth of the signal is greater than 20% or at least 500 MHz, respectively [3]. Impulse ultra-wideband radio (IR-UWB) uses short pulses (nanoseconds) to spread energy over at least 500 MHz of bandwidth [4]. It is a promising solution for short distance, low to moderate data rate, low cost, highly integrated, and low power radio communication such as RFID, and wireless sensor in ubiquitous intelligence and computing environment. In contrast to conventional RF communication systems, IR-UWB transmitters generate very short pulses that are able to propagate without an additional RF mixing stage [5]. The baseband-like architecture with low duty cycle signal guarantees low complexity and low power. On the other hand, it is resistant to severe multi-path, and has good time domain resolution allowing for location and tracking applications. Noise-like signal with ultra broad bandwidth provides robust and high speed communication links. It can achieve high processing speed, long operation range, and high security.

A novel RFID system at 10m using IR-UWB with asymmetric wireless links is suggested in this work. We use different communication schemes at the uplink and the downlink, individually. Readers broadcast conventional RF signals which carry commands, the clock and energy to tags, whereas, IR-UWB is applied in the reverse link. This Semi-UWB architecture does not only speed up the data rate of tag to reader transmission, but also control the tag power consumption in a target level. In addition, we devise a specified transmission protocol that can improve the network throughput in a multi-tag environment. By using the pipelined communication scheme and the enhanced adaptive framed ALOHA anti-collision algorithm, 1000 tags can be processed within 500msec. A tag is designed and implemented based on the proposed system specification. It consists of a power scavenging unit; a RF receiver; an IR-UWB transmitter; an embedded UWB antenna and a digital baseband. The digital baseband processor is composed by several modules such as control unit, pseudo random number generator, slot counter and memory. After simulation and verification (FPGA prototype), it is implemented with Synopsys DC for synthesis and Cadence SoC Encounter for layout. The chip will be fabricated and tested integrated with the front-end (transmitter and receiver) in UMC 0.18μm process.

II. SYSTEM SPECIFICATION

A. Design Consideration

Compared with other wireless communication systems, RFID holds some characteristics that need to be concerned during the system level design.

- *System capacity:* A huge number of tags might appear in a reading zone simultaneously. Further more, due to the massive tags environment; multi-access (anti-collision) algorithm is essential for the system efficiency.
- *Asymmetrical traffic loads and resources:* Unlike other RF communication systems, the traffic loads of RFID are highly asymmetrical between the uplink and the downlink. The data (e.g. synchronization, command) broadcasted from the reader is small, but the traffic transmitted by a great number of tags in the field is rather heavy. In the hardware perspective, tags have very limited resource such as memory, power supply, and computational ability, but a reader can be a powerful device.
- *Reading speed:* Reading speed in terms of processing delay is an important metric. High processing speed could be achieved by either a high data rate link for the tag to reader communication, or an efficient anti-collision algorithm.
- *Low power and low complexity hardware implementation:* Because RFID tags are resource-limited devices, the implementation upon the system specification must be simple and energy-efficient.

B. Semi-UWB Architecture

On the basis of the considerations above, we propose a Semi-UWB system architecture illustrated in figure 1. Due to the nature of the impulse UWB radio, the IR-UWB transmitter integrated on the RFID tag provides a robust, high speed and high security uplink under a low power and low complexity implementation. Instead of the typical full-UWB system, the traditional RF transceiver is applied as the downlink, for reasons that 1) the extremely high power consuming and complex UWB receiver is not feasible for resource-limited RFID tags; 2) The low downlink traffic becomes

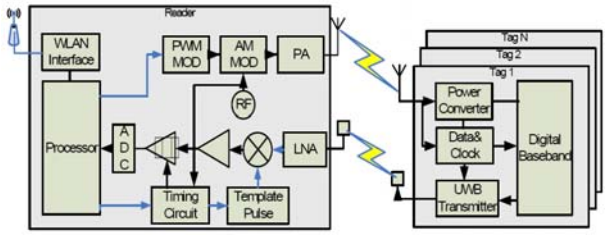

FIGURE 1 – THE ASYMMETRICAL COMMUNICATION ARCHITECTURE

insignificant for the system efficiency, hence a low data rate narrowband radio is adequate.

The reader broadcasts commands to tags using UHF (860MHz ~ 960MHz). The modulation is ASK with pulse interval encoding (PIE). The data rate (clock frequency) is adaptive from 40Kbps (KHz) to 160 Kbps (KHz) controlled by the reader. A tag replies information by transmitting UWB signal with a fixed data rate of 1Mbps. The UWB pulse rate is 10MHz, i.e. each bit of information is represented with a sequence of 10 pulses with a width equal to *Tp* = 500ps. The modulation options include OOK or PPM, depending on the type of the IR-UWB transmitter [6].

C. Data Communication Protocol

1). Operation Procedure

The specification in higher levels is a further issue that determines the energy efficiency as well as the system throughput. Hereby, we devise a specified data communication protocol for the proposed Semi-UWB architecture. Five functions are defined in the proposed protocol, namely **Wakeup**, **Request**, **Write**, **Modify** and **Kill**. The Wakeup and the Request are basic operations for identifying tags or gathering data. The Wakeup activates and identifies all tags in the reading field while the Request performs the similar function as the Wakeup, but does not affect the identified tags. Write, Modify and Kill are used to program tags. The Write is usually used to program the storage element for the first time. The operation of Modify and Kill are for a specific tag and only a single tag should response.

- *Wakeup*: Identify all tags in the reading field.
- *Request*: Identify the tags that have not been identified in the reading field.
- *Write*: Program tag's memory unconditionally.
- *Modify*: Program a specific tag with access control.
- *Kill:* Delete a specific tag.

The frame format, also called round, which represents an operation initiated by readers, is composed by four phases: powering, start of frame (SOF), commands, and processing. In the powering phase, the reader radiates continuous sinusoid wave to power passive tags. A SOF is used for frame synchronization. The sequence consists of ten continuous bit 0s and a bit 1. Afterwards, tags decode the received command and response the reader.

An acknowledgement mechanism is employed to guarantee the successful receptions and to disable the identified tags. Unlike traditional RFID where data integrity (QoS) is controlled by both readers and tags such as CRC check, in our work, only readers take charge of error handling. As a result, CRC checker can be removed from a tag that reduces the complexity. In each valid operation, the tag sends its current data and the reader checks the correctness of the operation. Because the uplink speed is high, this approach will not cause the processing delay even transmitting whole data. Besides, low energy consumption of UWB signal enables data transmission in the passive system.

A tag should maintain three control flags indicating its current status.

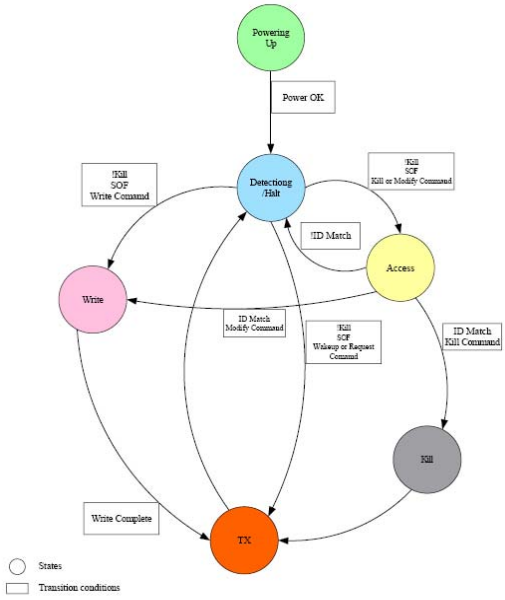

FIGURE 2 – THE STATE TRANSITION DIAGRAM

- *ACK*: Positive acknowledgment. It indicates this tag has been identified.
- *NAK*: Negative acknowledgment. It is formed by an N-bit counter that is increased by 1 for each failed transmission.
- *Kill*: A tag which has been deleted permanently.

The states transition diagram of the central controller is shown in figure 2.

- *Powering Up State*: Tags capture power by the power scavenging units and store in a relatively big capacitor.
- *Halt/Detecting State*: This is the initial state of each powered tag. In this state, tags are detecting incoming signals and capturing SOF and Command. After this state, tags enter a new frame to execute the corresponding operation.
- *Transmitting State*: A tag executes three procedures during transmitting state. First step is to load data into the transmitting cache and generate a PN code. Secondly, a slots counter in the tag counts down the PN code until it reaches 0. Finally, the tag sends the data and waits for ACK or NAK.
- *Writing State*: A tag programs its memory by receiving data from the reader.
- *Access State*: This state comes before an operation for a specific tag (Modify and Kill Commands). The tag compares its data with the incoming data bit by bit. This state is interrupted by different bits. Only one tag with the same data completes the state.
- *Kill State*: It sets the Kill Flag to permanently disable the tag.

2). Anti-Collisions

All tags in the reading filed respond after receiving either Wakeup or Request commands. However their responses may collide on the radio channel, therefore can not be received by the reader. The problem referred to as the Tag-collision. An effective system must avoid this collision by using anti-collision algorithm in order to enable the reader to collect many tags simultaneously. In order to increase its feasibility and efficiency, several versions of the ALOHA algorithm are presented in [7]. Among them, the most widely used one in wireless sensor and identification systems is the framed slotted ALOHA algorithm. Time is divided into discrete time intervals, called slots. A frame is a time interval between requests of a reader and consists of a number of slots. A tag randomly selects a slot in the frame and responds to the reader. A procedure called acknowledgment is required to resolve collisions

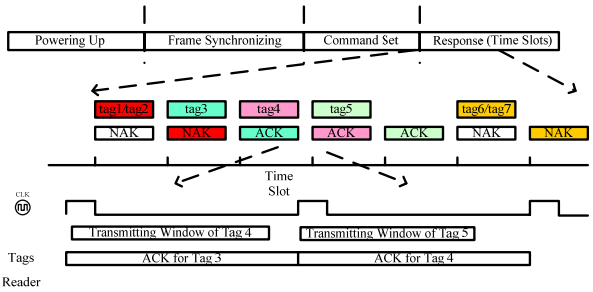

FIGURE 3 – FRAME FORMAT AND THE PIPELINE COMMUNICATION SCHEME

or failed transmissions. Collided tags retransmit in the next frame [8].

The overall goal of the anti-collision algorithm is to reduce the retrieving period with simply hardware implementation and low power consumption. To improve network throughput, we propose a more efficient scheme to overcome the anti-collision problem. It is based on the framed slotted ALOHA algorithm by employing following improvements. 1) We use a pipelined scheme to overcome the bottleneck caused by the low data rate downlink. In conventional approaches, a time slot contains a tag's data packet and the acknowledgement from the reader. Because of great asymmetry between the downlink and the uplink (UWB data rate is much higher than the narrowband radio data rate), the acknowledgement sent by the reader to tags becomes a bottleneck that degrades the network throughput. This problem can be solved by using a pipelined method posing the data packet and its corresponding acknowledgement in two adjacent slots. As can be seen in figure 3, a tag transmits data in the slot K, and then receives the corresponding ACK in the slot K + 1. 2) The maximum system efficiency of the framed slotted ALOHA is achieved when the N approximately equals to n, where N is the frame size and n is the tag number [8]. Dynamic frame sizes allocation replaces the traditional fixed framed ALOHA. With the tag number estimation algorithm [9], the reader can estimate the number of tags, and regulate the optimized frame size. 3) The reader skips idle slots using the scalable global clock controlled by the reader. It eliminates the delay introduced by empty slots.

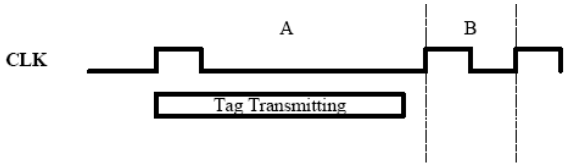

FIGURE 4 –SKETCH OF IDLE SLOT SKIPPING

3). Performance Analysis

Hereby, the system efficiency is defined as the ratio of the successful transmission time to the frame size. Given N slots and n tags, the number of r of tags in one same slot is binomially distributed as (1), the maximum system efficiency of the Framed

$$B_{n,\frac{1}{N}}(r)=\binom{n}{r}\left(\frac{1}{N}\right)\left(1-\frac{1}{N}\right)^{n-1} \quad (1)$$

Slotted Aloha is achieved when the N approximately equals to n [8]. If the frame size is small but the number of tags is large, too many collisions will occur and the fraction of identified tags will degrade. On the other hand, when the number of tags is much lower than the number of slots, the wasted slots can occur. As the description in the previous section, the dynamic frame size allocation can provide the optimal frame size to achieve the maximum throughput. Moreover, the idle skipping method can eliminate the delay caused by the empty slots. The simulation results of the system performance are shown in figure 5 and figure 6. As can be seen, more than 1000 tags can be processed within 500ms. Table 1 presents the comparison result with some standardized RFID protocols.

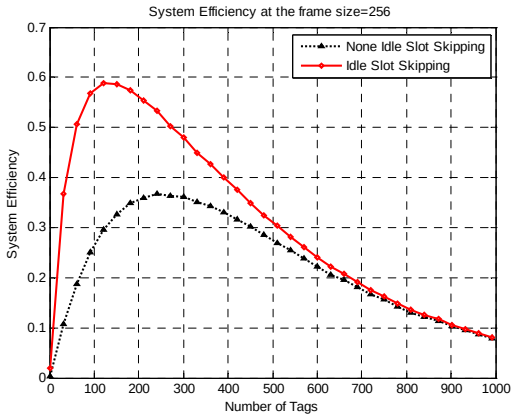

FIGURE 5 – SIMULATION RESULT OF THE SYSTEM EFFICIENCY

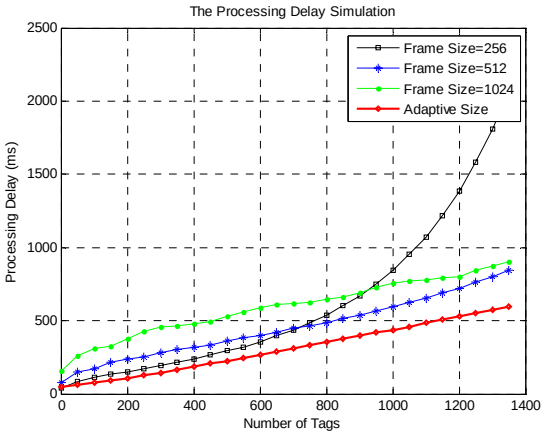

FIGURE 6 – SIMULATION RESULT OF THE PROCESSING DELAY

TABLE 1 COMPARISON OF DIFFERENT STANDARDIZED PROTOCOLS

Standards	Frequencies	Data Speed T→R	Processing Speed	Anti Collision
ISO 18000-3 Mode 2	HF	106 Kbps	1200 tags/sec	Not Specified
ISO 18000-6 A	UHF	40 Kbps	100 tag/sec	Framed Aloha
ISO 18000-6 B	UHF	40 Kbps	100 tags/sec	Binary Tree Search
EPC Class 0	UHF	Max 80 Kbps	200~800 tags/sec	binary tree search
EPC C1G2	UHF	Max 140 Kbps	1000 tags/sec	Framed Aloha
This Work	Semi-UWB	1Mbps	>2000 tags/sec	Enhanced Framed Aloha

III. Proof of Concept Design

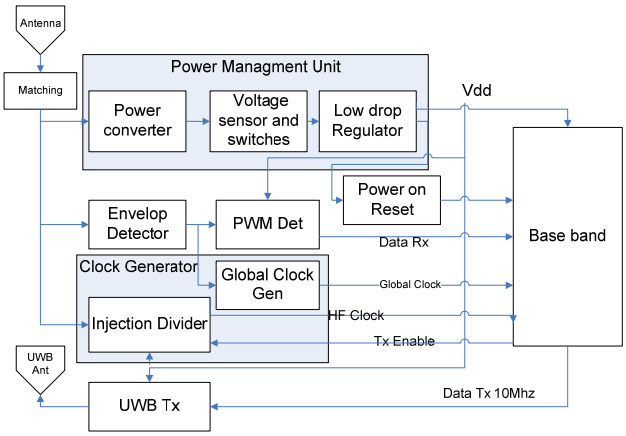

Figure 7 – Block Diagram of Semi-UWB RFID Tags

A low power and low complexity Semi-UWB RFID tag for proof of concept is designed (figure 7). The module consists of five parts: a narrowband receiver, a UWB transmitter, a power scavenging unit, a clock circuitry, and a digital baseband. The narrowband receiver receives RF signal and demodulates it into digital signal. The power scavenging unit converts the incoming RF signal to DC voltage and supplies the whole circuitry of the tag. It also generates a power-on-rest signal to the baseband when the capacitor is charged. A low frequency clock is captured from the received data as the baseband control. Another high frequency clock for the UWB pulse generator is imported by dividing the carrier of the incoming RF signal. The digital baseband is responsible for control, i.e., decodes commands, programs memory, fetch data, and exports data to the transmitter. Detailed circuit design and implementation issues are discussed in [2].

A protocol processor of RFID tags is designed to meet the specification of the previous section. Figure 8 illustrates the block diagram of the baseband processor. The control unit is formed by several FSMs which generate control signals to each sub module whereas sub modules send status signals to the control unit. A 128-bit memory is organized in three segments: 64 bits ID, 16 bits CRC and 48 bits reserved for other data. The pseudo number generator (PNG) and the slot counter are used to implement the transmission protocol and the anti-collision algorithm. The TX cache is a multi-clock module. Data is loaded into TX cache or transmitted to FSM using global clock. During the transmitting process, it uses 1 MHz clock to send the data to the modulator where generates 10 MHz digital signal to the front-end. The circuit simulation is successful and the design is tested by FPGA prototype. The ASIC for UMC 0.18µm is implemented using Synopsys DC for synthesis and Cadence SoC encounter for layout. The final results are summarized in table 2.

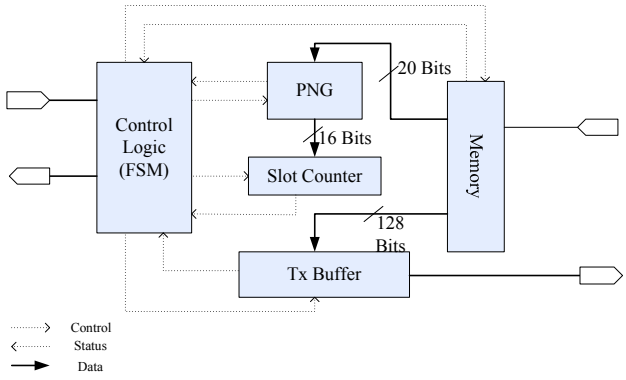

Figure 8 - Block Diagram of The Protocol Processor

IV. Conclusion

The future RFID-based ubiquitous identification and sensing applications expect both energy efficiency and system efficiency. A novel RFID system using impulse UWB technique is presented in this paper. The asymmetrical architecture and the specified communication protocol increase the processing speed and network throughput. A tag module is designed, and the simulation shows that the power consumption of the tag module is feasible for the battery-free passive system. Future work will be conducted by tag chip type-out and reader development.

Table 1 Implementation Result of The Protocol Processor

Radio Links	Rx	I-UWB
	Tx	UHF
Data Rate	Rx	40~160Kbps, Adaptive
	Tx	1Mbps
Functions		Write, Request, Wakeup, Kill, Modify
Anti-Collision		Enhanced Framed Slotted ALOHA
Process		UMC 0.18µm
Voltage Supply		1.8V
Power Consumption		Dynamic Power = 652.1648 nW Leakage Power = 148.3046 nW
Area		Combinational Area = 10348 Noncombinational Area = 24121

Acknowledgment

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