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A 0.46–0.52-THz fully-differential quasi-monostatic FMCW radar transceiver in 90-nm SiGe BiCMOS

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Abstract A 0.46–0.52-THz fully-differential quasi-monostatic frequency-modulated continuous-wave (FMCW) radar transceiver was designed in a 90-nm SiGe bipolar CMOS technology with f_T/f_{max} of 300/480 GHz. The transceiver chip has an area of 2.84 mm^2. A multiply-by-24 frequency multiplier chain is used to generate a 0.48-THz signal from a 20-GHz input signal. Two 0.48-THz push–push doublers are driven in quadrature for a differential output signal with a measured effective isotropic radiated power of up to −8.8 dBm at the transmitter at 0.47 THz. A differential subharmonic receiver mixer with a stacked quad topology achieves a measured system conversion gain of 7 dB and a measured single-sideband noise figure of 25.2 dB at 0.471 THz. FMCW radar measurements are performed using an on-board frequency source of a credit card-sized demonstrator at a bandwidth of 60 GHz.

Keywords Frequency-modulated continuous-wave (FMCW) radar · On-chip antenna · SiGe bipolar CMOS (BiCMOS) · Subharmonic mixer · Terahertz (THz)

Ein 0,46–0,52 THz volldifferenzieller quasi-monostatischer FMCW Radar-Sendeempfänger in 90 nm SiGe BiCMOS

Zusammenfassung Ein 0,46–0,52 THz volldifferenzieller quasi-monostatischer frequency-modulated continuous-wave (FMCW) Radar-Sendeempfänger wurde in einer 90 nm SiGe Bipolar CMOS-Technologie mit f_T/f_{max} von 300/480 GHz entworfen. Der Sendeempfänger Chip hat eine Fläche von 2,84 mm^2. Ein Frequenzmultiplizierer mit Multiplikationsfaktor von 24 wurde verwendet, um ein 0,48 THz-Signal von einem 20 GHz-Eingangssignal zu generieren. Zwei 0,48 THz push–push-Frequenzverdoppler werden in Quadratur getrieben für ein differenzielles Ausgangssignal mit einer gemessenen äquivalenten isotropen Strahlungsleistung von bis zu −8,8 dBm am Sender bei 0,47 THz. Ein differenzieller subharmonischer Mischer mit gestapelten Schalttransistoren in der Gilbertzelle erreicht einen gemessenen Systemgewinn von 7 dB und eine gemessene Rauschzahl von 25,2 dB bei 0,471 THz. FMCW Radar-Messungen wurden mit einer PLL-basierten Signalquelle in einem Demonstrator im Kreditkartenformat mit einer Bandbreite von 60 GHz ausgeführt.

Schlüsselwörter Frequency-modulated continuous-wave(FMCW)-Radar · On Chip-Antenne · SiGe Bipolar CMOS (BiCMOS) · subharmonischer Mischer · Terahertz (THz)

1 Introduction

Radar applications benefit from the large achievable bandwidths in the terahertz (THz) frequency range, resulting in a range resolution in the single-digit millimeter range. Traditionally, terahertz frequencies have been explored using split-block designs with III-V compound semiconductor Schottky diode frequency multiplier and driving amplifier chains. Although these designs achieve the highest performance in terms of noise figure and output power, the overall system size and scalability for low-cost mass-market deployment in a compact demonstrator is challenging. One example of such a diode multiplier-

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based split-block design is a vector network analyzer (VNA) frequency extender module which has been utilized at 0.85–1.1 THz [2] and at 1.1–1.5 THz [3] for radar operation typically occupying at least 20 cm in the largest dimension with a mass towards the kilogram range. Additionally, custom split-block radar designs have been demonstrated at 0.58 THz [4] and 0.675 THz [5] using GaAs Schottky-diode multipliers, with system sizes comparable to the VNA frequency extender modules.

In comparison, low-cost silicon-integrated technologies such as SiGe bipolar CMOS (BiCMOS) and CMOS have been outlined as a viable technology option [6] for future mass-market terahertz designs. Nevertheless, these production technologies in silicon only reach f_{max} of around 500 GHz, with recent advancements in SiGe BiCMOS achieving f_{max} of 670 GHz [7]. The performance is considerably lower compared to III-V technologies which have shown power amplification at 1 THz [8] with f_T/f_{max} of 0.61/1.5 THz indium phosphide HEMTs. This trend is illustrated in Fig. 1, where saturated output power measurements of power amplifiers above 500 GHz have only been shown in III-V technologies, with silicon-integrated power amplifiers plateauing around 300 GHz.

Therefore, there is a strong interest to fill the perceived terahertz gap in silicon-integrated technologies using transceivers with high integration levels for a compact and low-cost system demonstrator. Currently, state-of-the-art frequency-modulated continuous-wave (FMCW) radar transceivers in silicon-integrated technologies have been shown at 220–320 GHz in 65-nm CMOS [9], at 311–338 GHz [10], at 367–382 GHz [11] in 130-nm SiGe BiCMOS. More recently, a FMCW radar demonstrator was introduced at 0.45–0.49 THz in a monostatic configuration [12].

This paper proposes a 90-nm SiGe BiCMOS fully-differential quasi-monostatic 0.46–0.52-THz FMCW radar transceiver. Fully-differential dual-stacked patch antennas are integrated on chip, removing the otherwise required lossy, hard-to-model and unfeasible chip-to-board or chip-to-package interface. The f_T and f_{max} of the technology is 300 GHz and 480 GHz, respectively. This work is able to further extend the frequency range of the 240-GHz radar transceiver architecture [13] consisting of a fully-differential quadrature push–push doubler at the transmitter (TX) and a fully-differential subharmonic dual-stacked switching quad mixer [14] at the receiver (RX). Nevertheless, with this work, we are able to demonstrate subharmonic operation up to and beyond the technology's f_{max} of 480 GHz. The previously implemented radar transceiver [13] in a prior-generation technology with an f_T/f_{max} of 250/370 GHz was operating well below the f_{max} at 240 GHz. Although the single-ended monostatic architecture [12] is able to achieve a smaller area, it is limited in terms of the maximum permissible output power due to poor TX-RX isolation in the dual-use frequency doubler and subharmonic mixer circuit. When considering future improvements in SiGe BiCMOS [7] the proposed fully-differential quasi-monostatic architecture, expanded from [15] can accommodate future power amplifiers at the transmitter given a simulated 57 dB isolation between TX and RX antennas. The measured effective isotropic radiated power (EIRP) is −8.8 dBm at 0.47 THz and the measured single-sideband noise figure (NF_{SSB}) is 25.2 dB at 0.471 THz.

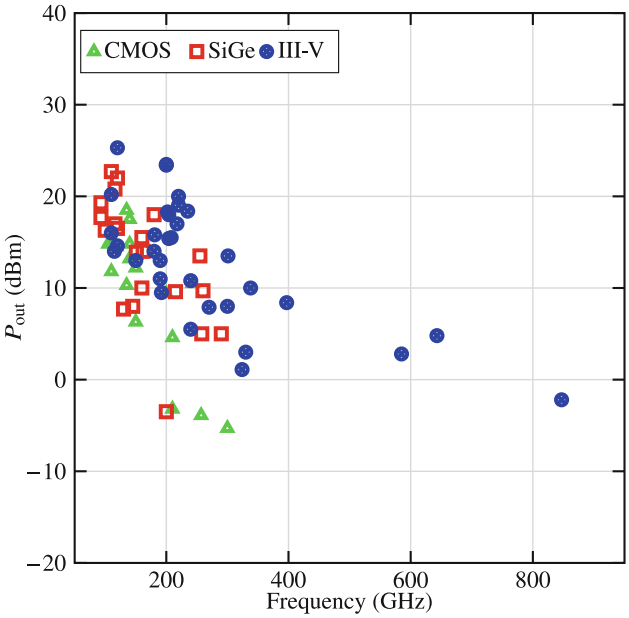


Fig. 1 Amplifier saturated output power versus frequency, from [1]

2 Transceiver design

The overall transceiver architecture is illustrated in Fig. 2a and consists of a frequency multiplier-based approach. At 20 GHz, an off-chip local oscillator (LO) signal originating from a phase-locked loop (PLL) synthesizer is applied as the input of the 0.48-THz transceiver. The first block, grouped as a ×6 frequency multiplier consists of a one-transistor active balun, a cascoded differential pair tripler and a bootstrapped frequency doubler from [16], depicted in Fig. 3 to achieve a 120-GHz signal. The TX-RX LO path is divided using a 120-GHz fully-differential branchline coupler. After the TX-RX division, a further bootstrapped frequency doubler circuit multiplies the LO frequency to 240 GHz on both the RX and TX path. On the TX side, a quadrature push–push doubler architecture is chosen to achieve a differential signal at 0.48 THz. The required 90° phase shift between the inputs of the two parallel common collector push–push doublers detailed in Fig. 4a, is achieved using a 240-GHz fully-differential branchline coupler. The 0.48-THz quadrature doublers, are driven by three stages

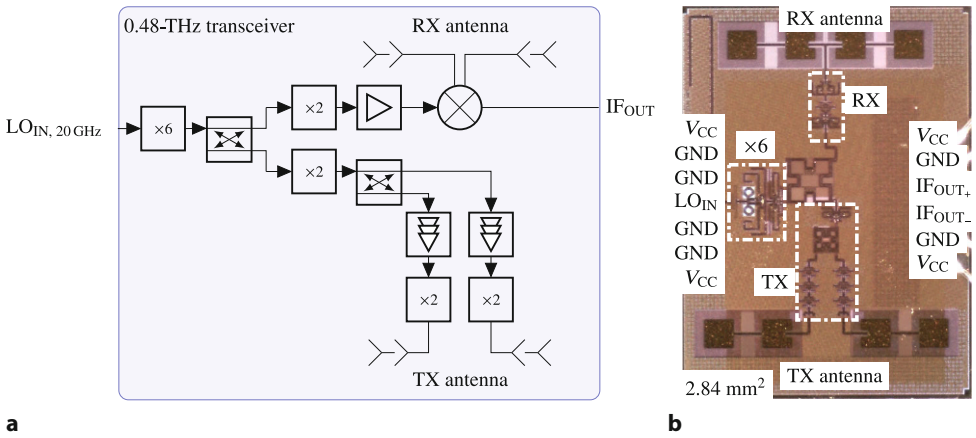
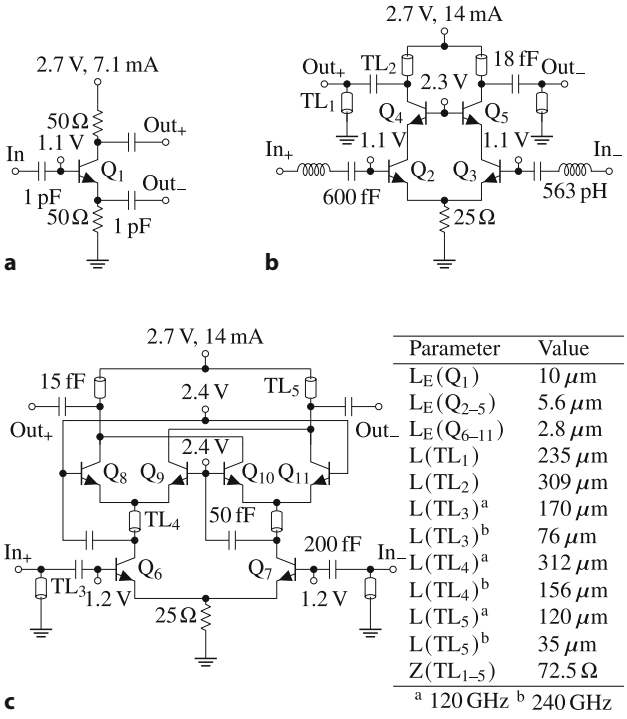


Fig. 2 **a** Block diagram of the 0.48-THz transceiver and **b** chip micrograph of the wire-bonded 2.84-mm^2 radar transceiver chip



Parameter	Value
$L_E(Q_1)$	10 µm
$L_E(Q_{2-5})$	5.6 µm
$L_E(Q_{6-11})$	2.8 µm
$L(TL_1)$	235 µm
$L(TL_2)$	309 µm
$L(TL_3)^a$	170 µm
$L(TL_3)^b$	76 µm
$L(TL_4)^a$	312 µm
$L(TL_4)^b$	156 µm
$L(TL_5)^a$	120 µm
$L(TL_5)^b$	35 µm
$Z(TL_{1-5})$	72.5 Ω

[a] 120 GHz [b] 240 GHz

Fig. 3 Times 6 frequency multiplier chain schematic diagrams of **a** 20-GHz balun, **b** 20-to-60-GHz frequency tripler and **c** 120-GHz frequency doubler. The 240-GHz frequency doubler schematic is comparable to the 120-GHz frequency doubler schematic with adjusted transmission line lengths. The bias circuit current consumption is included in the total current consumption

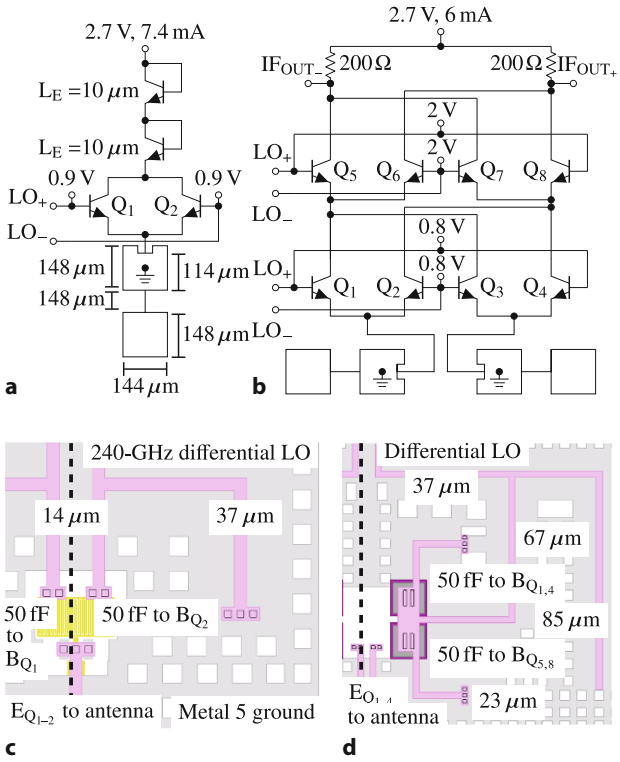


Fig. 4 Schematic diagram of **a** 0.48-THz common collector push–push frequency doubler, **b** 0.48-THz dual-stacked switching quad subharmonic mixer. The symmetric (dashed line) half-layout of the matching circuitry is shown in **c** and **d**, respectively. Transistors are sized with 2.8 µm emitter length, unless annotated otherwise. Single-ended transmission lines have an impedance of 72.5 Ω and the differential transmission lines have an impedance of 100 Ω. RF input matching at the mixer is achieved with a 80 µm long 65-Ω differential line. The bias circuit current consumption is included in the total current consumption

of amplifiers to compensate for insertion losses of the 240-GHz branchline coupler.

The subharmonic mixer on the RX side, depicted in Fig. 4b uses a dc-connection to the on-chip RX antenna array. The mixing process is essentially divided into two parts. First the 0.48-THz RF signal is down-converted by the bottom quad driven with a 240-GHz LO signal to an IF around 240 GHz. In a second step the IF output of the first quad is further down-converted to the desired IF around dc by the second quad which is also driven with a 240-GHz LO signal.

In Fig. 5a, a single stage 240-GHz amplifier is illustrated. The amplifier uses a differential dual-stacked common base topology for improved gain. Input matching is accomplished using TL_1 with 30 µm, a series 15-fF capacitor and TL_2 with 36 µm. To ensure stability from dc to well above the operating frequency, MOMCAPs of 50 fF are placed at each of the

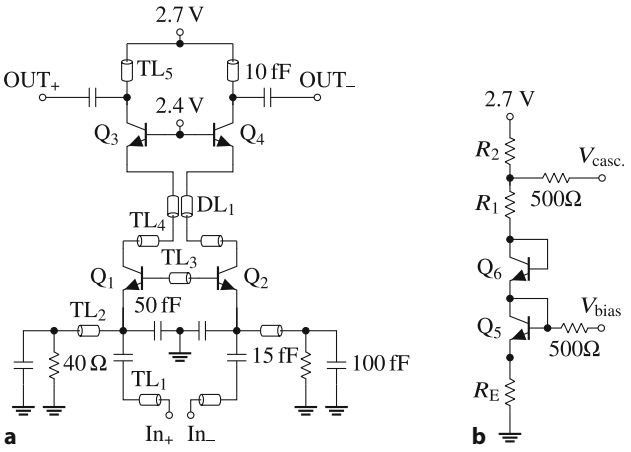


Fig. 5 Schematic diagram of **a** 240-GHz amplifier and **b** biasing circuitry for all circuit stages. Single-ended transmission lines have an impedance of 72.5 Ω and the differential transmission lines have an impedance of 100 Ω. Transistors $Q_{1–4}$ have 5.6 µm emitter lengths and transistors $Q_{5–6}$ are sized according to the current mirror ratio

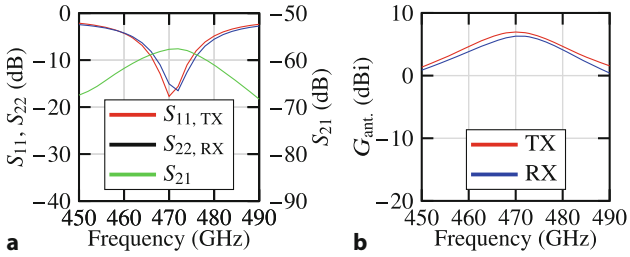


Fig. 6 Simulation of on-chip antenna **a** input matching and antenna coupling versus frequency and **b** realized gain versus frequency

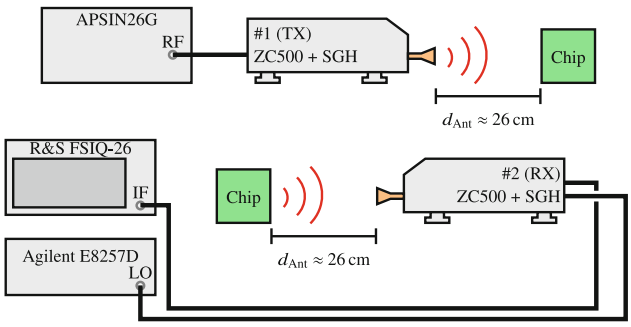


Fig. 7 Measurement setup for over-the-air transmitter and receiver characterization

emitters of the input transistors Q_1 and Q_2. Gain-boosting is introduced at the base of the input transistors Q_1 and Q_2 using TL_3 with 20 µm. TL_4 with 15 µm and the differential line DL_1 with 15 µm further help to boost the gain of the amplifier. Overall, the amplifier shows simulated gain of around 8 dB per stage with typical 3-dB bandwidths less than 20 GHz. For this reason, 3 stages are implemented in the TX path to guarantee a saturated output power of around 3 dBm, considering insertion losses of the 240-GHz branchline coupler and transmission lines and limited output power of the 240-GHz frequency doubler.

The current mirror, depicted in Fig. 5b is directly connected to the input transistors, while the cascode bias voltages are derived from a resistive divider integrated into the same current mirror reference path formed by R_1 and R_2. R_1 and R_2 together set the bias current. Differential circuits have two mirrors to improve layout symmetry. The emitter resistor R_E is sized accordingly for the current mirror factor. A one-to-one current mirror is implemented in Fig. 4 and a one-to-four current mirror is designed in Figs. 3 and 5a.

3 Measurements

The wire-bonded 0.48-THz transceiver is characterized using an over-the-air measurement setup, depicted in Fig. 7. The 26-dBi standard gain horn antennas attached to R&S ZC500 VNA frequency extenders have a distance of 26 cm to the transceiver chip to ensure farfield conditions. The signal input to the transceiver chip is a APSIN26G source. Two R&S ZC500 VNA frequency extenders are used for TX and RX characterization. The first frequency extender is used as a transmitter with its output power characterized by an Erickson PM4 power meter. The first frequency extender is then connected to the second frequency extender that is used as a receiver. In this way, the receiver conversion gain can be determined of the second frequency extender. A APSIN26G is used as the RF-source for the transmitting R&S ZC500 frequency extender. The receiving R&S ZC500 frequency extender is connected to the R&S FSIQ-26 signal analyzer. The LO signal from an Agilent E8257D signal source is connected to the receiving R&S ZC500 frequency extender. The 240-GHz branchline coupler has been characterized and compared to simulations in Fig. 8. A meandered design was implemented to achieve a compact layout. Simulated and measured insertion loss and phase shift are in good agreement at 240 GHz. The measured and simulated normalized antenna gain patterns are given in Fig. 9. Simulation and measurement agree well within 2–3 dB in the RX antenna, although the measured TX antenna E-plane deviates from simulation, perhaps due to a relative phase imbalance in the two quadrature paths prior to the 0.48-THz push–push common collector frequency doublers. A peak system conversion gain (CG) of 7 dB and a NF_{SSB} of 25.2 dB at 0.471 THz have been measured in Fig. 10a. The gain method [17] is used to determine the noise figure as no external noise source could be found at these frequencies. In Fig. 10b an EIRP of −8.8 dBm is measured at 0.47 THz. Using the EIRP measurement and the simulated realized antenna gain results in a calculated output power P_{out} of −15.8 dBm at 0.47 THz. The harmonics separated by 20 GHz are at least 30 dB below the carrier, as illustrated in Fig. 10c when a 20-GHz signal is fed into the transceiver. The phase noise performance

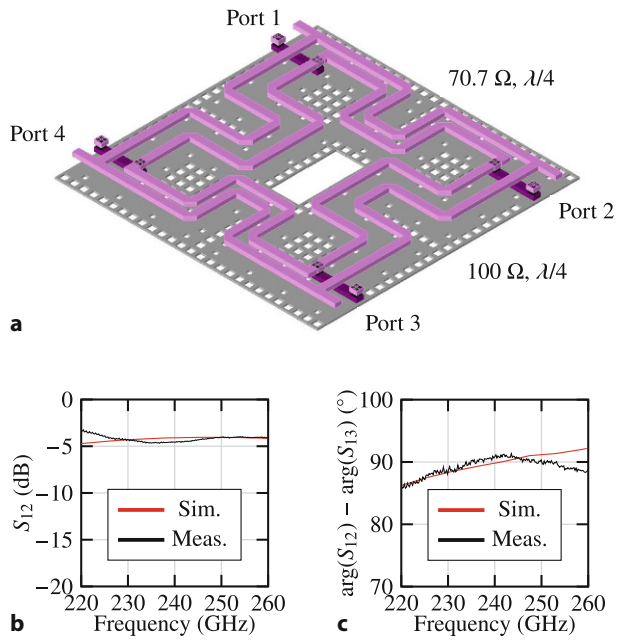


Fig. 8 240-GHz branchline coupler **a** layout implementation, **b** measured and simulated insertion loss and **c** measured and simulated phase shift

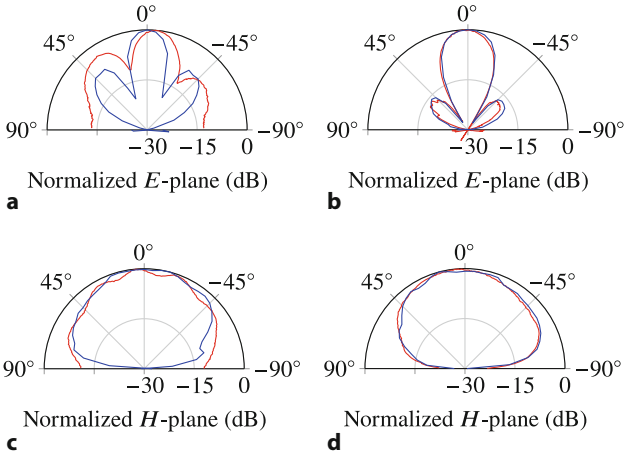


Fig. 9 Measured (*orange* –) and simulated (*blue* –) normalized gain of **a** transmitter antenna E-plane, **b** receiver antenna E-plane, **c** transmitter antenna H-plane and **d** receiver antenna H-plane at $f_{RF} = 0.47$ THz

is considered in a two step process. First, the 20-GHz signal from a APSIN26G source was directly connected to the R&S FSIQ-26. Afterwards, the 20-GHz APSIN26G source was connected to the transceiver. The multiplied transmitted signal was received by the R&S ZC500 frequency extender and downconverted to an IF signal, input to the R&S FSIQ-26. In Fig. 10d the phase noise translation due to a multiplication factor of 24 follows the theoretical 27.6 dB, within a 2-dB range.

Fig. 11a depicts the FMCW radar measurement setup using the demonstrator on-board frequency source and a single 1-cm trihedral reflector target at around 11.5 cm. When considering the ×24 multiplication factor of the transceiver, a 60-GHz RF bandwidth is achieved using a linear frequency sweep at the input LO from 19.3 GHz to 21.8 GHz in 1 ms. More details on the similar demonstrator platform are described in [12, 13]. The achieved range resolution can be estimated from Fig. 11b by examining the distance between the peak and the first null [18]. The peak-to-null distance is 6.5 mm in Fig. 11b. In the measurements, a Hann window is used to improve sidelobe supression at the cost of a 2 times larger peak-to-null width compared to the boxcar window. Therefore a calculated range resolution of 3.25 mm is

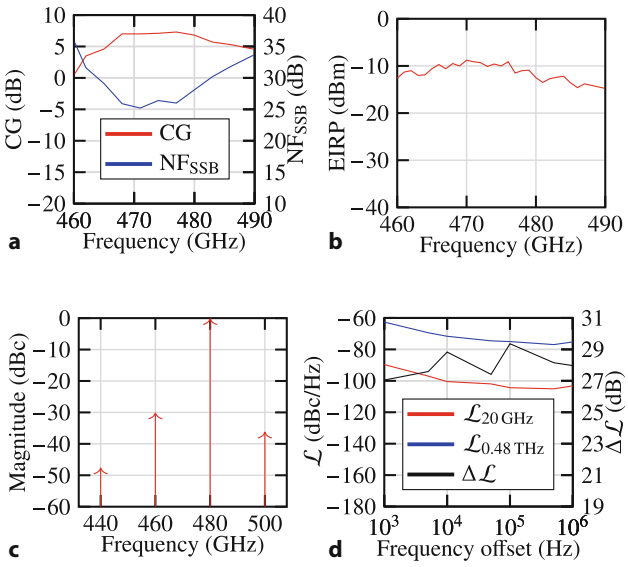


Fig. 10 Measured **a** system receiver gain and noise figure (with 31 dB analog frontend gain) at f_{IF} = 120 kHz using gain method from [17], **b** EIRP, **c** harmonic content with f_{LO} = 20 GHz input signal and **d** phase noise measurement of a APSIN26G source as input signal with f_{LO} = 20 GHz, f_{LO} = 20 GHz multiplied to 0.48 THz and resulting phase noise translation ($\Delta\mathcal{L}$)

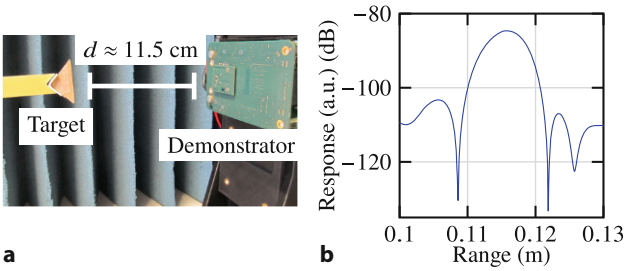


Fig. 11 Illustration of **a** measurement setup with transceiver chip wire-bonded on 2.0 × 2.4 cm^2 interposer PCB and mounted on 5.5 × 8.5 cm^2 demonstrator and **b** FMCW radar measurement with 1-cm corner reflector target at 11.5 cm using the on-board demonstrator frequency source in a linear frequency sweep from 19.3 GHz to 21.8 GHz in 1 ms

Table 1 FMCW Radar Demonstrators Above 0.3 THz in Silicon-Integrated Technologies

Technology	f_T/ f_{max}/ f_{RF} (GHz)	Topology	Chip area (mm^2)	P_{dc} (mW)	NF_{SSB} (dB)	Reference
65-nm CMOS	–/280/220–320	Monostatic, 5-channel comb	5.00	840	28.0	[9]
130-nm SiGe	300/350/311–338	1-TX, 1-RX, 2-chip	1.97	2942	30.3	[10]
130-nm SiGe	230/–/367–382	1-TX, 1-RX, 1-chip	4.18	380	35.0	[11]
90-nm SiGe	300/480/450–490	Monostatic	1.42	280	32.0	[12]
130-nm SiGe	470/650/447.3–491.3	1-TX, 1-RX, 1-chip	1.92	877	–	[19]
90-nm SiGe	**300/480/463.2–523.2**	**1-TX, 1-RX, 1-chip**	**2.84**	**640**	**25.2**	**This**

determined, while the theoretical range resolution is given as

$$\Delta R = \frac{c}{2B_{sw}} = 2.5\,\text{mm} \tag{1}$$

at a 60-GHz sweep bandwidth B_{sw}.

Table 1 details the current state-of-the-art FMCW radar demonstrators above 0.3 THz in silicon-integrated technologies. The 100-GHz bandwidth in [9] comes at the cost of a second fixed 10-GHz LO signal, generated using a laboratory source. The 10-GHz LO signal is used to create the frequency shifts of the five individual 20-GHz bandwidth comb channels. In [10] a two-chip solution demonstrates an increased dc power consumption and a larger system size and cost when compared to a single-chip transceiver. In [19] a quasi-monostatic transceiver is proposed that uses a single-ended TX and a differential RX. A comparable EIRP to this work of around −10 dBm is achieved at 0.46 THz, nevertheless in a SiGe BiCMOS technology with f_T/f_{max} of 470/650 GHz. An on-chip free-running voltage-controlled frequency source is used in the FMCW radar measurements in [11], which results in a highly non-linear frequency ramp. This work is the first demonstration of a fully-differential quasi-monostatic FMCW radar transceiver at 0.48 THz. The transceiver is integrated in a compact credit card-sized demonstrator, using an on-board off-the-shelf frequency source at around 20 GHz. With this work, the operating frequency of silicon-integrated radar transceivers is further extended beyond 0.5 THz. The measured system noise figure compares well with silicon-integrated FMCW radar transceivers above 0.3 THz.

4 Conclusion

A 0.46–0.52-THz fully-differential quasi-monostatic FMCW radar transceiver has been implemented in a 90-nm SiGe BiCMOS technology with an f_T/f_{max} of 300/480 GHz. The transmitter achieves a measured EIRP of −8.8 dBm at 0.47 THz and the receiver demonstrates a measured conversion gain of 7 dB and a measured single-sideband noise figure of 25.2 dB at 0.471 THz. A power amplifier with more than 6 dBm of output power at 300 GHz has been shown in [7] using a SiGe BiCMOS technology with f_T/f_{max} of 470/650 GHz, motivating a further extension of the operating frequency of the radar transceiver to 0.6 THz using the proposed fully-differential subharmonic architecture.

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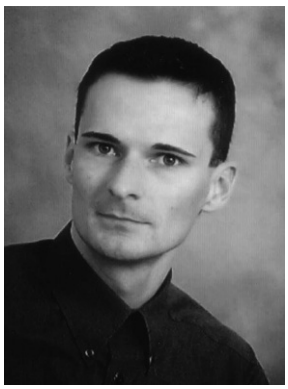

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