Functionality-power-packaging considerations in context aware wearable systems

Conference Paper

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ORIGINAL ARTICLE

Functionality-power-packaging considerations in context aware wearable systems

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Abstract Wearable computing places tighter constraints on architecture design than traditional mobile computing. The architecture is described in terms of miniaturization, power-awareness, global low-power design and suitability for an application. In this article we present a new methodology based on three different system properties. Functionality, power and electronic Packaging metrics are proposed and evaluated to study different trade offs. We analyze the trade offs in different context recognition scenarios. The proof of concept case study is analyzed by studying (a) interaction with household appliances by a wrist worn device (acceleration, light sensors) (b) studying walking behavior with acceleration sensors, (c) computational task and (d) gesture recognition in a wood-workshop using the combination of accelerometer and microphone sensors. After analyzing the case study, we highlight the size aspect by electronic packaging for a given functionality and present the miniaturization trends for 'autonomous sensor button'.

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1 Context aware wearable systems

Wearable computing as defined by [1, 2] envisions personal, mobile computing systems that are always on, useful in all situations and most of all, easy to use. Thus whereas a conventional mobile device would only be used for an occasional schedule check or address lookup, a wearable device would constantly provide the user with useful information such as nearby shops and special offers, transport delays, or health and lifestyle-related reminders (taking medicine, diet etc). Such systems are particularly important in professional applications such as emergency response units, manufacturing and maintenance. Thus a wearable system might constantly provide a fireman with hints and warning about hazards related to his environment, his physiological state and his current actions.

A key component of the wearable computing vision is the ability of the system to model and recognize user activity and the situation around him. This so called context awareness [3] allows the system to proactively provide the user with the right information at the right time, reduces the complexity of the user interface, and allows new modes of information recording. One of the most popular approaches to context awareness in a mobile environment is based on simple on-body sensors. Thus an accelerometer, light sensor and a microphone placed on the wrist could be used to track interaction with household appliances [4] or the use of tools [5]. In a similar way an accelerometer and/or gyroscope on the upper leg can differentiate between level walking, going upstairs, going downstairs and running.

1.1 Basis architecture

Overall, a context aware wearable system consists of a number of interconnected modules placed at different body locations. Each module consists of sensors, analog to digital converter (ADC), computing elements, radio frequency (RF) circuitry and hybrid power supplies (batteries and energy scavenging generator) (see Fig. 1). When designing such systems one has to take into account not only the usual computer performance measures but also the optimization criteria resulting from the fact that the system is placed on the human body. These criteria are often referred to as 'Wearability'. They include among other properties such as form, weight, flexibility, heat generation and esthetic considerations. In technical terms the two main challenges for achieving good wearability are overall system size and power consumption.

Miniaturization can be achieved by designing smaller individual components and integrating them as one functional unit with suitable electronic packaging technologies. Power consumption can be minimized by duty cycling, reducing the active energy per operation, selecting low-power features, classifiers and implementing power-aware algorithms on the processor. At the same time, the performance of the wearable system should not be affected and should offer high suitability for different tasks. Here a trade off is faced by designers between suitability for a given context task, recognition performance, electronic packaging by miniaturization and power consumption. Commercial microcontrollers and processors are flexible enough due to their versatile instruction sets that allow the implementation of different wearable tasks. Dedicated processors (ASICs) on the other hand execute the given task faster, require less silicon area and consume lower power than general-purpose architectures. However, they lack the suitability for a wide range of applications. If the wearable scenario changes, a re-design of the ASIC is required. Reconfigurable devices combine the flexibility of general processors and the performance of ASICs, but they do not meet the strict demands of power consumption.

1.2 Paper scope

As sketched above, the design of a wearable system can be viewed as a multi dimensional problem with conflicting optimization criteria. This paper is dedicated to formalizing the trade offs involved in solving this problem. In doing so we focus on an individual module as shown by Fig. 1. We propose to describe such a module by three parameters that represent different properties. 'Functionality' defined as a combination of suitability for a context-task and required recognition performance with a given set of features and classifiers, 'Electronic Packaging'(routing area, volume, size) and 'Normalized Energy/Power consumption' parameters are proposed.

Clearly reducing a complex design tradeoff to a three parameters metric is a gross simplification that will not provide an exact and generally valid characterization of the system. Instead the parameters are intended as 'figures of merit' that give a rough estimation of where in the design space a particular system is situated. Such figures of merit are useful to enable a system designer to quickly judge the effect of certain design choices on the system.

The paper motivates and postulates formulas for computing the three parameters and evaluates their usefulness as a design tool on practical system examples implemented at the 'ETH Wearable Computing Lab'. In particular we present various trade offs of the 'autonomous sensor button' with the proposed metrics. The results show that the proposed figures of merit are useful in selecting an optimal system for solving a given context recognition task.

2 Related work and paper contribution

Our group pursues the vision of autonomous sensor nodes, seamlessly integrated into the user's outfit, to

Fig. 1 Proposed wearable system architecture
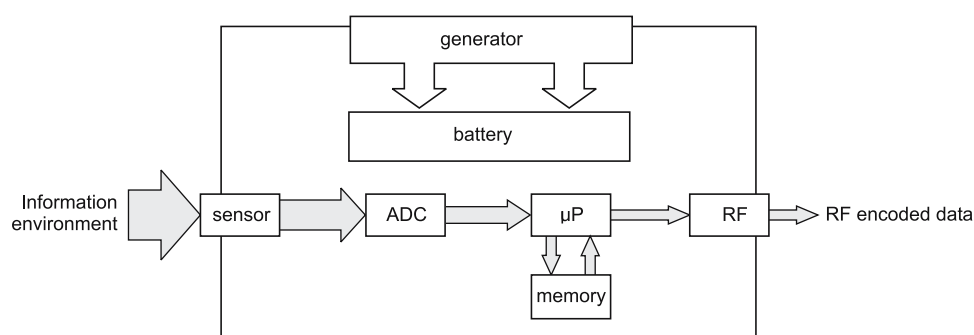
recognize activities and context in daily life situations. This vision implies that the wearable sensor nodes should be extremely small and consume so little power that no power source change is required for several months to years. Working towards this vision, the previous work of our group dealt with issues such as, activity recognition using low-power features and classifier algorithms [4, 6], optimization of power and size in a multi-sensor context recognition platform [7], development of hybrid micro power supply to achieve autonomous behavior [8], electronic packaging aspects of an ultra-miniaturized wearable sensor button, reliability modeling of embedded systems in wearable computing [9, 10], detailed systematic approach considering wearability and power consumption [11] and methodologies for context-aware system design were proposed [12] for selecting optimized architectures with respect to power consumption. The main aspect which sets us aside from the work done by other groups in the field of personal and ubiquitous systems is the focus on *context aware wearable systems*. System-level design approaches specific to power-performance optimization, speech processing in wearable computing, trading of prediction accuracy versus power consumption was proposed by the group of Smailagic etal. [13, 14]. Additionally systematic design approaches in wearable computing were also investigated by them [15, 16]. Here, wearable systems do not necessarily include sensors and are not evaluated in activity context recognition tasks. They also do not deal with the aspect of miniaturization with electronic packaging and evaluating the functionality. Developing new electronic packaging technologies such as SiP (System-in-Package) for achieving the goals of miniaturization, long-term performance and reducing the production costs have been the interest of several packaging research groups with more emphasis on technology. They did not focus on wearable systems and an evaluation of different context recognition applications [17, 18].

In this paper, we present a metric that characterizes a context sensitive wearable module by three parameters. These parameters sum up the functionality, power consumption and electronic packaging issues. The metric is meant as a tool to facilitate quick evaluation of the effect of different design choices on the suitability of the system for different application areas. To the best of our knowledge this paper provides the following novelties.

- Proposing metrics that summarizes key design choices of a context sensitive wearable system in three parameters.

- Evaluation of the metrics on practical design examples.
- Detailed description of a specific design example: the autonomous sensor button including in depth miniaturization design studies of heterogeneous integration.

In Sect. 3, we propose the metrics and introduce different categories of activity recognition tasks. In Sect. 4 we present different wearable systems and explain the hardware. Section 5 consists of a case study where the metrics are applied to analyze the trade offs of the system in different activity recognition tasks. In Sect. 6 we present the miniaturization aspects of 'autonomous sensor button' for a given functionality. Finally we state our conclusions and proposed work for the future.

3 Proposed metrics-methodology

3.1 Proposed metrics

As stated in the introduction we aim to provide a simple figure of merit like metrics to help the system designer judge the suitability of different systems for different types of tasks. We base this metrics on three parameters: an abstract functionality, an electronic packaging metrics, and normalized energy consumption. As figures of merit the definitions of these three parameters presented below are not to be take as any formally provable laws. Instead they have been defined based on our experience with several generations of context sensitive wearable system to best reflect different design choices. The usefulness of the definitions is demonstrated on a set of examples later in the paper.

*(a₁)***Functionality (scenario)** The performance of a context sensitive wearable module in a given scenario is essentially the quality of context recognition. However, plain recognition accuracy is not a sufficient parameter since it does not reflect the hardness of a particular recognition task. Neither does it reflect the accuracy requirements of the task.

We thus propose to use relative recognition performance (R.R.P) as described below. Isolated actions or continuous activities can be recognized by using features from single or multiple sensors together with a classifier algorithm. Implementation of the complex features and algorithms is restricted by the available hardware resources, which influences the recognition rate. The proposed metric normalizes the recognition rate of different tasks on a scale of 0.1–1. We define the limits of recognition performance based on the task. A

task is deemed successful if it meets the stipulated 'higher limit or above' and unsuccessful if it does not meet the lower limit with respect to the recognition rates.

- R.R.P = 1 (completion of the task)
- R.R.P = 0.1 (unsuccessful completion of the task)
- R.R.P = W_p (partial completion of the task) where W_p = weights assigned

$$W_p = \frac{R_s - R_{low}}{R_{high} - R_{low}} * x \tag{1}$$

R_s recognition rate achieved during the task
R_{low} lower limit of Recognition rate (scenario specific)
R_{high} upper limit of Recognition rate (scenario specific)
x 0.9 (for the R.R.P scale (1.0 – 0.1 = 0.9)).

This metric serves as a performance-measure of a system for solving a context recognition task considering the effect of features and classifier algorithms. Also the task can be a computational job such as calculation of a feature or set of features towards application in context recognition. It can be called Relative Task Solvability (R.T.S). R.T.S can only be rated as either 1.0 or 0.0 for successful and unsuccessful completion.

*(a₂)***Functionality(node)** Functionality(node) is defined as the suitability of a node for solving different tasks. With respect to the processor contained on a node we propose to use the internal memory size, the operating frequency and diversity of the instruction set as key parameters. Thus our metric is specified by the device/processor maximum operating frequency (f_{max}), program and on-chip memory (M_{p+c}) and number of core instructions 'I', normalized on a logarithmic scale. The last parameter might seem strange. Indeed, in a high performance general purpose processor, a higher number of instructions is not correlated with a higher overall performance. However in small, embedded devices additional instructions are often signal processing and other special purpose operations that indeed significantly increase the capability of the device. Moreover devices at the lowest end of the embedded spectrum tend to have smaller instruction sets, as they have to use as little area as possible to meet stringent pricing targets.

Often ASIC (Application-Specific-Integrated-Circuits) and FPGA (Field Programmable Gate Arrays) are custom designed for a specific application and do not rely on the instruction set. Since ASIC's are de-

signed for custom specific applications, the suitability for different tasks is taken as '0' having the lowest flexibility. With the proposed metric, different families of processors used in context recognition tasks are evaluated as shown in Table 1. The calculated values prove that this metric holds true for a wide range of processor families.

In order to compare the microcontrollers and DSP's with the same core architecture this metric is useful. However, it is important to realize that ASIC's could be regarded as devices with lowest flexibility with best power savings. Commercial micro controllers are regarded to have moderate flexibility. Modern FPGAs offer to combine the suitability of digital signal processors and performance of ASICs to improve the suitability. However, they consume very high-power compared to an ASIC, that is designed to solve the similar application. One such example can be quoted to justify the reason, not to consider them in the current investigation. Mencer et al. [19] compared the implementation of the IDEA cryptography algorithm to compare SA-1000 (RISC), DSP, FPGA and ASIC architectures. Although, it's possible to achieve high performance, they can not achieve power savings compared to an ASIC which is intend to do the same task (Tables 2, 3).

$$F_{node} = \log\left(\frac{f_{max} * M_{p+c} * I}{100 * a * b}\right). \tag{2}$$

f_{max} maximum operating frequency
M_{p+c} (program memory + on-chip memory)
I no. of core instructions
a normalization factor for memory
b normalization factor for frequency.

(b) Electronic packaging metrics The wearable systems should be compact and light. The electronic packaging technology and the scheme by which wearable systems are designed using sensors, a processor and signal conditioning circuitry, dominates the agenda since it directly affects the wearability. Area in the x–y space (area occupied on the human-

Table 1 Suitability Comparison Between Microcontroller, DSP, FPGA and ASIC

Type	Flexibility	Power savings
ASIC	Lowest	Best
FPGA	Moderate	Poor
Microcontrollers (fixed point)	Architecture dependent	Good
DSP	Architecture dependent	Moderate

Table 2 Comparison Between RISC, DSP, FPGA and ASIC [19]

Type	Technology (μm)	Clock (MHz)	Performance (MBit/s)	Power (W)	Efficiency (MBit/J)
RISC SA-110	0.35	200	32.0	1.0	32.0
DSP TMS320C6x	0.25	200	53.1	6.0	8.9
FPGA XC4020XL	0.35	33	528.0	3.2	167.6
ASIC (VINCI)	1.20	25	177.8	1.5	118.7

Table 3 Functionality(node) applied to Processors used in context recognition

Processor	f_{max} (MHz)	M_p (kb)	Inst	Pin count	F_{node}
MSP430F123	8	4	27	32	2.15
MSP430c33x	3.8	24	27	100	3.20
MSP430F1611	8	48	27	64	4.64
PIC18Fx480	10	16	75	44	4.78
PIC18Fx580	10	24	75	44	5.19
μPD78082	5	16	66	44	3.96
μPD78083	5	24	66	44	4.37
SA-1110	251	24	110	256	8.79
x-Scale	400	32	80	544	13.83
AT91M40807	21	128	40	100	6.98
TMS320c55xx	200	24	85	144	8.31

body when placed) and volume of the system represents comfort and miniaturization. Based on the ITRS road map [20], the projections for processor pin-count follows a scale of power 2. In order to compensate for this growth and emphasize the 'packaging effort' within the system ($\sqrt{(\text{Pin}_{\text{proc}})} * \text{vol.}$) with usage of a logarithmic scale is imperative. For a wearable system, using a processor with a higher pin-count does not affect it's wearability but the packaging effort does ('effort in system-integration'). We thus propose the following metric:

$$Pkg_a = \log\left[\frac{\text{Wear}_{\text{Area.}} * \sqrt{(\text{Pin}_{\text{proc}})}}{1\text{mm}^2 * 1,000}\right]. \tag{3}$$

$$Pkg_b = log\left[\frac{\text{Wear}_{\text{Vol.}} * \sqrt{(\text{Pin}_{\text{proc}})}}{1mm^3 * 1,000}\right]. \tag{4}$$

$$Pkg_c = \log[R_a]. \tag{5}$$

Wear$_{\text{Area}}$ area of the wearable system after packaging in mm^2

Wear$_{\text{Vol.}}$ volume of the wearable system after packaging in mm^3

Pin$_{\text{proc}}$ number of pins of the processor

R_a routing area with a given substrate.

As shown in Fig. 1 the wearable system consists of analog circuitry, RF unit, digital processor and power supply units. This calls for 'Hetero System Integration' concepts. ITRS road map [20] projects that SiP solutions are more suitable for hetero system integration compared to the traditional System-On-Chip (SOC) solutions. This is attributed to shorter cycle times to market, lower cost, risk assessment and a high degree of modularity compared to SOC solutions. This trade off is shown in the Fig. 2. For high volume memory applications or applications dominated by digital logic, SOC remains to be the key driver and for multi-sensor context recognition systems SiP is apt. But the complexity in the SiP solution grows with introducing MEMS devices and power supply as a part of the package. The cost of system using SOC technique with MEMS sensors and CMOS RF unit becomes much higher. The addition of different modules to the 'logic' by SOC for systems that are used in the current investigation is shown in Table 4. Addition of chemical sensors and electro optical systems will further increase the cost.

Within SiP designs, different options are available for hand held and wearable computing systems which require higher degree of miniaturization. They are 'stacked dies and modules' (where different chips, modules are stacked to achieve higher integration), 'folded systems' (all components are crammed in a folded flex and bent to certain degree in order to achieve the required form factor) and 'moulded devices'. Selecting the suitable physical design parameters from the Table 5 for SiP design results in reduced size and volume.
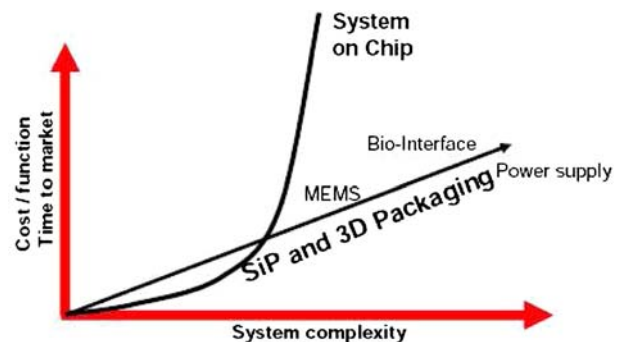

Fig. 2 Packaging technologies trade offs

Table 4 Cost of adding technology in units of mask levels [20]

Cost of adding (mask)	Logic	SRAM	Flash	DRAM	CMOS RF	MEMS
Logic	0					
SRAM	1–2	0				
Flash	4	3–4	0			
DRAM	4–5	3–4	7–9	0		
CMOS RF	3–5	5–9	6–9	6–10	0	
MEMS	2–10	3–12	6–14	6–15	5–15	0

(c) Normalized power or energy consumption The active power or energy consumption of a processor is defined as the energy/power consumed in performing a number of classifications (N) in a time 't' to solve a context recognition task. The energy/power values of the processor are measured and normalized to a logarithmic scale. The proposed power-consumption metric serves to represent a wide range of power values (from a few micro watts to several watts), which would not be feasible with linear representation. The normalized power consumption P_{norm} of the processor is defined as

$$P_{norm} = \log\left(\frac{P_{proc}}{1\,m\,W}\right) (or)$$
$$P_{overall} = \log\left(\frac{P_{sen} + P_{adc+processor} + P_{RF}}{1\,m\,W}\right) \quad (6)$$

If a scenario requires continuous monitoring of the activities, the overall continuous power consumption needs to be evaluated. It consists of the power consumption of the sensors, ADC, processor and the power consumption of the RF unit.

The number of classifications per second depends on the architecture of the processor, the complexity of the algorithm and the task to be recognized. In order to compare different architectures, the active classification energy for performing 'N' classifications in time 't' can also be used as a metric .

$$E_N = \log\left(\frac{E_{proc}}{1\,m\,J}\right) \text{ or } T_N = \log\left(\frac{T_{ex}}{1ms}\right). \quad (7)$$

E_N normalized classification energy consumption
E_{proc} energy consumption of the processor in mJ.

If the task is a computational job such as calculating a particular set of features or a single feature, then the execution time T_{ex} normalized on a logarithmic scale can be considered as a suitable metric (T_N). If the wearable system is employed with the duty cycling, in that case logarithmic value of the number of operating hours during a classification with a rechargeable battery represents the power metric.

$$P_{duty} = \log(\text{operating hours}) \quad (8)$$

All these metrics, costs of functionality, power and packaging can be calculated in a combined form for a given architecture. It will also be shown that, these metrics help in selecting optimal wearable architecture.

3.2 Tasks

A task is defined as the recognition of a single or set of activities in a wearable computing scenario, using information from sensors. We propose to divide context recognition tasks into three categories (Table 5) based on the computational complexity (No. of instructions per second) and minimum memory size (M_{min}). It is assumed that we have a priori knowledge about what sensors are required in each activity. The features and the classifier algorithms are known [4, 6]. They range from simple daily-life activities detection using 'mean' feature with a C 4.5 decision tree classifier algorithm to solving a complex health monitoring task using Hidden Markov Models (HMM). For low level tasks the features are simple time domain features such as 'mean','maximum', 'minimum' and 'slope' with a C

Table 5 Technology trade offs with in System-in-a-Package [21]

Parameters in SiP	Integration ability	Stacked die	Stacked modules	Folded flex	Moulded devices
Redistribution capability	Vertical	–	–	High	Medium
	Lateral	Low	High	High	Medium
Integration of passives	Discrete	Low	High	High	High
	Embedded	Low	High	Medium	Medium
Wire length	WL	High	Low	High	Medium
No. of layers	l	≤5	7	10	32
Layer thickness(G+C)	Gap G (μm)	Negligible	100–1,200	200–1,200	50–600
	Carrier C(μm)	200–600	50–1,200	20–100	50–200
VIC density	1/mm² mm	0.5	0.5–12	5–30	10–50

4.5 decision tree classifier algorithm. For medium level tasks, a combination of time and frequency domain features ('peak count' 'FFT', 'roll-off-point', 'center of gravity', 'band width' etc.) or time domain features ('variance' and 'fluctuation' which requires a multiplication or division operation) with classifier algorithms such as K-nearest neighbor and Naive Bayes are used. High-level tasks deal with much more complex algorithms such as Hidden Markov Models and wearable vision algorithms (Table 6).

- *std* standard deviation, *rpt* roll off point, *fluc* fluctuation
- *cg* center of gravity, *mcr* mean crossing rate, *LDA* linear discriminant analysis, *FFT* fast Fourier transformation.

4 Wearable systems architecture

In order to evaluate the proposed metrics, we have implemented the following wearable systems (Table 7).

The systems A and B consists of accelerometers (ADXL311 from Analog Devices), microphone (SPO103 from Knowles Acoustics) and visible light sensor (SFH3410 from Osram Semiconductors) together with MSP430 family processors and an nRF 2401 transceiver from Nordic Semiconductors. In 'A' (WSpack 1.0) an external ADC, 12 bit and 8 channel AD7888 from Analog Devices is used, where as 'MSP430F1611' already includes a 12-bit AD converter. The clock for the microcontroller is generated by an internal digital controlled oscillator (DCO). The DCO is stabilized by an external 32 kHz quartz crystal. The data from the microcontrollers is forwarded to an nRF2401 transceiver for wireless transmission. They are powered by a small lithium-polymer battery (VPP402025 from Varta) which has a capacity of 150 mAh. The entire systems are fabricated on a 4 layer FR-4 substrate. 'A' has overall size of 27×32 mm^2 with a thickness of 9 mm, where as B has

Table 7 Practical design examples

System	Processor
A. WSpack 1.0 [4]	MSP430F123 (Texas instruments)
B. WSPack 2.0 [7]	MSP430F1611 (Texas instruments)
C. Autonomous sensor button	MSP430F1611(Texas instruments)
D. ARC chip [25]	ASIC (0.25 μm UMC L250 technology)
E. QBIC [26]	XScale (Intel)

a size of 41.5×27.5 mm^2 with a thickness of 9 mm due to slightly bigger microcontroller. A detailed hardware explanation for A, B is given in [4, 7]

System C consists of a 3-axis accelerometer from ST Micro. (LIS3L02AQ3) and similar components of microphone and light sensors as in A and B. System 'C' additionally includes a hybrid power supply (a DC–DC converter with solar cell). The entire system is divided into three modules. The sensors and the RF transceiver are on the top module, the microcontroller with power supply unit as second module which in turn is connected to a third module, a solar cell unit. The system has a radius between of 17 mm and thickness of 11 mm with two 1 mm holes for sewing it to the clothing.

We also have implemented an ASIC (0.25 μm UMC L250) for detecting walking behavior [25]. It can process the input data from accelerometers, pressure sensors and a GPS sensor. The chip is designed to calculate, 'mean', 'variance', 'maximum', 'high-band', 'low-band', 'slope', 'entropy' features together with FFT (64, 128, 256 pt) besides an option to by pass certain features. The K-Nearest Neighbor algorithm is implemented in the chip to detect walking behavior. The activity recognition chip is used for simple-walking behavior (idle, walking straight, walking up/down) using only acceleration data and detailed level-walking (elevator up, down) using the additional data from the pressure sensor. The entire area occupied by the chip is 2.435 mm $\times 2.435$ mm with a core area of 3.204 mm^2. The chip is designed to have a maximum operating frequency of 8 MHz. The supply voltage to the core is 2.5 V and the I/O: max is 3.3 V. The final system that

Table 6 Categories of tasks based on the complexity

Task	Category	Features—*Classifier*	Inst./s (MIPS)	M_{min} (*Kb*)
Category I	Household activities[4]	Mean, mcr, max, min.—*C4.5*	<1	<2
Category II	Walking [22, 23] Kitchenette [6] Workshop [5]	Mean, std, fluc variance, cg, rpt, LDA FFT—*K-NN, Bayes*	≥1 and ≤10	≥2 and ≤100
Category III	Eating habits sign language [24]	—*HMM, vision algorithms*	>10	>100

we have considered in the study is the QBIC, this consists of an XScale processor from the 'Intel' family. The QBIC has a belt form factor and can be used for field trials. The friendly user-interface allows different sensors to be connected without major modifications in the design (Figs. 3, 4).

5 Case study: discussion

The proposed metrics are evaluated in three tasks with the systems introduced in Sect. 4. In Task A, 'walking behavior', three activities are required to be detected using accelerometers. For the activities 'Idle', 'walking', and 'walking up/down' using the features shown in Table 4, it is possible to achieve recognition rates of around 90% [22, 23]. For the Task B, 'office-worker' activities such as ' sitting at the desk', 'typing on the keyboard', 'moving the mouse', 'taking a nap', 'lifting a cup and drinking from it' are to be recognized. Simple feature with a C 4.5 decision tree classifier algorithm is sufficient in this case [27]. In Task C a 32- bit FFT is implemented and tested on the systems to calculate the execution time. Finally in Task D, the recognition of tool use in a wood-workshop or shop floor for maintenance worker is performed by autonomous sensor
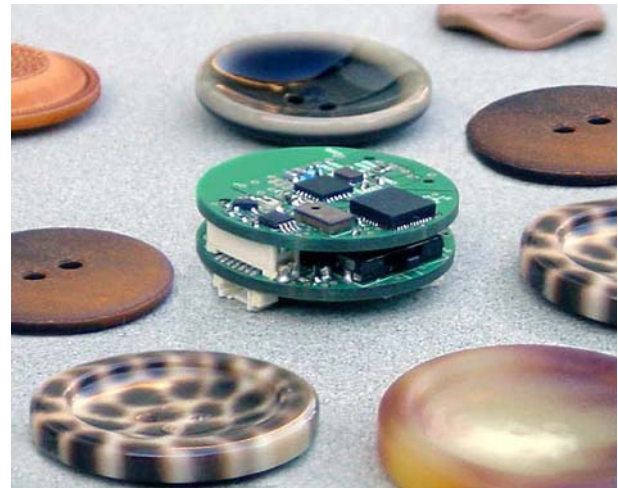

Fig. 4 Autonomous sensor button module

button. In the workshop scenario, accelerometer and a microphone are used to recognize a set of nine activities (drilling, hammering, sawing etc.). Features from the accelerometer data (sampled at 100 Hz), 'mean' and 'peak count' are classified using a Naive Bayes classifier. This classification output is compared against the classifications of the microphone data. This is obtained from a 4.6 KHz sound signal, to which an FFT is

Fig. 3 System architecture of autonomous sensor button
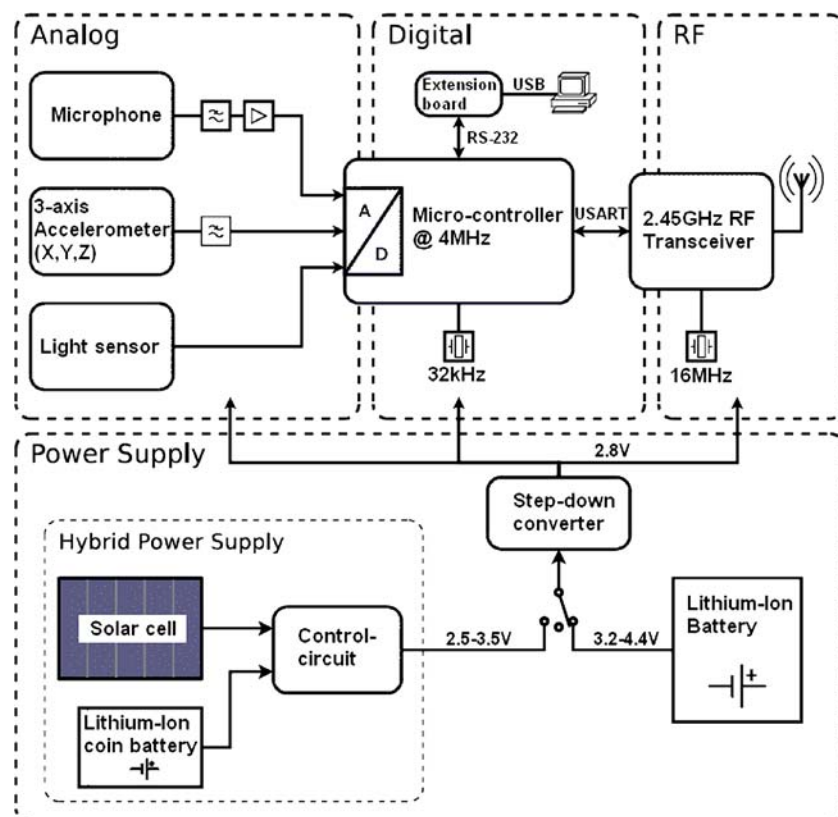
applied, and then reduced using Linear Discriminant Analysis (LDA), classified using minimum distance classification. For the scenario of an office worker, sensor button spends more time in low-power mode and performs classification only during interesting periods. The wood-workshop on the other hand requires active mode for most of the time, and can only go into sleep mode when the worker is taking a break (Figs. 5, 6).

The test results of ARC chip power consumption, using the acceleration test vectors calculating 'mean', 'variance', 'maximum' and fast fourier transform (256 pt FFT) with the K-NN algorithm is shown in Fig. 7. Also the measured active power-consumption results of the MSP430F1611 processor at different supply voltages are shown in Fig. 8. These measurements allow us to estimate the energy consumption values in the current case study.

For task A, the MSP430F123 processor could not complete the recognition task. It does not have a hardware multiplier and due to limited memory, during the distance matrices calculations of the K-NN algorithm with 5-9 neighbors, buffer-overflow problems occur. The 'ARC chip' performed 200 classifications @2 MHz, the behavior with frequency is linear. The XScale processor performed ten classifications/s @400 MHz using 'mean', 'variance' features and running a K-NN classifier algorithm with a data input of 100 samples/s. K-NN requires calculation of eucledian distances to the training vectors in the memory and classifies the activities using sorting. Here a sorting algorithm such as bubble sort would be required, which takes 390 ms at 1 MHz sorting 32 bytes of data (32 vectors) on the MSP430F1611 or similar processors

Fig. 6 Wood-workshop

Fig. 7 Power(asic)

Fig. 5 Office worker
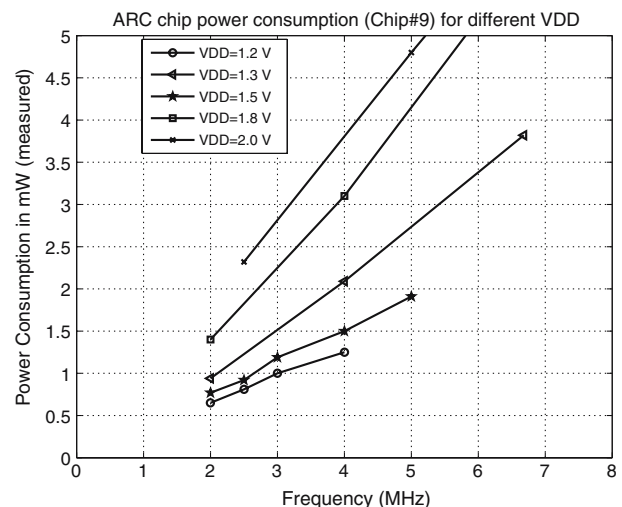
[28]. This can be roughly translated so that sorting 100 feature vectors can take 1.17 s. Therefore at 4 MHz around three classifications are possible. The active energy costs (E_{Na}) of all the systems are calculated to perform ten classifications of task A.

For task B, the expected recognition performance (80–83%) can be achieved by using all the processors. Lower recognition rates for MSP430F123 can be attributed due to it's limited memory size. The calculation of 'mean' feature and classification with decision tree classifier (6–7 decisions) is possible on all the four processors. Using MCR, fluctuation features even higher recognition rates can be achieved. In this scenario a complete redesign of ASIC would be required,
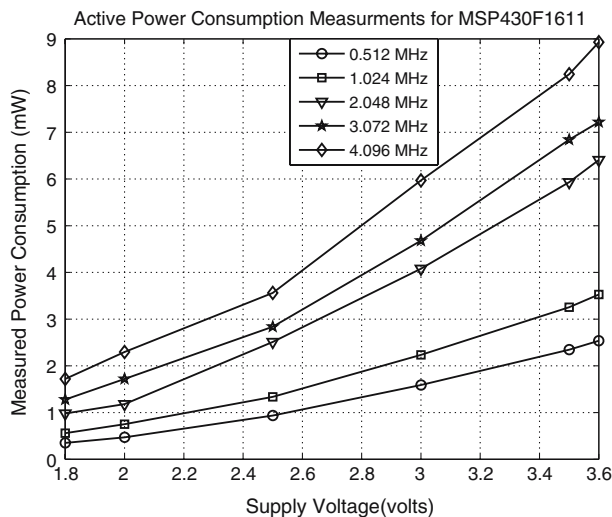
Active Power Consumption Measurments for MSP430F1611

Legend:
- 0.512 MHz
- 1.024 MHz
- 2.048 MHz
- 3.072 MHz
- 4.096 MHz

X-axis: Supply Voltage(volts)
Y-axis: Measured Power Consumption (mW)

Fig. 8 MSP430F1611

hence we have emulated an ASIC, similar to the ARC chip used in the walking behavior task. Using MSP430 processors 3 classifications @1 MHz were achieved. For the ASIC, it would be above 100 classifications @1 MHz, whilst on an XScale processor performing around more than 100 classifications @150 MHz (minimum clock frequency) can be achieved. This can be attributed due to the lower complexity of the decision tree classifier in comparison to a K-NN classifier algorithm [4, 6]. The active energy costs (E_{Nb}) of all the systems are calculated to perform 100 classifications for task B. The measured and calculated metrics for all wearable systems for both tasks are shown in Table 8.

5.1 Trade offs between different systems

From the behavior of the diagrams the ideal system is that which is centralized. For task A, only WSPack1.0 (F123) failed to complete the task but scores the lowest packaging costs. ARC (ASIC) shows best energy costs with respect to other systems but lacks the suitability or functionality(node), whilst QBIC/XScale combination showed best functionality but higher packaging and energy costs. WSPack2.0 has medium functionality and packaging costs. It fails to score above QBIC in

performance and lower energy costs than the ARC chip. Task B has a lower complexity than Task A and all the systems could complete it. The distribution of metrics moves closer to the center in case of WSPack1.0. For this task too, ASIC scored the lowest energy costs. WSPack2.0 scores medium packaging, power, functionality costs. QBIC/XScale, meanwhile has poor performance considering high packaging and power costs but scores best functionality. None of the systems score best performance for all the proposed metrics in both of the tasks. From the case study it can be inferred that all the three metrics dominate each other with different trade offs to have the best centralized distribution. Netcharts tool from Visual Mining, Inc. (http://www.visualmining.com) was used for the representation (Figs. 9, 10, 11).

The functionality(node) is characterized by high memory and operating frequencies. This contradicts achieving lowest energy consumption as well as lower packaging costs (higher pin-count corresponds to higher packaging effort and more area). At the same time, commercial processors which consume lower energy might not achieve better recognition performance or cannot complete the tasks at all. The proposed trade offs between functionality-power-packaging can also be verified by search interfaces such as PISA [29, 30]. This interface uses several search algorithms such as SPEA2, based on the strength pareto evolutionary techniques[31]. Due to the current design space, instead of a complete search algorithm we have applied dominance-non dominance algorithm (for minima) [29]. This approach is useful, to check the dependency of solutions, where automaticly solutions can be identified as shown in solution dependencies in Case (A),(B) and (C). In the case (C) for a 32-bit 64 pt FFT, such behavior can be observed, where XScale processor is faster than its F1611 (both scoring 1), where as F123 fails to complete the task scoring 0.

$$\text{Min.Sol (A)} = \begin{pmatrix} -2.15 & 1.58 & 2.17 & -0.10 \\ 0.0 & 1.86 & -3.21 & -1.00 \\ -13.83 & 4.58 & 6.90 & -1.00 \\ -4.64 & 1.73 & 2.54 & -1.00 \end{pmatrix}$$

Table 8 Evaluated tasks

Evaluated tasks	Sensors	Feat.—Classifier	Recogn.
A. Walking	Accl.—(12-bit, 100 Hz)- above knee	'mean','max','var'—K-NN	≥80%
B. Office-worker	Accl.,light (12-bit, 32 Hz) on the wrist	'mean', 'MCR', ''fluc'' or only 'mean'—C 4.5	≥75%
C. FFT	64,128,256 pt (16, 32-bit)	FFT	1.0 or 0.0
D. Wood-workshop	Accl.,microphone 100 Hz (acc) 4.6 KHz (μ) on the wrist	'mean', 'no. of peaks' FFT, —Naive Bayes LDA	≤70%

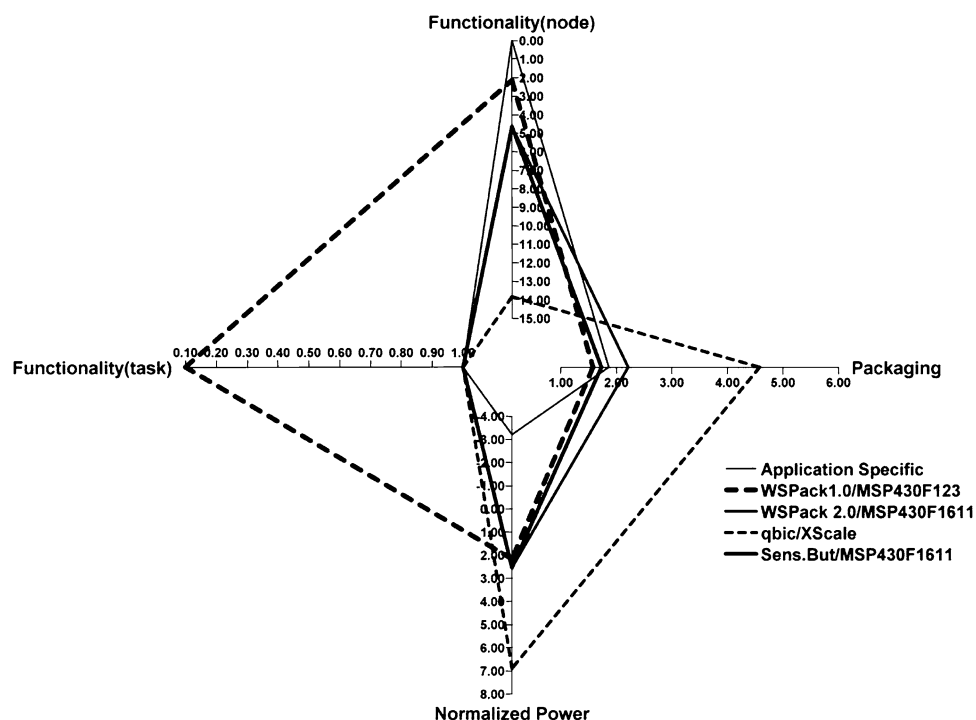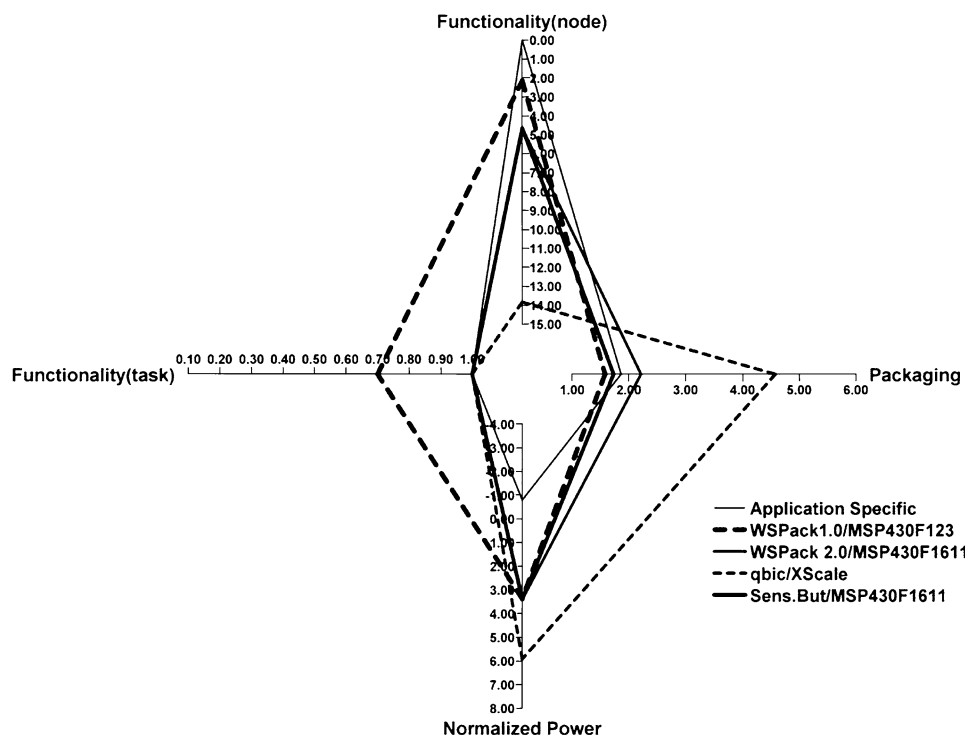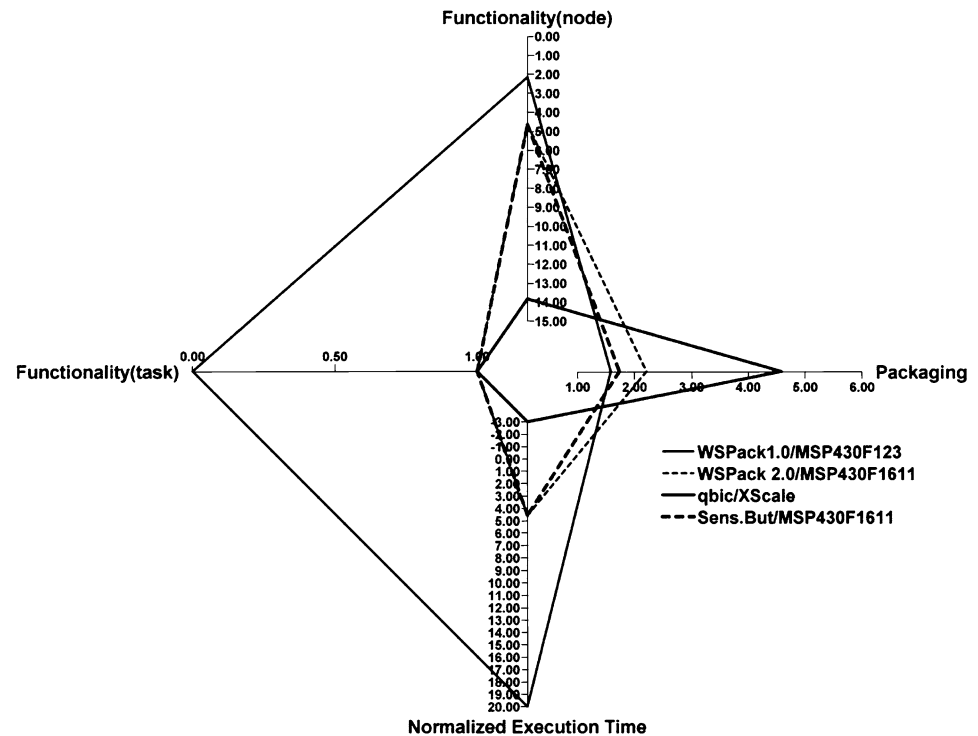**Fig. 9** Functionality-power-packaging trade offs for task A

Fig. 10 Functionality-power-packaging trade offs for task B

$$\text{Min.Sol (B)} = \begin{pmatrix} -2.15 & 1.58 & 3.37 & -0.70 \\ 0.0 & 1.86 & -0.79 & -1.00 \\ -13.83 & 4.58 & 5.92 & -1.00 \\ -4.64 & 1.73 & 3.41 & -1.00 \end{pmatrix}$$

$$\text{Min.Sol (C)} = \begin{pmatrix} -2.15 & +1.58 & \pm\infty & 0 \\ -13.83 & +4.58 & -5.92 & -1 \\ -4.64 & +1.73 & +4.56 & -1 \end{pmatrix}$$

Fig. 11 Functionality-power-packaging trade offs for task C

It can be seen from the results of dominance(non) algorithm, that no solution completely dominates at the same time. It would be feasible to optimize two metrics for a fixed third metric in order to achieve global optima or vice versa. With in the family of systems, between WSPack2.0 and sensor button (using the similar processor and sensors), the sensor button dominates only in terms of electronic packaging metric due to smaller size. Hence the solutions of system B are ruled out in the design space and rest of the solutions output is executed.

6 Trade offs for autonomous sensor button

Functionality-power-packaging metrics for the autonomous sensor button are evaluated to achieve further miniaturization and reduced continuous power consumption. The continuous power consumption of sensor button is evaluated in different scenarios. In office worker scenario (combination of accelerometer and light sensor), kitchen scenario (using a MEMS microphone) and wood-workshop scenario (combination of microphone and accelerometer) are analyzed. The measured continuous power values are reported in Table 9. During the non interesting periods, sensor button goes into a sleep mode. In the sleep mode, two of the three processor clocks (master, subsystem) are shut down and only auxiliary clock is active. This reduces the power consumption to around 20 μW. Two DC–DC converters are evaluated for the suitability with the sensor button. A linear converter (TPS 71501) and a step-down converter (TPS62220) both from Texas Instruments are evaluated for efficiency. In the sleep mode sensor button consumes 21.5 μW with the linear converter where as 27.4 μW with the step-down converter. However, the step-down converter scores higher performance around 96% during the classification mode due to it's modulation scheme. The continuous classification power consumption values are measured for different tasks on sensor button. The following measurements are shown for 128 pt FFT computed for every 54.5 mS for the microphone. The

Table 9 Evaluation of metrics to design examples

System/Processor	Funct$_n$	Pkg$_a$	E_{Na}	Funct$_a$	E_{Nb}	Funct.$_{tb}$
A. WSPack1.0/MSP430F123	2.15	1.58	2.17	0.1	3.37	0.70
B. WSPack2.0/MSP430F1611	4.64	2.21	2.54	1.0	3.41	1.0
C. Sensor button/MSP430F1611	4.64	1.73	2.54	1.0	3.41	1.0
D. ARC/ASIC$_{arc\ A}$	1.97	1.86	-3.21	1.0	-0.79	1.0
E. QBIC/X-Scale	13.83	4.58	6.90	1.0	5.92	1.0

'mean'(approximately for 500 mS) is calculated with nine values (9 × 54.7 = 492.2 mS), 'peak count' calculated over 2.02 s with 37 values (37 × 54.7) are calculated. The accelerometer is sampled at 100 Hz where as the microphone is sampled at 4.68 kHz. A Naive Bayes classifier and linear discriminant analysis are running on the microcontroller to perform the recognition. The overall power consumption, including the wireless transmission for sending the classification result to another node at a distance of 10 m, are measured. By employing the duty cycling in all the scenarios, the operational time is significantly improved as reported in the Fig. 12. Varying the duty cycling of the sensor button, the overall operating time is improved from 42 h upto 300 h calculated with a 150 mAh lithium polymer battery. During the periods of sleep mode, the battery is shut down and the system can be powered by a solar cell (ref: Fig. 3). The solar cell(s) integrated in the clothing connected to the node powers the system. By employing a MPPT (Maximum-Power-Point-Tracking) algorithm, it was possible to achieve 1.25 mW during bright indoors and 7.21 mW during dull outdoors with a 'RWE SCHOTT solar', ASI07/090072JH module. After calculating the power trade offs, we have evaluated packaging trade offs for the sensor button by minimizing the routing area and estimating the possible reduction in the size of the individual components.

6.1 Relevant design parameters for miniaturization

In order to determine the trade offs with electronic packaging, the sensor button architecture is evaluated using different physical design parameters shown in Tables 10, 11. These parameters are from [21, 32] and
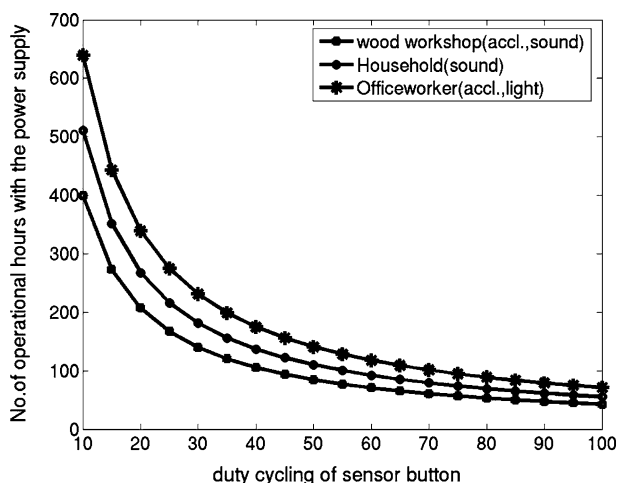
based on the industry review of 2005. The routing area mapped on a logarithmic scale is used to represent the packaging metric. The minimum component size for SiP is expected to be reduced from 600×300 to 200×100 μm² by 2013. For low-cost/hand held devices, number of (#die/SiP) reaches from 6 to 14. In hand helds, the substrate cross section thickness is predicted to be reduced from 50 to 25 μm and blind via dimater will be reduced from 60 to 30 μm. We assume that wearable systems follow similar trends as in hand helds. By applying the proposed design parameters to sensor button architecture, the following trade offs are observed. The functionality of the system during wood-workshop activity is represented. From the calculations, the MCM-C substrate has the best routing area optimization in this case. If the system is designed with less number (≤5), MCM-D thin film provides higher degree of miniaturization. After selecting the MCM-C substrate physical design parameters for minimizing the routing area, power trade off can be observed for the same functionality. Battery operational time is calculated under different duty cycling conditions. The operational time in hours mapped on a logarithmic scale is taken as the power metric. From Figs. 13 and 14 it can be concluded that by selection of suitable packaging technique and duty cycling both miniaturization and autonomous behavior are improved in the selected context task (Table 12).

Fig. 12 Active time trade offs with sensor button

Table 10 Sensor button power consumption during different scenarios

Evaluated scenario (sensors)	Power consumption (mW)	Operating time (h)
A. Wood-workshop (motion, audio)	12.99	42.73
B. Kitchen (audio)	9.96	55.72
C. Office worker (motion, light)	7.78	71.33
D. Sleep mode(step-down converter)	0.0274	20,270
E. Sleep mode (linear converter)	0.0215	25,862

Table 11 Physical design for SiP integration [20, 32]

Substrate (parameter)	MCM-L PCB	MCM-L HDI	MCM-C ceramic	MCM-D thin film
Line width (μm)	125	50–75	75–100	10
Line space (μm)	125	50–75	250	10
Via land (μm)	650	100–225	200	30
No of layers	up to 30	8–10	15–30	2–5
Material	FR-4	FR-4	Alumina	Si, Metal

Fig. 13 Packaging trade off during a selected functionality
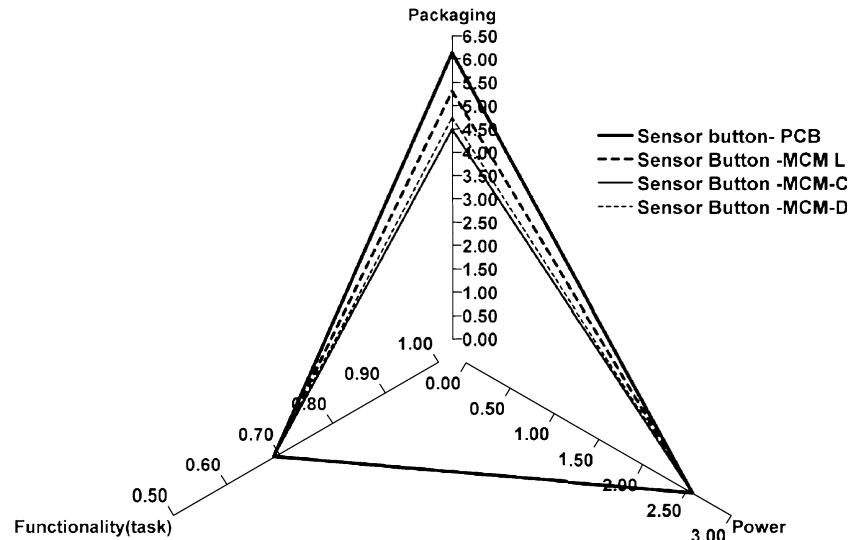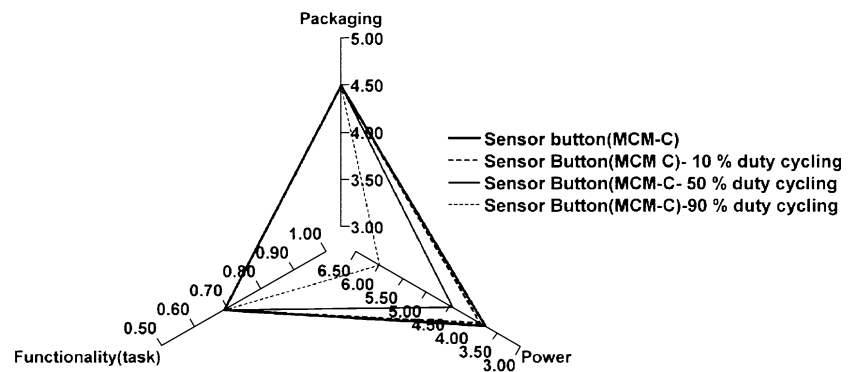

Fig. 14 Operational time trade off for fixed packaging and functionality

6.2 Miniaturization trends in individual components

Miniaturization can also be achieved by reducing the individual size of the components in combination with the physical design parameters of SiP. Hetero system integration combines different components such as silicon IC's, MEMS sensors, RF unit and power conversion and storage devices as one single system. This solution is superior compared to SOC solution due to shorter time cycles for production, lower cost and risk and high modularity. However, CMOS based implementations of SOC continues to provide the lowest

Table 12 Design parameters for different interconnect technologies [32, 33]

Parameter (interconnect)	Wire bond	Flip chip	TAB
Min. pad pitch (Die) (μm)	50	100–120	60
Min. pad pitch (Substr.) (μm)	120	100–120	200
Electrical perform. L (nH)	1–5	0.06–0.2	1–3
Electrical perform. C(pF)	0.2–0.6	0.02–0.03	0.2–0.6

cost per module and highest degree of integration for systems dominated by digital logic. SOC should be viewed as complementary to SiP and hetero system integration. Submodules of a SiP can be packaged as SOC modules and combined to achieve required form factor. The size reduction in individual components is calculated based on the predictions from ITRS, iNEMI road maps and by following the trends of hand held devices [20, 34].

6.2.1 Miniaturization of the digital unit

From the Moore's law and based on the ITRS, iNEMI road maps the following trends are estimated. For every 1.5 years the number of transistors or the functions on the chip (DRAM) is doubling. The increase in the function is achieved by increasing the chip size 1.4 times for every 3 years. In case of DRAM (bits/cm^2) and in case of MPU (no. of transistors/cm^2) are used as measures. The projected trends for the DRAM, MPU can be achieved till 2014 without any implication. At this point due to thinner gate oxide, the leakage cur-

rents will start dominating. Further integration will require longer time periods. In case of DRAM it would be 2.5 years to double the bits/cm^2 and in case of a MPU it would be 3 years. Averaging this for 1 year, it would be possible to achieve 41% increase in the density or only with 59% silicon area (Si$_A$) to achieve a fixed density. This results in 29% of the cost for every year till 2013–2014. The ADC is integrated with the digital unit. Extreme low-power ADC with bare die size in the range of 0.06 mm^2 the size and power consumption of the digital block [35]. There are several trends available to integrate components in the digital block which normally could be cause for source of errors. One such example is replacing quartz crystals. Combining the advances in semiconductor and MEMS process techniques quartz crystals can be replaced using surface micromachined resonators [36] (Fig. 15).

$$A_d = \text{Si}_A * 0.59 + A_{\text{adc}} + \text{Pad}_A * N_{\text{Pad}} \qquad (9)$$

A_d area of the digital unit
Si$_A$ area of digital logic(processor)
A_{adc} area of the analog to digital converter
N_{pad} number of pads for the digital part.

6.2.2 Miniaturization of the RF unit

The scaling for the analog RF front end does not follow the similar trends as in the digital world. Because the component size and antenna are defined by the 'operating radio frequency' and the 'gain' which is fixed by the application. Analog design usually requires large transistors and large passives which increase the RF unit area. Some degree of miniaturization can be achieved by integrating the passive components 'on-chip' with the help of additional thick metal layer. However, reducing the size of RF passive high-Q filters is difficult with the traditional fabrication techniques. For a low data rate application such as sensor button, operated in already crowded '2.45 GHz' frequency band (Bluetooth, ISM Band, 802.11 b etc.) some amount of front-end filtering is required. Operating at higher frequency bands allows to reduce the size of passives and antenna. This comes with a price of increase in gain, which further increases the power consumption. We can expect that the miniaturization of RF unit can be achieved between 10 and 15% annually till 2014.

$$A_{\text{RF}} = \text{RF}_{\text{chip}} + \text{Pad}_A * N_{\text{Pad}} + A_{\text{passives+filter}} \qquad (10)$$

A_{RF} area of the RF unit
RF$_{\text{chip}}$ area of the RF Transceiver chip
$A_{\text{passives+filter}}$ area occupied by the passives and filters.

6.2.3 Miniaturization of MEMS sensors

The miniaturization trend in MEMS devices does not follow Moore's law. The minimum influence of the packaging technology on the performance of the MEMS sensors, in other words 'compliant packaging' is the key for setting the goals of miniaturization. The 3-axis accelerometer (Ref. Fig. 4) can be reduced to the size of 4.84 mm^2 and even further by changing the package without affecting it's usefulness for context recognition. In case of silicon microphones, used in hearing aid applications the maximum miniaturization for a single chip module is $3.6 \times 3.6 \times 1.7$ mm^3 with a

Fig. 15 Predictions based on ITRS road map [20]
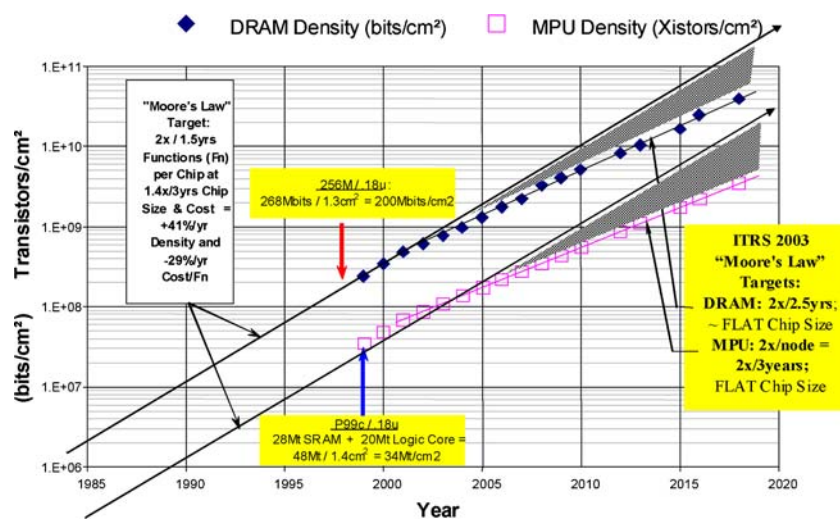
backside volume of 3 mm^3 as quoted by Dehe et al. [37]. For MEMS microphones used in detecting tool sounds a size of 5.50 mm^2 and a bare die size of 1.69–2.0 mm^2 would be feasible. By using chip scale packaging (CSP) and integrating the filters as part of digital unit, area reductions can be achieved. The size limits for MEMS sensors depends on various application specific parameters such as detection range, signal to noise ratio and read out circuity. The higher limit of miniaturization of MEMS sensors can be attributed CMOS readout circuitry size and detection limits. One of the lower end of detection limits are in the range of 12 zF ($z = 10^{-21}$) for a signal which has displacement of 16 fm (averaged over 10 s) [38]. The minimum size of the detection circuit satisfying the resolution and range in the task defines the limit for MEMS sensors.

$$A_{\text{MEMS}} = \text{MEMS}_{\text{chip}} + A_{\text{readout}} + A_{\text{filter}} \qquad (11)$$

A_{MEMS}	area of the MEMS unit
$\text{MEMS}_{\text{chip}}$	area of the MEMS chip
A_{readout}	area of CMOS readout circuitry
A_{filter}	area for filters (if any).

6.2.4 Miniaturization of batteries for personal computing

Lithium polymer batteries are highly suitable for portable, hand held and wearable computing applications. They have the highest energy density among all the commercial rechargeable batteries. Miniaturization of them, below 1 cm^3 leads to reduction in energy density. This happens because the fraction of the battery package is enhanced at the expense of active material. Below 1 mm thickness the energy density is greatly reduced due to the dominant thickness of packaging foil. Some approaches are available to deposit thin film lithium batteries in a package which allows to support self powered wireless micro systems [39]. It is assumed that the miniaturization, packaging and integration of batteries with SiP is lagging by 4–5 years in comparison with the digital world. Inclusion of energy harvesting system such as solar cell together with the micro batteries allows higher degree of autonomous behavior.

6.3 Size trade off for autonomous sensor button

Based on the miniaturisation trends in individual components and the physical design parameters for packaging technologies, the overall size and volume reductions for the sensor button is estimated. The estimated size of the individual components is shown in Tables 13 and 14.

In the Design A, the following scheme is proposed. Three sub system modules are designed with MCM-C packaging technique and stacked together as a sensor button SiP. Solar cells and light sensor on the top module, analog, digital and RF units in the center module and batteries as the bottom module are stacked together to realize Design A. The substrate area for analog, digital parts, RF components including the space for wire bonding is calculated as 54.34 mm^2. This value comes after deducting 1.8 mm^2 (radius of 0.5 mm) area required for the two holes. The available substrate area for the top module is around 51 mm^2, which allows two solar cells of each 20 mm^2 and the light sensor to be wire bonded. The bottom module consists of two lithium polymer batteries of $5 \times 5 \times 0.2$ mm^2 size. After carefully considering the entire scheme including the spacing for an antenna, we believe that it is possible to design the sensor button with 7.48 mm radius having a thickness between 5.1 and 5.4 mm (Fig. 16).

In the design B, modularity is given higher prirority. Two sub system modules are designed and stacked together as sensor button SiP. The sensor and the RF Unit are placed on the top module. The digital unit and two lithium polymer batteries of $2.5 \times 2.5 \times 0.2$ mm^3 size are placed on the bottom module. Solar cells are separated and integrated into the clothing. The substrate area for the top module is calculated around

Table 13 Miniaturization in Li-poly battery [39]

Size (mm^3)	Voltage (V)	Power (mW)	Energy (mWh)
$10 \times 10 \times 10$	4.1–3.0	150–600	150
$10 \times 10 \times 0.2$	4.1–3.0	5–20	3.5

Table 14 Sensor button size reduction by miniaturized components

Component	Size (area) in mm^2 Design A	Size (area) in mm^2 Design B
Micro accelerometer	6.84	4.84
MEMS microphone	5.50	1.69–2.0 (bare die)
Visible light sensor	1.5–2.0	1–1.5
Microprocessor	4.20	1.45
RF unit	15–20	10–11
Additional components	10–15	7–10
Solar cells	40–45	38 (integrated into clothing)
Batteries	45–50	13

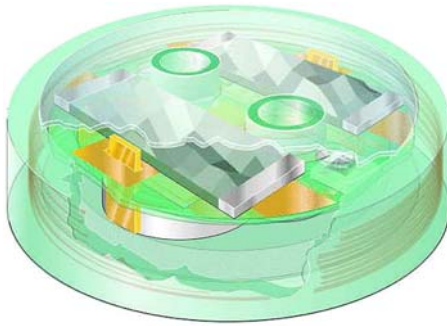**Fig. 16** Miniaturized autonomous sensor button (Design A: 7.48 mm radius ×5.1 mm thick, Design B: 6.16 mm radius ×2.9 mm thick)

36.05 mm^2 and for the bottom module is 30.63 mm^2. Considering the space required for the wire bonding and two holes for the warability, overall size is estimated to be 6.16 mm radius having a thickness range of between 2.9 and 3.3 mm. In comparison to the Design A, Design B provides modularity for the replacement of the sensor module or digital unit with ease. The thickness can be further reduced by using extremely thin stacked die modules [40]. If the system is to be used as data logger (Design C) as per the trends of 2005–2006, size reduction in the range of 6 mm radius having a thickness of 4.2 mm would be possible by choosing similar to that of Design A [9]. The projected performance for design C [9] would allow on-body context by 2014. Implementing heterogeneous integration in combination with self duty cycling sensors, ultra low power ADC, processor, packaged rechargeable batteries combined with low-power design techniques [35] one can expect that by 2013 it would be feasible to integrate self powered sensor button nodes seamlessly into the clothing. Thus it will be feasible to

perform continuous context recognition for several years with on-body nodes without having to replace or recharge the power source.

By applying the packaging metric Pkg$_b$ for a given functionality the influence of volume can be observed in the Fig. 17. Clearly the design B dominates in terms of overall volume and Design C occupies minimal area on the human body providing maximum comfort (Table 15).

7 Conclusions and future work

We have presented a new methodology to study the functionality-power-packaging considerations in wearable systems. From the evaluation of the proposed metrics it was concluded that they assist in designing low-power, miniaturized sensor nodes for different context recognition applications. Also it was shown that, functionality, power and packaging metrics dominate each other with different trade offs in the design space. Medium performance processors are more suitable for solving both low and medium level context tasks showing medium overall costs. However, they cannot be optimized for lowest energy and highest functionality and are not suitable for high level tasks just as low performance microcontrollers are not suitable for medium level tasks. Packaging and power trade offs of sensor button for different functionalities are evaluated. It was shown that by selecting MCM-C packaging technique with suitable duty cycling both size reduction and autonomous behavior are greatly improved (Fig. 18).

The miniaturization design studies show that it would be possible to design self powered sensor but-

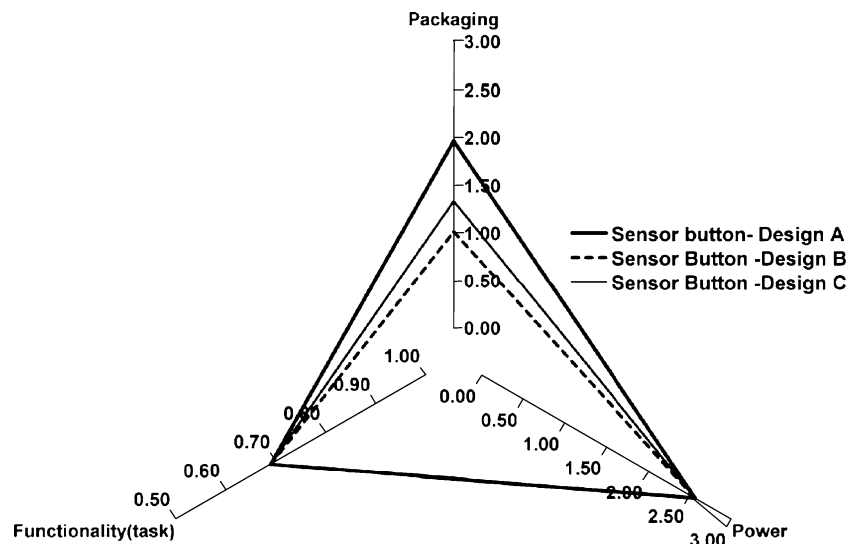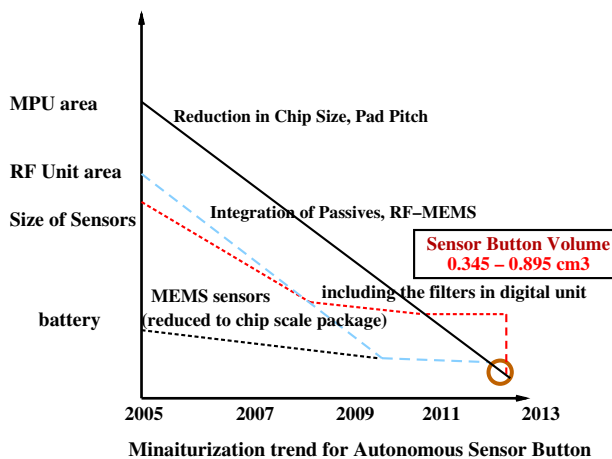**Fig. 17** Packaging trade off with the design study

Table 15 Design study of sensor button: area, volume

Analysis	Area on the body (cm²)	Volume (cm³)	Function
Design A	1.75	0.895	On-body context
Design B	1.19	0.345	On-body context
Design C	1.13	0.474	On-body context

Fig. 18 Miniaturization trend for autonomous sensor button

tons in the size range of 7.48 mm radius with a thickness of 5.1 and 6.16 mm radius with a thickness of 2.9 mm integrated into clothing. In our future work, we are planning to consider even complex scenarios and extend this methodology to a wearable body area network. We would be creating a 3d smax model of sensor button with the housing (ref: Fig. 19) to visualize the assembly and packaging design.
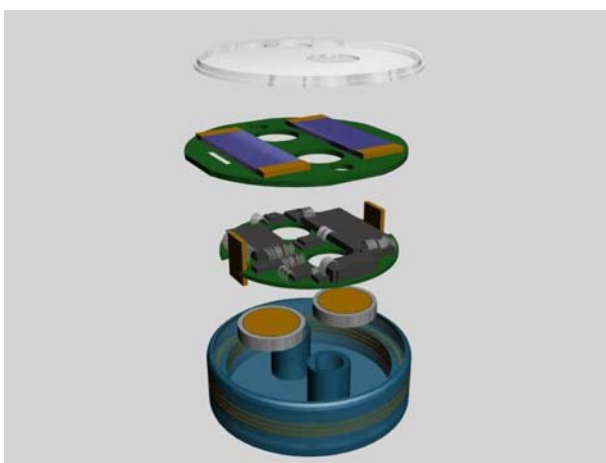
Fig. 19 3D smax model of the sensor button assembly with the housing

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