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Guest Editorial

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Advances in semiconductor technology allow much higher performance levels on a single chip. At the same time, the ever-shrinking device dimensions and voltages have given rise to increased problems of faults and defects. Furthermore, nanotechnology is emerging as an alternative, as lithography-based silicon VLSI technology is expected to hit its limit. However, imperfections in the fabrication process along with on-chip temperature and voltage variations result in yield-reducing defects and faults, whose density and severity grow significantly with the size and density of the chip. Therefore, a new paradigm for the development and use of defect and fault tolerant techniques at the design phase is required to complement existing efforts at the manufacturing phase. Novel techniques to address the emerging challenges and issues in the new VLSI technology era are introduced in this special issue, containing nine selected papers, whose preliminary versions were presented at the 22nd IEEE Defect and Fault Tolerance Symposium in 2007.

The nine papers of this special issue are classified into three categories, which are emerging technology, testability/test vector, and modeling.

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The emerging technology category opens with a paper by M. Fukushi et al. that proposes and evaluates an efficient defect isolation framework motivated by the need to achieve scalability for extremely large scale DNA self-assembled networks. The second paper by M. Hashempour et al. investigates the characterization of the intentionally induced puncture on an erroneous DNA tile site in the grown DNA crystal as part of a healing process. The third paper, presented by X. Ma et al., investigates QCA (Quantum-Dot Cellular Automata) for testable implementations of reversible logic in array systems. The method makes fault masking possible in the presence of multiple faults. The last paper, by F. Karim et al., deals with the effects of random shift clocks and presents a model to evaluate errors in QCA.

There are three papers related to testability and test vector issues. The first paper, by W. K. Al-Assadi and S. Kakarla proposes new DFT techniques for Asynchronous NULL Convention Logic (NCL) to enhance the controllability and observability with acceptable gate overhead using an existing commercial DFT tool. The second paper by M. Favalli and M. Dalpasso analyzes the problem of bridging fault detection in the presence of parameter fluctuation and proposes a method to find the minimal set of test vectors to tackle bridge faults at low frequency. The last paper in this category is by K. Namba et al. They present a non-intrusive test compression algorithm for IP core testing using reconfigurable networks, fixing–flipping coding, and fixing–shifting–flipping coding.

Finally, there are two papers in the modeling category. The first paper by M. Valderas et al. presents a quantized delay model to capture delays of a circuit under test in an FPGA. This new approach builds an FPGA based Single Event Transient (SET) emulator. The last paper in this category is authored by R. Ghaida and P. Zarkesh-Ha. They

propose and test a layout sensitivity model to estimate electro-migration vulnerable narrow interconnects, focusing on a stochastic method of critical area analysis that consists of the modeling of the layout sensitivity to defects, defined as the ratio of critical areas to the overall layout area.

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Cristiana Bolchini graduated from Politecnico di Milano with a degree in Electronic Engineering in 1993, where she received a Ph.D. in Automation and Computer Science Engineering in 1997. Since Dec. 2003 she is an Associate Professor at the Dipartimento di Elettronica e Informazione of the same institution. She has published about 80 papers on refereed international journals and conference proceedings related to the design of digital systems with fault detection and tolerance properties. Dr. Bolchini participates to the Technical Program Committee of conferences and symposia in the area of test and fault tolerance for digital systems and is a reviewer for journals and transactions in this same area, and she is an Associate Editor of the IEEE Transactions on Computers. Her research activity within the design of digital systems is devoted mainly to methodologies for the design of embedded systems, with the aim of providing the capability to cope with the occurrence of hardware failures during the normal life of the device. Furthermore, Cristiana Bolchini also carries out a research activity on issues related to data management for context-aware, mobile systems, with the aim to define methodology and tools for selecting, "tailoring" and integrating heterogeneous and transient data sources, according to the user's context.

Prof. Yong-Bin Kim received B.S. degree in Electrical Engineering from Sogang University in Seoul, South Korea in 1982, the M.S. degree and Ph.D. both in Computer Engineering from New Jersey Institute of Technology and Colorado State University in 1989 and 1996, respectively. From 1982 to 1987, Dr. Kim was with Electronics and Telecommunications Research Institute (ETRI) in South Korea as a Member of Technical Staff. From 1990 to 1993 he was with Intel Corp. as a Senior Design Engineer, and involved in micro-controller chip design and Intel Pentium Pro microprocessor chip design. From 1993 to 1996 he was with Hewlett Packard Co., Fort Collins, Colorado as a Member of Technical Staff, and involved in HP PA-8000 RISC microprocessor chip design. From 1996 to 1998 he was with Sun Microsystems, Palo Alto, California as an individual technical contributor, and involved in 1.5 GHz Ultra Sparc5 CPU chip design. From 1998 to 2000, he was an assistant professor in the Dept. of Electrical Engineering of University of Utah. He is currently Associate Professor in the Department of Electrical and Computer Engineering at Northeastern University. Prof. Kim has published more than 100 technical papers in VLSI and its related areas and he is holding two US patents. His research focuses on high speed low power Digital and Analog VLSI circuit design and methodology.