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Editorial

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The last *IEEE International High Level Design Validation and Test Workshop* (HLDVT'09) was held in San Francisco, California during November 4–6, 2009. For several years, this workshop has provided a forum for discussing high level design verification and test methods. High level, which refers to register-transfer or behavior, is an excellent abstraction to deal with complexities of system design, verification and test. As is true everywhere else, it is always better to catch bugs and correct errors as early in a product realization process as possible. Higher levels, being closer to the specification, provide that capability.

This issue contains nine papers selected from the program of HLDVT'09. These papers were initially submitted by authors in response to *JETTA*'s special issue call for papers with a submission deadline of September 15, 2009. All papers were reviewed by independent reviewers and revised under the guidance of Prabhat Mishra, who is the Guest Editor for this issue. We thank him for diligently completing the journal's editorial process in a timely manner. His guest editorial in the following pages provides a compact summary of the papers included in this issue.

A previous issue of JETTA on related theme was titled, "High-Level Test Synthesis," and was published in October 1998 (Volume 13). HLVDT is an annual event. HLVDT'10 is scheduled to take place in Anaheim, California during June 10–12, 2010. For details, please visit http://www.hldvt.com/10/.

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