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Editorial

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The first paper in this issue is authored by Falconer, Greenwood, Morgan, Kamisetty, Norman and Ganguly of Intel Corporation, USA. They use a fitness guided evolutionary algorithm to derive data patterns that would produce the most inter-symbol interferences (ISI) in a bus. New patterns are created using random bit crossover and mutation and those with higher ISI are given greater chance to survive. The paper illustrates with an application to a bi-directional bus that provides communication between processor and other memory and video devices on a chipset.

The second paper, authored by Eggersglüß, Fey, Glowatz, Hapke, Schloeffel and Drechsler of University of Bremen, Germany, uses multi-valued logic and Boolean satisfiability (SAT) to generate robust and non-robust path delay tests. For efficiency, gates are structurally classified and treated appropriately by the SAT analysis based upon their signal values in the two-vector test.

The third paper examines the hardware-based soft error detection methods for their false alarm characteristics. An analysis of single transient faults shows that a double sampling checker has a large false error detection rate while an integrate and sample type or a triple sampling type checker can be designed for zero false error. The paper is authored by Reddy and Amrutur of the Indian Institute of Science and Parekhji of Texas Instruments, India.

In the fourth paper, Keren of Bar-Ilan University, Israel discusses a coding scheme for economical error checking. In fact, the new one-to-many code has a built-in error tolerance property. Therefore, many errors do not require any checking action hence simplifying the checker hardware.

The fifth paper is authored by Testa, Lapuyade, Deval and Bégueret of IMS Laboratory, France and Carbonero of STMicroelectronics, France. The authors analyze the test problem for a voltage controlled RF oscillator. They show that peak-to-peak detection may be a better method than other proposed methods such as the measurement of either dc current or a high frequency current signature.

The next paper is authored by Kim and Jone of University of Cincinnati, USA and Wang of SynTest Technologies, USA. An analysis of bridging faults in a synchronizer shows that fault effects depend on the location of the bridge, the bridging resistance value, the input signal type (rising or falling) and the signal arrival time. This work has applications to other circuits with multiple clock domains.

The final contribution of this issue is the article by Tseng and Lee of Yuan Ze University, Taiwan. In general, a coding scheme reduces test data volume at the cost of the hardware required for the decoder. The multi-dimensional run-length codes, proposed in this paper, reduce the decoder hardware, especially as the circuits become larger.

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