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Editorial

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This issue contains articles on mixed-signal test, digital BIST, SOC test, test power and security.

First three papers discuss mixed-signal testing. The first paper is authored by Srinivasan of Texas Instruments, Dallas, and Chatterjee, Cherubal and Variyam of Georgia Institute of Technology, Atlanta, USA. They propose a multi-tone power ratio (MTPR) test for broadband communication devices. They show improved accuracy in a low-cost measurement system by adding multi-tone dither noise to the test signal.

The second paper is authored by Long, Wang, Tian, Huang and Long from the University of Electronic Science and Technology, Chengdu, China. They address the problem of fault diagnosis in linear systems and use a genetic algorithm to find the optimum frequency for testing.

The third paper provides a frequency domain built-in self-test (BIST) solution for analog circuit test. The test input is generated by some digital circuitry, a digital to analog circuit and a filter. The response analysis is performed by first-order sigma-delta modulators and a digital signal processor. The authors of this paper are Barragán, Vázquez and Rueda from the University of Sevilla, Spain.

In the fourth paper, de Souza of Federal University of Paraíba, Brazil, and de Assis and Freire of Federal University of Campina Grande, Brazil, propose a novel test pattern generator synthesis method for digital circuits. They have adopted the Berlekamp-Massey algorithm from the communication theory to synthesize an optimal linear feedback shift register that will produce a predefined set of patterns.

The fifth paper is authored by Berg, Ren, Gaydadjiev and Goossens of Delft University of Technology, The Netherlands, and Marinissen of IMEC, Leuven, Belgium. They propose the reuse of functional interconnects of a system in the implementation of the test access mechanism (TAM). Their test wrapper for an embedded core minimizes the test time for a given test set and the available bandwidth of interconnects. This work first appeared at the *Thirteenth IEEE European Test Symposium*, Verbania, Italy, in May 2008.

The next paper is authored by Almukhaizim and Alsubaihi of Kuwait University, Kuwait, and Sinanoglu of University-Abu Dhabi, United Arab Emirates. They explore the problem of reducing peak power during scan shifting. Scan chains are partitioned to operate on separate clock phases and the clock phase for a scan chain is dynamically set by hardware on a per pattern basis. An integer linear program (ILP) determines the optimum partitioning schedule while accomplishing the minimum peak power objective.

The final contribution of this issue is an article by Gammel and Mangard of Infineon Technologies AG, Munich, Germany. The authors give a mathematical analysis of fault attacks and security in electronic systems. Readers will find several new results of theoretical and practical significance in this paper.

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