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# Editorial

**Vishwani D. Agrawal**

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Austin, Texas was the site of the *JETTA* Editorial Board meeting on November 2, 2010. It was attended by Magdy Abadir, Jacob Abraham, Vishwani Agrawal, Krishnendu Chakrabarty, Kwang-Ting (Tim) Cheng, Patrick Girard, Dimitris Gizopoulos, Charles Glaser (Springer), John Hayes, Bruce Kim, Erik Jan Marinissen, Peter Maxwell, Cecilia Metra, Nicola Nicolici, Rubin Parekhji, Michel Renovell, Matteo Sonza Reorda, Adit Singh, Haralampos Stratigopoulos (Guest Editor, Mixed-Signal Test, 2011), Mohammad Tehranipoor and Yervant Zorian. The Board discussed and adopted a time-line for the journal's peer review process. According to this new time-line the time between the initial submission and final decision, including any revisions, should range between 12 to 20 weeks.

This issue contains articles on diagnosis and characterization, mixed-signal test, memory test, test time reduction, and system test.

The first paper proposes on-chip hardware schemes for delay measurement. Authors are Datta, Sabastine, Raghunathan and Abraham of the University of Texas at Austin, and Carpenter and Nowka from IBM Research, Austin, Texas. They discuss implementations of modified Vernier delay line (MVDL) and skewed inverter delay line (SIDL).

The second paper is authored by Ladhar and Masmoudi from Electronics, Micro-technology and Communication Laboratory, Sfax, Tunisia. The authors construct intra-gate fault dictionaries to diagnose defects that are internal to cells of a failing chip.

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The third paper provides an embedded test solution for a mixed-signal test problem. Passive components of the circuit are characterized with the help of an analog test bus and a test controller. The authors of this paper are Hannu, Saikkonen, Häkkinen Karttunen and Moilanen from the University of Oulu in Finland.

In the fourth paper, Dubey and Garg of ST Microelectronics India Private Limited, Greater Noida, India and Mahajan of the University of Michigan, Ann Arbor, Michigan, USA examine resistive defects leading to read recovery faults of a static memory device. The proposed approach uses a delay line based self timed methodology and reduces the test time.

The next two papers continue the theme of test time reduction. Authors Namba and Ito of Chiba University in Japan discuss test compaction for a specific type of scan structure known as Chiba scan. The Chiba scan forms a scan register using only the master latches of the system while the slave latches are used for holding test data to facilitate two-pattern delay testing. The operation requires four clock signals. The second paper in this group is authored by Mehta and Devashrayee from Nirma University, Ahmedabad, India and Dasgupta of Indian Space Research Organization, Ahmedabad, India. Their scheme of a modified selective Huffman coding aims at an all-round test cost reduction through higher compression, reduced test hardware overhead and reduced test application time.

The final paper is authored by Gandini and Ruzzarin of Motorola Italia, Milan, Italy and Sanchez, Squillero and Tonda from Politecnico di Torino, Torino, Italy. They focus on software errors that would cause increased power dissipation in a mobile phone system. An example is a software bug that might prevent the system from entering an intended sleep mode. The technique requires adding new tests once such a malfunction is discovered.

This issue completes Volume 26 of *JETTA*. This volume contains two special issues. The first of these featured "Mixed-Signal Test" for which Karim Arabi served as guest editor. The second, a special issue on "High-Level Design Validation and Test" had Prabhat Mishra as guest editor. For 2011, we have planned two theme issues. Appearing first will be Mixed-Signal Test under the guest editorship of Haralampos Stratigopoulos and Krishnendu Chakrabarty. Following that will be Testing of Three-Dimensional Stacked Integrated Circuits whose guest editors are Erik Jan Marinissen and Yervant Zorian.

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