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Editorial

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Two new editors are joining the editorial board. They are Shawn Blanton of Carnegie Mellon University and Partha Pande of Washington State University. Shawn is an established researcher in the area of testing and is currently serving as the program chair of the *International Test Conference*. Partha is the new editor for the Newsletter of the Test Technology Technical Council of the IEEE Computer Society and was appointed by the Council. He started writing the Newsletter from October 2010, replacing Mohammad Tehranipoor who continues on the board as a regular editor. Biographies of the new editors appear in this issue.

A list of reviewers who conducted reviews for *JETTA* in 2010 appears in this issue. We acknowledge their contribution to the journal and thank them for devoting their expertise and time to serve the profession. Peer review is an essential and perhaps the most important part of our editorial procedure.

In the first paper of this issue, Nummer and Sachdev of University of Waterloo, Waterloo, Canada describe a design for a pipelined datapath whose performance can be assessed by a slow speed tester. This is done by inserting measurable delays in signal paths during test.

The second paper gives a design for a built-in circuit that conducts the drain leakage test (DLT) for detecting crystal defects, which could potentially affect the reliability of the device under test. The authors are Malandruccolo, Ciappa and Fichtner from Swiss Federal Institute of Technology (ETH), Zurich, Switzerland and Rothleitner from Infineon Technologies AG, Villach, Austria.

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The third and the fourth articles discuss the test data and power issues of scan testing. In a test compression scenario, some bits must be masked before the circuit response is compacted and transmitted to the tester. A simple masking scheme may reduce the masking control data from the tester and cause over-masking thereby resulting in loss of fault coverage. The first of these papers proposes a set of serially loaded registers for trade-offs between reduced over-masking and reduced tester data volume. The authors are Rabenalt and Goessel from University of Potsdam, Potsdam, Germany and Leininger from Infineon Technologies AG, Neubiberg, Germany. The second article in this group is authored by Zhou, Xiao, Ye and Wu from Harbin Institute of Technology, Harbin, China. They demonstrate the use of first distributing flip-flops among scan chains, then ordering those flip-flops within chains and, finally, organizing test data for a trade-off between reduced test data volume and reduced power consumption during test.

The fifth and sixth articles deal with microfuidic systems. A paper by Al-Gayem, Richardson and Burd of Lancaster University, Lancaster, UK and Liu from Moor Instruments Ltd., Axminster, UK describes methods for monitoring the reliability of sensor electrodes used in micro-fluidic systems used in bio-analytical instruments. The next paper is authored by Zhao and Chakrabarty of Duke University, Durham, NC. They propose the use of an exclusive-OR network, also implemented using microfluidic logic devices, to generate a compacted signal from multiple observation points for fault diagnosis in a digital microfluidic cell array.

The seventh paper describes a novel built-in self-test for linearity of a digital to analog converter (DAC). By reducing the number of measurements over the conventional all-code measurement test time is reduced. This paper is contributed by three authors from Taiwan. They are Ting

from National Kaohsiung University of Applied Science, Kaohsiung, Chang from National Cheng-Kung University, Tainan, and Huang from Motech Industries, Inc., Tainan.

This issue starts volume 27 of *JETTA*. Of the six issues this year, at least two will carry special themes. Appearing first will be a special issue on "Analog, Mixed-Signal, RF and MEMS Testing," for which guest editors are Haralampos Stratigopoulos and Krishnendu Chakrabarty. We will have another issue devoted to "Testing Three-Dimensional Stacked Integrated Circuits," for which Guest Editors are Erik Jan Marinissen and Yervant Zorian. We continue our special relationships with broad-theme test meetings such as *IEEE European Test Symposium* (ETS) through which selected papers from a workshop or symposium are submitted to *JETTA* and, if accepted by our peer review process, appear in regular issues. Cecilia Metra has been coordinating the ETS papers for several years. In addition, this year Fabian Vargas and Erika Cota are serving as guest editors of selected papers from the *IEEE Latin American Test Workshop* (LATW). The second, third and fifth papers of this issue are from ETS 2009.